MC6172

(Formerly MC6862)

2

2400 bps DIGITAL MODULATOR

The MC6172 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.

The modulator provides the necessary modulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6172 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data communication terminals, and I/O interfaces for counters.

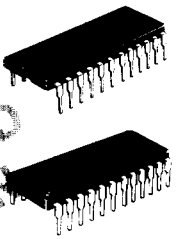
N-channel silicon-gate technology permits the MC6172 to operate using a single voltage supply and be fully TTL compatible.

The modulator is compatible with the MC6173 demodulator to provide medium-speed data communications capability.

- Clear-to-Send Delay Options
- 511-Bit CCITT Test Pattern
- Terminal Interfaces are TTL Compatible
- Compatible Functions for 201B/C Data Sets
- CCITT and U.S. Phase Options
- 1200/2400 bps Operation
- Answer-Back Tone
- The MC6173 Is the Companion Demodulator
- Application Note Available — AN-870

MOS
(N-CHANNEL, SILICON-GATE)

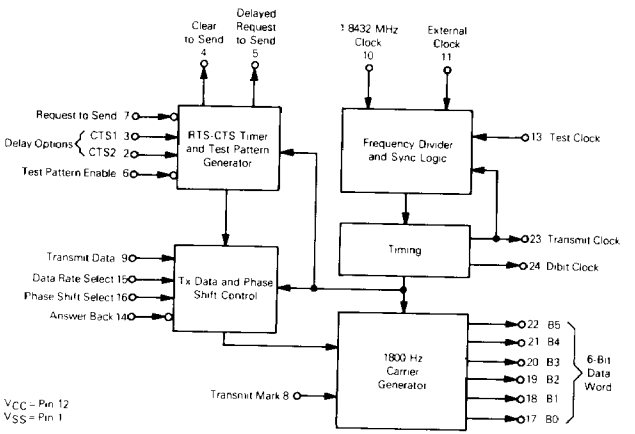
2400 bps MODULATOR



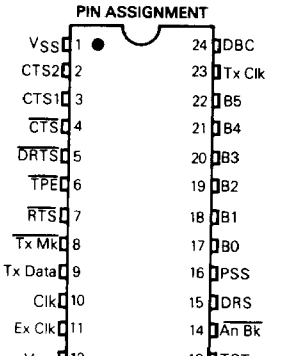
L SUFFIX
CERDIP PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 709

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	T_L to T_H 0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Package Cerdip Package	θ_{JA}	 120 65	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ±0.25 Vdc, V_{SS} = 0, $T_A = T_L$ to T_H, all outputs loaded as shown in Figure 1 unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	V_{SS} + 0.8	V
Input Current ($V_{in} = V_{SS}$) CTS1, CTS2, PSS, DRS, $\overline{An\ Bk}$, and $\overline{Tx\ MK}$ $\overline{RTS}$ and $\overline{TPE}$	I_{in}	– –	– –	−0.2 −1.6	mA
Input Leakage Current (V_{in} = 5.25 V, $V_{CC} = V_{SS}$)	I_{IL}	–	–	2.5	μA
Output High Voltage (I_{OH} = −0.04 mA, Load A) (I_{OH} = 0.0 mA, Load B)	V_{OH1} V_{OH2}	V_{SS} + 2.4 V_{CC} − 0.5 V	– –	V_{CC} V_{CC}	V
Output Low Voltage (I_{OL} = 1.6 mA, Load A)	V_{OL}	V_{SS}	–	V_{SS} + 0.4	V
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Internal Power Dissipation (Measured at $T_A = T_L$) (All inputs at V_{SS} except Pin 13 = 57.6 kHz and ALL outputs open)	P_{int}	–	210	315	mW
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% points)	t_r, t_f	–	–	1.0*	μs
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r, t_f	–	–	40	ns
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	–	70	%
Tx Data Setup Time (Figure 2)	t_{su}	35	–	–	μs
Tx Data Hold Time (Figure 2)	t_h	35	–	–	μs
Output Transition Times	t_r, t_f	–	–	5.0	μs

*Maximum Input Transition Times are ≤0.1 × Pulse Width or the specified maximum of 1.0 μs, whichever is smaller.

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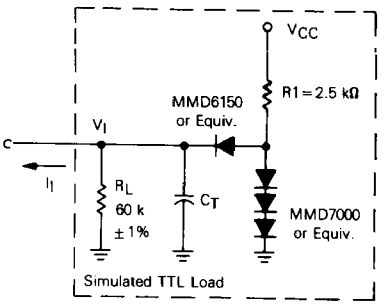
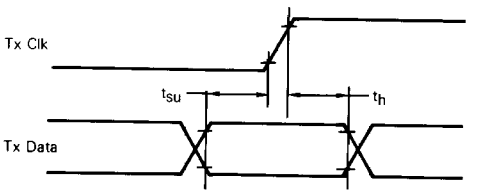
FIGURE 1 – OUTPUT TEST LOAD



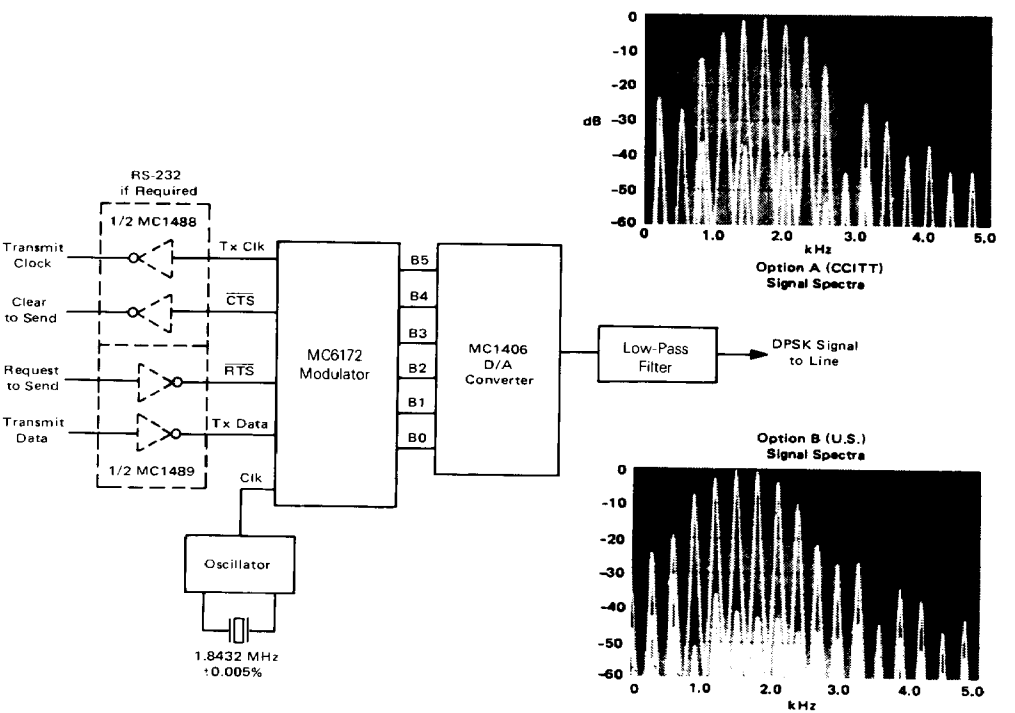
C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 2 – TRANSMIT DATA SETUP AND HOLD TIME



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3 – 2400 bps MODULATOR INTERFACE

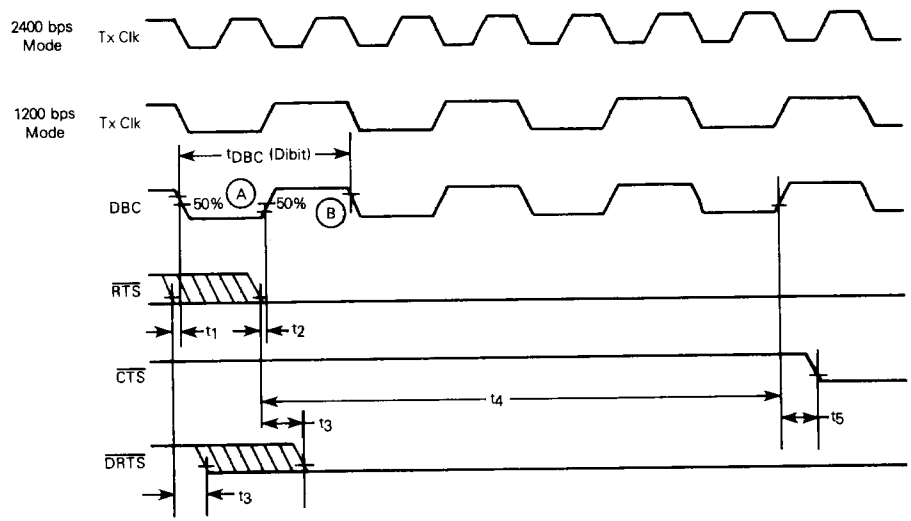


DELAY TIMINGS (See Figures 4 and 5)

Characteristic	Symbol	Min	Typ	Max	Unit
$\overline{RTS}$ to DBC Delay	t_1	–	–	8	μs
DBC to $\overline{RTS}$ Delay	t_2	45	–	–	μs
$\overline{RTS}$-$\overline{DRTS}$ Delay	t_3	–	–	35	μs
$\overline{RTS}$-$\overline{CTS}$ Delay					
CTS1 = 0, CTS2 = 1	t_4*	0	–	35	μs
CTS1 = 1, CTS2 = 0		8.56	–	9.35	ms
CTS1 = 1, CTS2 = 1		24.9	–	26.4	ms
CTS1 = 0, CTS2 = 0		147.0	–	154.0	ms
$\overline{CTS}$-DBC Delay					
CTS1 = 1, CTS2 = 0	t_5	–	–	35	μs
CTS1 = 1, CTS2 = 1		–	–	35	
CTS1 = 0, CTS2 = 0		–	–	35	
$\overline{RTS}$ to $\overline{CTS}$ Low	t_6	–	–	1.60	ms
$\overline{RTS}$ Min Delay	t_7	–	–	1.67	ms
DBC to $\overline{DRTS}$ Delay	t_8	–	–	35	μs
DBC Cycle Time	t_{DBC}	833.28	833.33	833.37	μs

*The reference frequency tolerance is not included.

FIGURE 4 – $\overline{RTS}$-$\overline{CTS}$ AND $\overline{RTS}$-$\overline{DRTS}$ DELAYS



$\overline{RTS}$-$\overline{CTS}$ delay options are selected by the CTS1 and CTS2 inputs, and are stated as time delay interval t_4. An $\overline{RTS}$ input signal synchronized about point A will synchronize $\overline{CTS}$ with the positive transition of DBC (Dibit Clock). Delay t_4 is measured with respect to the negative transition of $\overline{RTS}$.

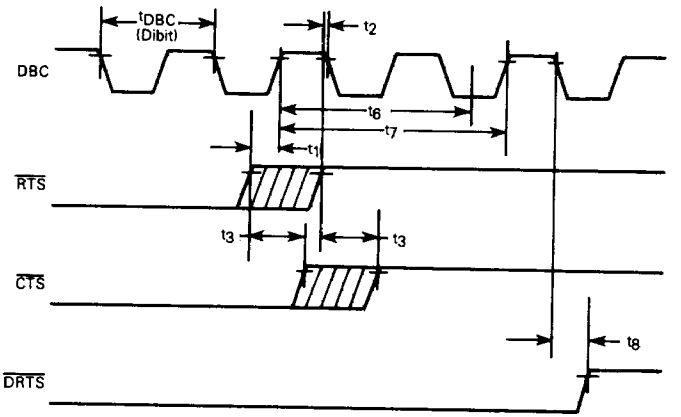
$\overline{RTS}$ signals synchronized with the positive transition of DBC (point B), will result in the same $\overline{CTS}$ delay (t_4). For this case the negative transition of $\overline{CTS}$ is synchronized with the negative transition of DBC with delay t_4 measured with respect to the negative transition of $\overline{RTS}$.

$\overline{DRTS}$ will go low within t_3 of the negative transition of $\overline{RTS}$. With the exception of the no-delay option, $\overline{CTS}$ will go low within t_5 of the positive transition of DBC, following the t_4 delay selected. This applies when $\overline{RTS}$ is synchronized to Point A as shown.

If $\overline{RTS}$ goes high and remains high ≥ 20 μs within time interval t_4, a reset of the internal $\overline{RTS}$-$\overline{CTS}$ timer function will occur. If $\overline{RTS}$ goes high for less than 20 μs, the circuit may or may not respond to this momentary loss of the $\overline{RTS}$ signal.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 5 — LOSS OF $\overline{RTS}$ TO $\overline{DRTS}$ DELAY



A positive transition of $\overline{RTS}$ after $\overline{CTS}$ has become active can result in different functional characteristics of the $\overline{CTS}$ and $\overline{DRTS}$ output signals, depending on the time duration that $\overline{RTS}$ remains inactive.

Under all conditions, $\overline{CTS}$ will go high within t_3 following a positive transition of $\overline{RTS}$. If $\overline{RTS}$ goes high in the shaded region shown (i.e., synchronized to the positive transition of DBC) and remains high beyond the time interval defined as t_7, then $\overline{DRTS}$ will go high within t_8 of the next negative transition of DBC. If $\overline{RTS}$ were to go low after t_7, the $\overline{RTS}$-$\overline{CTS}$ delay times given in Figure 4 will result.

If $\overline{RTS}$ goes high in the shaded region shown, and then returns low within time interval t_6, the negative transition of $\overline{CTS}$ will follow within 35 μs, and $\overline{DRTS}$ will remain in the active or low state. Under these conditions, the normal $\overline{RTS}$-$\overline{CTS}$ delay times are not encountered when $\overline{RTS}$ is reactivated. If $\overline{RTS}$ goes low for less than 20 μs, the circuit may or may not respond

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

DEVICE OPERATION

GENERAL

Figure 3 shows the modulator and its intra-connections. The data to be transmitted is presented in synchronous serial format to the modulator for conversion to DPSK signals used in transmission. The modulator output is digital; therefore, a D/A converter and a filter transform the signal to an analog form.

The control functions provide four different Clear-to-Send delay options. An Answer-Back tone is available for automatic answering applications. The modulator has a built-in 511-bit pseudorandom pattern generator for use in system diagnostic tests.

INPUT/OUTPUT FUNCTIONS

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ signal from the data terminal controls transmission from the modulator. A low level on $\overline{RTS}$ activates the modulator data output. A constant mark, for synchronization, is sent during the $\overline{RTS}$ to $\overline{CTS}$ delay interval. Termination of the transmission is accomplished by taking $\overline{RTS}$ high (see Figures 4 and 5).

Delayed Request to Send ($\overline{DRTS}$)

This output can be used to control transmission as specified by the Transmit Mark control input. $\overline{DRTS}$ follows the negative transition of $\overline{RTS}$, and goes negative within t_3 of the negative transition of $\overline{RTS}$ (Figure 4). The delay from a positive transition of $\overline{RTS}$ to a positive transition of $\overline{DRTS}$ is shown in Figure 5. The $\overline{DRTS}$ delay allows data within the modulator to be transmitted before transmission is inhibited.

Clear to Send ($\overline{CTS}$)

$\overline{CTS}$ follows $\overline{RTS}$ to both the logic 0 and logic 1 levels. The delay from a negative transition of $\overline{RTS}$ to a negative $\overline{CTS}$ transition is selectable by external strapping of CTS1 and CTS2. The delay from a positive transition of $\overline{RTS}$ to a positive $\overline{CTS}$ transition is less than t_4.

$\overline{CTS}$ will go low within t_5 after the positive transition of the Dibit Clock (see Figure 4) except when the non-delay option is selected. For the no-delay option, $\overline{CTS}$ follows $\overline{RTS}$ within t_5.

$\overline{RTS}$-$\overline{CTS}$ Delay Options (CTS1, CTS2)

The $\overline{RTS}$-$\overline{CTS}$ delays are selectable according to the following strapping options

$\overline{RTS}$-$\overline{CTS}$ Delay	CTS1	CTS2
0.0 + 0.035 ms, −0.0 ms	0	1
8.55 to 9.35 ms	1	0
24.90 to 26.4 ms	1	1
147.0 to 154.0 ms	0	0

Transmit Mark (Tx Mk)

The Transmit Mark control allows the system designer to select whether the Delayed Request to Send activitates and deactivates the transmission on the modulator chip or off the chip in the output amplifier.

When Tx Mk is high, transmission is controlled on the modulator chip, and occurs from the chip only when $\overline{DRTS}$ or Answer Back is in the logic 0 state (see Figure 6).

When Tx Mk is low, transmission is controlled off the modulator chip. In this mode, the modulator chip transmits marks at all times except when data or an Answer-Back tone is being transmitted (see Figure 6).

Test Pattern Enable ($\overline{TPE}$)

A 511-bit test pattern generator is contained on the modulator chip. This pattern is in accord with CCITT specification V52.

The 511-bit test pattern is activated by applying a logic 0 to $\overline{TPE}$. A mark (logic 1) condition on the Transmit Data input with $\overline{TPE}$ activated (logic 0) causes the test pattern to appear at the data output. A space (logic 0) condition on Tx Data with $\overline{TPE}$ activated causes the test pattern data to appear inverted at the data output.

Although the Motorola 2400 bps modulator contains a CCITT 511 test pattern generator it does not incorporate the 511 data randomizer or scrambler.

Random data applied to Tx Data with TPE activated causes the test pattern data to be scrambled (exclusive NORed) with the data, and the result appears at the data output.

The MC6173 demodulator does contain a built-in data descrambler, which is enabled by $\overline{TPE}$ input going active. To scramble data using the modulator, the circuit in Figure 7 must precede the Tx Data input of the modulator. Tx Data is added to the scrambler output pattern. Then the data is delayed by a full data bit before being transmitted by the modem. This assures a proper Transmit Data/Transmit Clock phase relationship.

If the data scrambler is to be an optional feature, then the transmit data multiplexer would also have to be built. This is selected by the Test Pattern Enable signal or any other signal that is found suitable.

The scrambling of data in the data comm environment is not done in an attempt to encrypt information in the normal sense of the word. Rather, the purpose of the scrambling of data is to guarantee that with respect to the modem carrier, there is always random data on the line with little chance for a long string of ones or zeros to exist. This is particularly important if an adaptive equalizer is being incorporated at the demodulator. The adaptive equalizer will require reasonably evenly distributed data to optimize its statistical response to the incoming signal. The normally used code is the CCITT 511 sequence which is exclusive ORed with data.

The test pattern generator can be enabled only when $\overline{CTS}$ and $\overline{RTS}$ are logic 0. If $\overline{TPE}$ is activated outside this time interval, the previously stated $\overline{RTS}$-$\overline{CTS}$ and $\overline{RTS}$-$\overline{DRTS}$ delays, shown in Figures 4 and 5, are not valid.

Data-Rate Select (DRS)

The modulator can transmit at either 2400 bps or 1200 bps. Both data rates utilize an 1800 Hz carrier signal and employ phase shifting at 1200 Hz. The 2400 bps rate is obtained by encoding two bits of data into each phase shift. The 2400 Hz rate is selected by applying a logic 1 to the Data-Rate Select lead. The 1200 Hz rate is selected by applying a logic 0 to DRS.

Phase-Shift Select (PSS)

Option A (CCITT) or Option B (U.S.) phase shift can be selected for 2400 bps operation. The input data format and phase shift relationship for these two options are as follows:

Data	PSS = 0 Option A*	PSS = 1 Option B
00	0°	+45°
01	+90°	+135°
11	+180°	+225°
10	+270°	+315°

*See example Figure 8.

FIGURE 6 — TRANSMIT MARK CONTROL

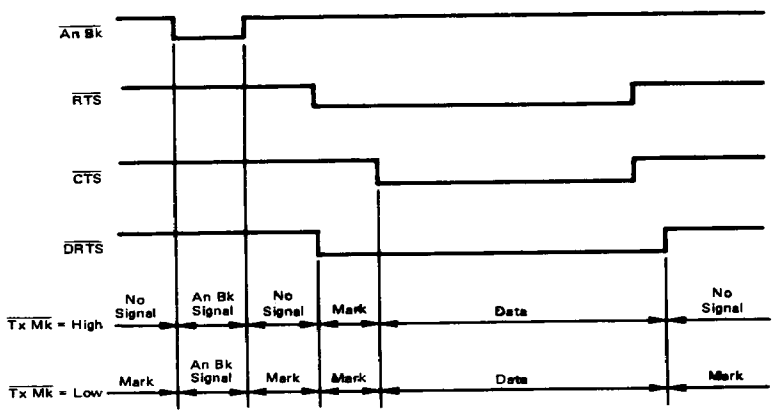


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FIGURE 7 — MODULATOR CCITT 511 DATA SCRAMBLER

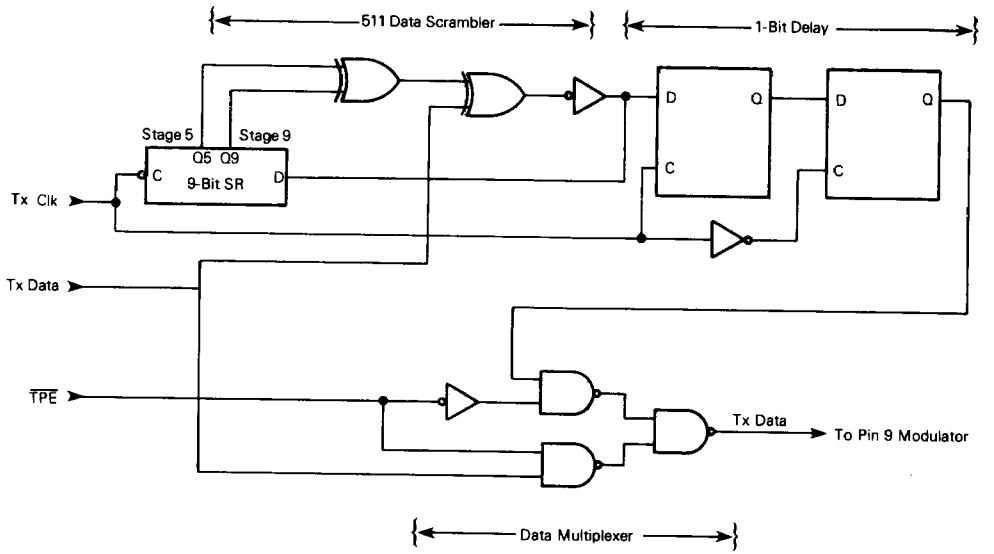
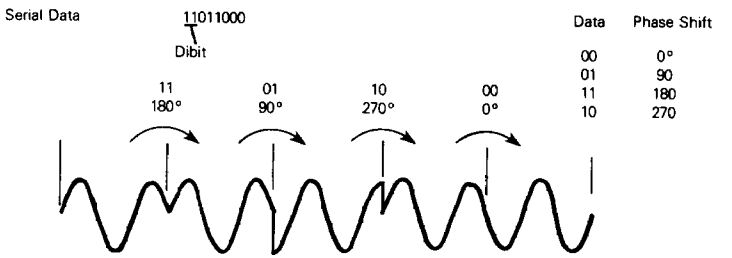


FIGURE 8 — EXAMPLE-CARRIER PHASE SHIFTS FOR OPTION A



For 1200 bps operation, Option C (CCITT) or Option D (U.S.) phase shift can be selected:

Data	PSS = 0 Option C	PSS = 1 Option D
0	+90°	+45°
1	+270°	+225°

Option C is selected by applying a logic 0 to the Phase Shift Select lead when the Data Rate Select lead is strapped for 1200 bps operation (logic 0). Option D is selected by applying a logic 1 to PSS with DRS at logic 0. The phase shifts shown are the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next dibit.

Transmit Data (Tx Data)

Transmit Data is the serial binary information presented for DPSK modulation. A high level represents a mark. For timing, see Transmit Clock (Figure 4).

Transmit Clock (Tx Clk)

A 2400/1200 Hz Transmit Clock output is provided for the communication terminal. The Transmit Data signal is sampled on the positive transition of Transmit Clock. The Transmit Data to Transmit Clock setup and hold time requirements are shown in the Electrical Characteristics Table and in Figure 2.

Dibit Clock (DBC)

A 1200 Hz Dibit Clock identifies the modulation timing. This signal goes negative less than 100 μs prior to the start of dibit modulation.

External Clock (Ex Clk)

A 2400/1200 Hz clock signal applied to the External Clock lead causes Transmit Clock to be synchronized with Ex Clk. This input must have an accuracy within ±0.005%.

When no transitions occur on this input, the internal clock provides the 2400/1200 Hz transmit timing signal. Fast synchronization of Tx Clk to Ex Clk is not provided on the chip. *When Ex Clk is not used, it should be tied to either the logic 0 or logic 1 state.*

1.8432 MHz (Clk)

This input must be a square wave with rise and fall times of less than 40 ns and a 50 ±20% duty cycle. The clock accuracy must be written ±0.005%.

Answer Back ($\overline{\text{An Bk}}$)

A logic 0 level applied to Answer Back causes a 2025 Hz carrier to be generated on the modulator chip instead of a phase shifted 1800 Hz carrier. A logic 1 level applied to $\overline{\text{An Bk}}$ enables the modulator to generate the normal phase shifted 1800 Hz carrier signal, as shown in Figure 6. The time delay from a transition on $\overline{\text{An Bk}}$ to the appropriate signal at the modulator chip output is less than 2 ms.

Activation of $\overline{\text{An Bk}}$ (a logic 0) will disable all other operation modes including the $\overline{\text{Tx Mk}}$ function, and will reset $\overline{\text{CTS}}$ to an inactive state along with the $\overline{\text{RTX}}$-$\overline{\text{CTS}}$ internal timer. $\overline{\text{An Bk}}$ should therefore be activated only before initiating $\overline{\text{RTS}}$ or after loss of the $\overline{\text{DRTS}}$ output signal. The combination of a logic 0 on $\overline{\text{An Bk}}$ with a logic 0 on $\overline{\text{TPE}}$ is not used in normal system operation, and hence is used as a reset input during device test.

Digital Output (B0-B5)

These outputs are designed to interface with a 6-bit digital-to-analog converter. The resultant signal out of the D/A is the differential phase shift keyed signal quantized at a 14.4 kHz rate. A low-pass filter can then be used to smooth the data transitions. B0 is the least-significant bit, and the positive level the active state.

Test Clock (TST)

A test signal input is provided to decrease test time of the chip. *In normal operation this input must be strapped low.*