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TECHNICAL DATA

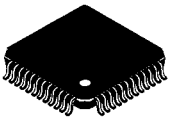
MC141625

Advance Information

Advanced NTSC/PAL Comb Filter
CMOS

The Advanced NTSC/PAL Comb Filter is a video signal processor for VCRs and TVs. It separates the Luminance Y and Chrominance C signals from the NTSC composite video signal by using digital signal processing techniques which minimize dot-crawl and cross color. This filter allows a video signal input of an extended frequency bandwidth by using a 4 fsc clock. The built-in A/D and D/A converters allow easy connections to analog video cassette recorders and television circuits.

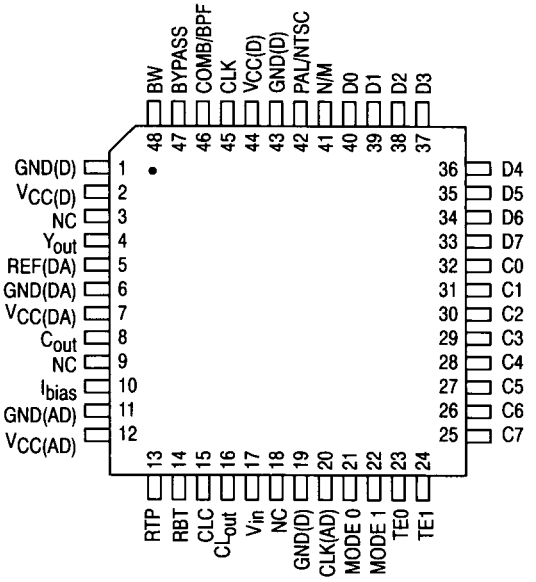
- Built-In High Speed 8-Bit A/D Converter
- Two Line or Four Line Memories
- Advanced Combing Process
- Two 8-Bit D/A Converters
- Built-In Clamp Circuit
- On-Chip Reference Voltage Regulator for A/D Converter
- Digital Interface Mode



FU SUFFIX
QFP
CASE 898

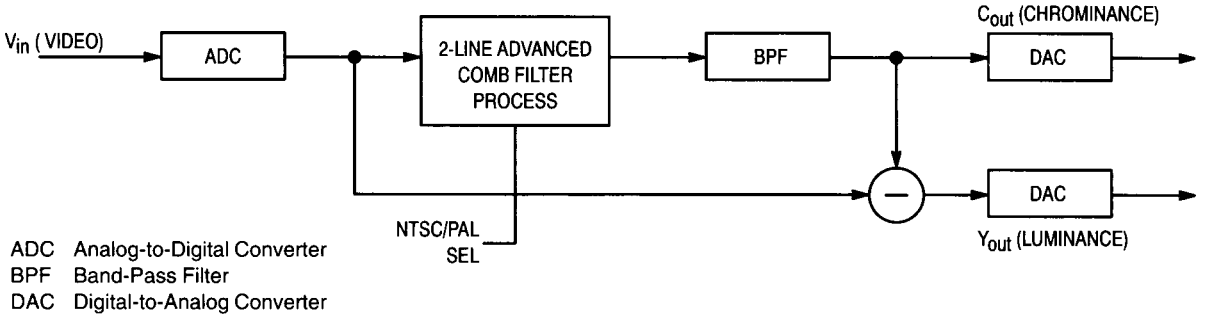
ORDERING INFORMATION

MC141625FU Quad Flat Package (QFP)



NC = NO CONNECTION

SIMPLIFIED BLOCK DIAGRAM



ADC Analog-to-Digital Converter
BPF Band-Pass Filter
DAC Digital-to-Analog Converter

This document contains information on a new product. Specifications and information herein are subject to change without notice.

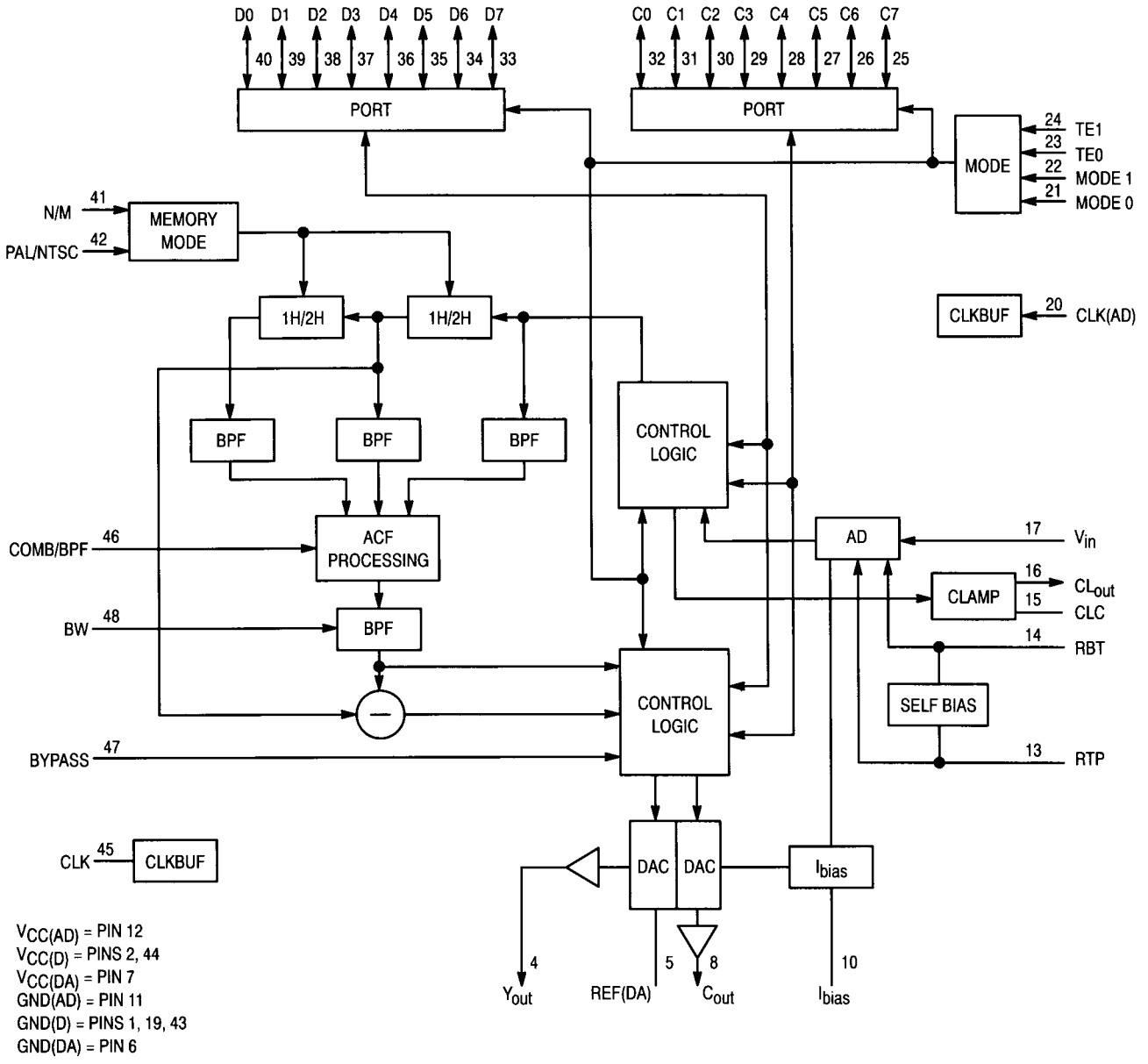


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Value	Unit
DC Supply Voltage (Referenced to GND), $V_{CC(AD)}$, $V_{CC(D)}$, $V_{CC(DA)}$	V_{CC}	– 0.5 to + 7.0	V
DC Input Voltage (Referenced to GND)	V_{in}	– 1.5 to V_{CC} + 1.5	V
DC Output Voltage (Referenced to GND)	V_{out}	– 0.5 to V_{CC} + 0.5	V
DC Input Current (per pin)	I_{in}	± 20	mA
DC Output Current (per pin)	I_{out}	± 25	mA
DC Supply Current (V_{CC} and GND pins)	I_{CC}	± 100	mA
Power Dissipation	P_D	750	mW
Storage Temperature	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage ($V_{CC(AD)}$, $V_{CC(D)}$, $V_{CC(DA)}$)	V_{CC}	4.5	5.0	5.5	V	
Operating Supply Current	I_{CC}	—	90	120	mA	1
Operating Power Dissipation	P_D	—	450	660	mW	1
Ambient Operating Temperature	T_A	– 20	—	80	°C	

NOTE:
1. During normal mode.

CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit	Notes
Clock Frequency		f_c	12	17.734475	20	MHz	1
Input Level Clock		V_c	500	—	—	mV p-p	2
High Level Input Voltage	CLK, CLK(AD)	V_{IH}	3.15	—	—	V	3, 4
Low Level Input Voltage	CLK, CLK(AD)	V_{IL}	—	—	1.1	V	3, 4
Clock Duty Cycle	CLK, CLK(AD)	DC	40	50	55	%	3, 4

NOTES:
1. During PAL system B, G, H, I.
2. In normal and CCF modes.
3. CLK in digital input comb filtering and digital output comb filtering mode.
4. CLK(AD) is available only during digital input comb filtering mode.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	± 1.0	± 1.5	LSB
Differential Nonlinearity	DNL	—	± 0.5	± 1.0	LSB
Analog Input Range	V_{in}	—	3.0	3.3	V p-p
Top Reference Level	V_{TP}	V_{BT}	—	$V_{CC(AD)}$ – 0.3	V
Bottom Reference Level	V_{BT}	1.4	—	V_{TP}	V
Top Self Reference Level	V_{TPS}	4.5	4.6	4.7	V
Bottom Self Reference Level	V_{BTS}	1.45	1.55	1.65	V
Maximum Analog Input Range During Self Reference	V_{ins}	2.9	3.1	3.2	V p-p
Reference Resistor Value	R_{ref}	250	350	450	Ω

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High Level Input Voltage	MODE 0, MODE 1, BW, C0 – C7, D0 – D7, PAL/NTSC, Bypass	V_{IH}	3.15	—	—	V
Low Level Input Voltage	MODE 0, MODE 1, BW, C0 – C7, D0 – D7, PAL/NTSC, Bypass	V_{IL}	—	—	1.1	V
Input Leakage Current (V_{in} = $V_{CC(D)}$ or GND(D))	MODE 0, MODE 1, BW, C0 – C7, D0 – D7, PAL/NTSC, Bypass	I_{lkg}	—	—	± 10	µA
Data Setup Time (During Digital Comb Filter Mode)	D0 – D7	t_{su}	20	—	—	ns
Data Hold Time (During Digital Comb Filter Mode)	D0 – D7	t_h	20	—	—	ns
Data Input Rise Time (During Digital Comb Filter Mode)	D0 – D7	t_r	—	—	10	ns
Data Input Fall Time (During Digital Comb Filter Mode)	D0 – D7	t_f	—	—	10	ns
Output Data Delay (During Digital Comb Filter Mode)	D0 – D7	t_d	—	50	—	ns

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Y/C Separation		—	40	—	—	dB
Band-Pass Filter	– 3 dB During PAL System B, G, H, I Wide Bandwidth	— —	— —	± 1.6 ± 1.3	— —	MHz
Band-Pass Filter	– 3 dB During PAL System B, G, H, I Narrow Bandwidth	— —	— —	± 1.3 ± 1.1	— —	MHz

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	—	± 1	LSB
Differential Nonlinearity	DNL	—	—	± 0.5	LSB
Analog Output Voltage, Y_{out}	V_{YO}	1.1	1.2	1.3	V p-p
Analog Output Voltage, C_{out}	V_{CO}	1.1	1.2	1.3	V p-p
Full Scale Voltage, Y_{out}	V_{YFS}	1.3	1.5	1.7	V
Full Scale Voltage, C_{out}	V_{CFS}	1.3	1.5	1.7	V
Zero Scale Voltage, Y_{out}	V_{YZS}	0.1	0.3	0.5	V
Zero Scale Voltage, C_{out}	V_{CZS}	0.1	0.3	0.5	V
Output Impedance	Z_O	—	100	300	Ω

ADC – DAC GENERAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage Gain (During Self Bias)	—	– 8.9	– 8.0	– 7.1	dB
Output Bandwidth (at – 3 dB During PAL System B, G, H, I)	—	—	7.3	8.0	MHz
Differential Gain	DG	—	—	5	%
Differential Phase	DP	—	—	5	Deg
Bias Current (I_{bias} resistor = 10 kΩ)	I_{bias}	—	135	—	μA

CLAMP CIRCUIT CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Clamp Mode Output Saturation Voltage, CL_{out}	V_{clys}	2.8	3.1	—	V
Bias Mode Output Voltage, CL_{out}	V_{CLC}	2.95	3.05	3.15	V

NOTE:

Clamp Mode Output Voltage, V_{cly} (Non-input when connecting V_{in} – CL_{out})

$$V_{cly} = (V_{TP} - V_{BT}) (N + 1) / 256 + V_{BT} \pm 50 \text{ mV}$$

where N: Clamp Code Input (N < 255)

- If the calculated value of the output voltage, $V_{cly} > V_{clys}$, then $V_{cly} = V_{clys}$
- Clamp Value N is fixed during the digital input comb filtering mode and the digital output comb filtering mode, fixing N = 8.

Bias Mode Output Voltage, V_{CLC} (Non-input when connecting V_{in} – CL_{out})

$$V_{CLC} = (V_{TP} - V_{BT}) / 2 + V_{BT} \pm 10\%$$

BYPASS CIRCUIT CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Min	Typ	Max	Unit
Bypass Switch Time During PAL	—	– 2 H	—	
Bypass Switch Time During NTSC	—	– 1 H	—	

GENERAL SIGNAL DELAY (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Min	Typ	Max	Unit
During PAL B, G, H, I (fsc = (1135/4 + 1/625)fh)	—	129.099	—	μs
During NTSC (fsc = (455/2)fh)	—	64.917	—	μs
During PAL/N (fsc = (917/4 + 1/625)fh)	—	129.081	—	μs
During PAL/M (fsc = (909/4)fh)	—	128.195	—	μs

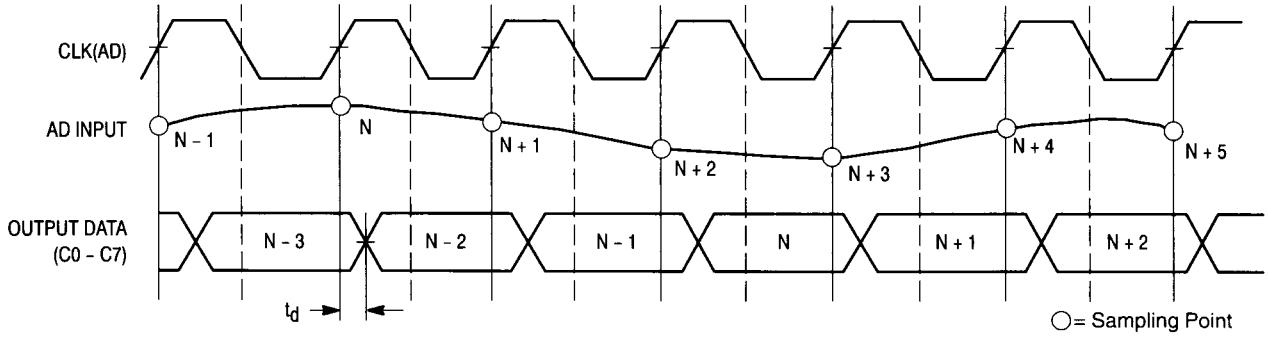


Figure 2a. A/D Converter Timing Diagram (During Digital Input Comb Filtering Mode)

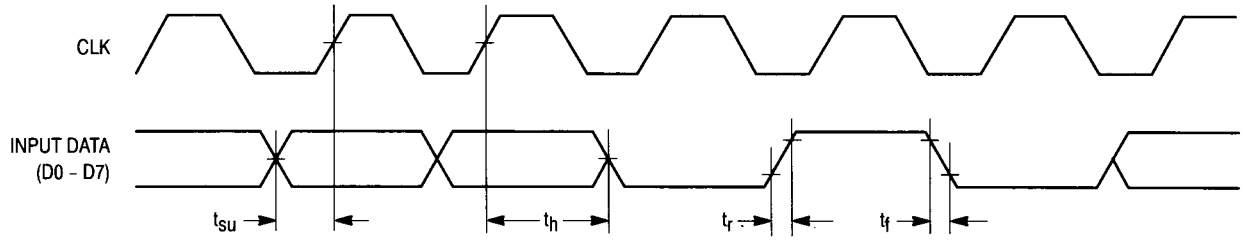


Figure 2b. Digital Signal Input Timing Diagram (During Digital Input Comb Filtering Mode)

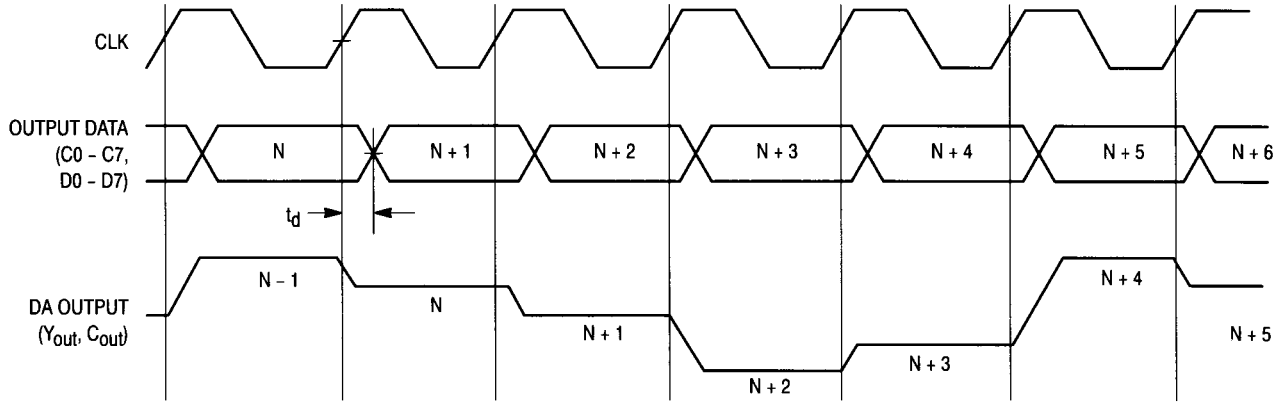


Figure 2c. Output Signal Timing Diagram (During Digital Output Comb Filtering Mode)

Figure 2. Timing Diagrams

PIN DESCRIPTIONS

Pin	Pin Name	Function
1	GND(D)	GND for Digital circuit.
2	$V_{CC(D)}$	Power supply for Digital circuit.
3	NC	No connection. Generally GND level.
4	Y_{out}	Luminance signal output.
5	REF(DA)	Reference for D/A converter. Generally connected to GND(DA) through a multilayer ceramic capacitor (0.1 μF).
6	GND(DA)	GND for D/A converter.
7	$V_{CC(DA)}$	Power supply for D/A converter.
8	C_{out}	Chrominance signal output.
9	NC	No connection. Generally GND level.
10	I_{bias}	Bias circuit current control for A/D, D/A converters. Generally connected to GND(DA) through an external resistor.
11	GND(AD)	GND for A/D converter.
12	$V_{CC(AD)}$	Power supply for A/D converter.
13	RTP	Top reference input for A/D converter. Supplies top reference voltage internally.
14	RBT	Bottom reference input for A/D converter. Supplies bottom reference voltage internally.
15	CLC	Clamp time constant setting pin.
16	CL_{out}	Voltage output for clamp. It can clamp an input signal by connecting with V_{in} and inputting the video signal by ac coupling.
17	V_{in}	A/D converter input. Maximum input voltage is 3.3 V p-p.
18	NC	No connection. Generally GND level.
19	GND(D)	GND for Digital circuit.
20	CLK(AD)	CLK input for A/D converter. Available only in Digital input comb filtering mode and a portion of test mode. Input level is CMOS level.
21, 22	MODE 0, 1	MODE inputs. GND level during Normal mode.
23, 24	TE0, TE1	Test mode input. Generally GND level.
25 to 32	C7 – C0	Clamp level input. Digital input/output interface 1.
33 to 40	D0 – D7	Digital Input/Output Interface 2. General GND level.
41	N/M	Pins for PAL N and PAL M. Generally GND level.
42	PAL/NTSC	PAL/NTSC mode input. Ground level during PAL mode.
43	GND(D)	GND for Digital circuit.
44	$V_{CC(D)}$	Power supply for Digital circuit.
45	CLK	CLK input. AC coupling input by external capacitor. Minimum CLK input level is 500 mV p-p during normal and CCF modes.
46	Comb/BPF	Comb Filter/Band Pass Filter Switching Input. Generally operates as comb filter at GND level.
47	Bypass	Filter bypass mode pin. Generally GND level.
48	BW	Chrominance bandwidth selecting input. Narrow bandwidth in LOW level.

Figure 3 shows the I/O signals of the Advanced NTSC/PAL Comb Filter.

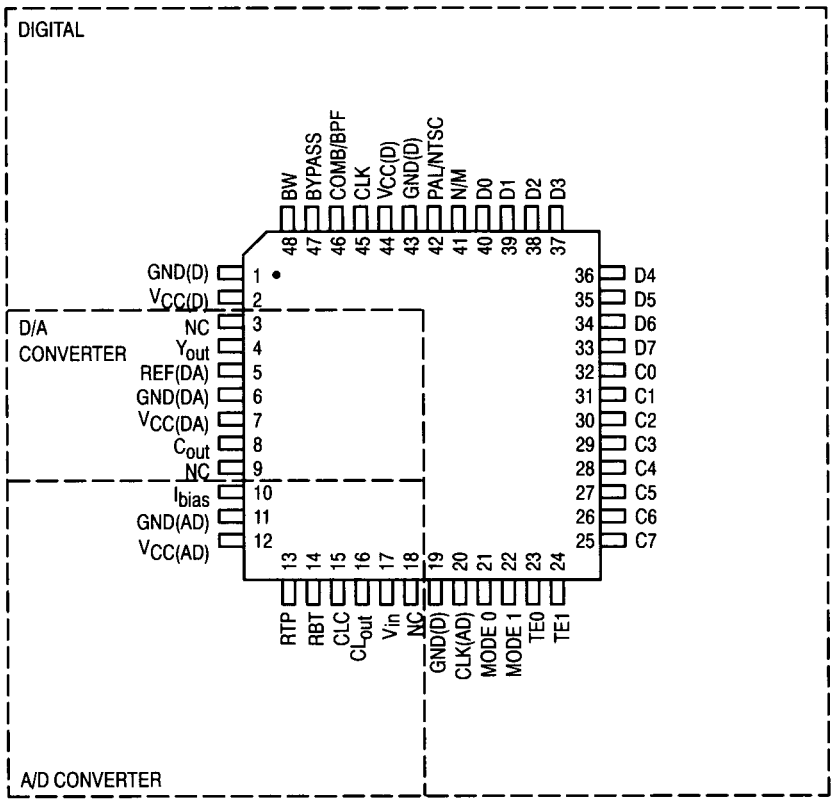


Figure 3. Pin Assignment

DEVICE DESCRIPTION

INTRODUCTION

The Advanced NTSC/PAL Comb Filter is a high-performance HCMOS digital filter with built-in A/D and D/A converters. The basic function of the chip is the separation of the Luminance Y and Chrominance C signals from the NTSC composite video signal. The Advanced NTSC/PAL Comb Filter minimizes the problems often generated by Y/C separation such as dot-crawl and cross color. It uses a 14.3 MHz clock for NTSC or 17.7 MHz clock for PAL that allows an extended frequency bandwidth video signal to be input. This Y/C separation is realized by the digital advanced comb filters. Figure 1 shows the complete block diagram for the Advanced NTSC/PAL Comb Filter.

ADVANCED NTSC/PAL COMB FILTER DESCRIPTION

Figure 4 is the simplified block diagram of the Advanced NTSC/PAL Comb Filter chip. There are three major functions represented on this block diagram. The first block is the analog-to-digital conversion block. The high speed 8-bit binary A/D converter converts the incoming analog video signal to an 8-bit binary data stream. The conversion frequency is 14.3 MHz for NTSC or 17.7 MHz for PAL, which is four times the color subcarrier frequency. The maximum analog video input is 3.3 V p-p.

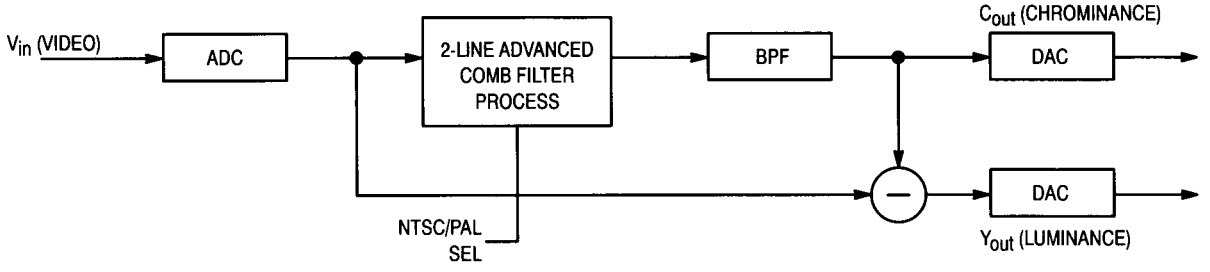


Figure 4. Simplified Block Diagram

The second block contains the Advanced NTSC/PAL Comb Filter algorithm. The digital data from the A/D converter is processed by the algorithm of the Advanced NTSC/PAL Comb Filter. The composite video is filtered by the band-pass filter (BPF) and separated into the Luminance Y and Chrominance C signals. The Comb/BPF pin allows external selection of either the comb filter algorithm or band-pass filtering.

The third block is the digital-to-analog conversion block. Two 8-bit D/A converters convert the luminance and chrominance into analog outputs. The conversion frequency is four times the subcarrier signal (14.3 MHz for NTSC or 17.7 MHz for PAL). The chrominance analog output is biased with a dc offset of half the value of the D/A converter reference.

A voltage reference for clamping is built into the chip. It produces a clamp voltage by comparing the output code of the A/D converter to the external clamp level input signal. This voltage is output via the CL_{out} pin and provides the capability to do on chip dc restoration of the video signal. The input video signal can be clamped by connecting CL_{out} to the video input, and inputting a video signal with ac coupling.

A/D Converter

The composite video signal input is converted to the digital code by the high speed 8-bit A/D converter. The input voltage range is determined by the value of the reference voltage inputs, RBT and RTP. The limits for the converter are 1.4 V minimum for RBT and $V_{CC(AD)} - 0.3$ V maximum for RTP. This produces a maximum conversion value of 3.3 V p-p maximum video input signal for $V_{CC(AD)}$ of 5 V. A self-bias function generating $V_{TP} = 4.6$ V, $V_{BT} = 1.55$ V can be realized by connecting the internal A/D converter reference voltage supply with the A/D converter reference pin. The sampling clock frequency of the A/D converter is 14.3 MHz for NTSC or 17.7 MHz for PAL, which is four times the color subcarrier frequency.

Clamp Voltage Regulating Circuit

The clamp voltage regulating circuit sync tip clamps the input signal when the V_{in} pin is connected to the CL_{out} pin and the video signal is input using ac coupling. It compares the digital value of the clamp level input, C0 – C7, with the A/D converter output code. The clamp voltage is output by the CL_{out} pin. The clamp circuit operates as though the sync tip level of the video signal is synchronized with the digital value input to C0 – C7.

In the digital input comb filtering mode and the digital output comb filtering mode, the video signal is clamped by fixing the internal clamp level to ($08). The value of C0 – C7 is ignored by the clamp circuit with these operating modes.

The circuit operates in the bias mode during the CCF mode. It outputs half the value of the A/D converter reference voltage from CL_{out}. The input video signal is biased at half of the A/D converter reference voltage by connecting the CL_{out} with V_{in} and inputting the video signal via ac coupling.

Advanced NTSC/PAL Comb Filter

The Advanced NTSC/PAL Comb Filter is a digital comb filter developed for use in either the NTSC or PAL system. The vertical correlation circuit provides high picture quality and high resolution and requires no adjustment for its Y/C separation. By proper selection of the PAL/NTSC pin and N/M pin combination, the PAL B, G, H, I, PAL M, PAL N, or NTSC method can be realized. The clock frequency should be either 14.3 MHz, which is four times the NTSC subcarrier, or 17.7 MHz, which is four times the PAL subcarrier. Table 1 shows the relationship between the PAL/NTSC pin, N/M pin, and the color TV methodology.

Table 1. Color TV Conversion Function

System	PAL/NTSC	N/M
PAL B, G, H, I	L	L
NTSC	H	L
PAL N	L	H
PAL M	H	H

The Comb/BPF pin can be used to select between band-pass filtering and comb filtering. When the Comb/BPF pin is at H level, the separated Y/C output is filtered by the band-pass filter. There are two band-pass filters that have different bandwidths built in to this chip, and this allows the selection of color signal bandwidth via an external BW pin. Table 2 shows the relationship of the BW pin and the bandwidth. Generally, the bypass pin operates as the advanced comb filter at ground level. By setting this pin at H level, the input video signal can be outputted as Y_{out} output and C_{out} output without filtering.

Table 2. Bandwidth Conversion Function

Bandwidth	BW
Narrow	L
Wide	H

D/A Converter

The luminance and chrominance signals separated in the advanced comb filtering portion are converted to analog signals by two 8-bit D/A converters. The output voltage range is from 0.3 V to 1.5 V, 1.2 V p-p. The sampling clock of the D/A converter is 14.3 MHz for NTSC or 17.7 MHz for PAL. This is the same as the A/D converter.

OPERATING MODES

The Advanced NTSC/PAL Comb Filter can be operated in any of four modes. These modes are fixed by a digital code inputted into MODE 0 and MODE 1. The descriptions of the four types of operating modes are:

Normal Mode

This mode is for the normal Y/C separation. The video signal input to the A/D converter is separated into its Y and C components and output as analog information from the D/A converter outputs. The clamp circuit operates as sync tip clamp by connecting CL_{out} with V_{in}, and clamps the input video signal to the digital value input at C0 – C7.

Chrominance Comb Filter (CCF) Mode

This mode reduces the noise of a chrominance signal. The chrominance signal input to the A/D converter is filtered by the Advanced NTSC/PAL Comb Filter algorithm, and the filtered chrominance signal is output from C_{out} after reducing the accumulated noise. The Y_{out} subtracting C_{out} components (noise components) removed by the comb filter algorithm are output at Y_{out}. The clamp circuit operates in the bias mode and biases the chrominance signal at the half point of the A/D converter reference voltage if CL_{out} is connected to V_{in}.

Digital Input Comb Filter Mode

In this mode the comb filter is used as two separate blocks, the A/D converter portion, and the filter and D/A portion. This mode can re-input and filter converted digital data output by the A/D converter after arbitrarily being digitally processed by external circuits. The converted digital data outputs into C0 – C7. Moreover, the data input into D0 – D7 is filtered by the Advanced NTSC/PAL Comb Filter algorithm, and is output as an analog signal from Y_{out} and C_{out}. The two blocks can can operate independently with different frequency and phase clock signals. The CLK(AD) pin is the clock input to the A/D converter block and the CLK pin is the clock source for the filter and D/A converters. At this time, the clamp circuit works as a sync tip clamp when CL_{out} is connected to V_{in}, and clamps the input video signal to the internally fixed digital value ($08).

Digital Output Comb Filtering Mode

This mode outputs digital values of the luminance and chrominance signals in addition to functioning as a standard analog output Y/C separator. This allows arbitrary digital processing of the filter-processed Y and C digital outputs by an external circuit. It interfaces with an analog circuit easily, since both analog Y and C signals are output at the same time.

The video signal input to the A/D converter is converted to digital data, and forwarded to the filter portion. The Y/C separated data from the filter portion is output from Y_{out} and C_{out} after the D/A conversion. At the same time, the filter portion output is also forwarded to the digital interface and the luminance digital value is output from C0 – C7 and the chrominance digital value is output from D0 – D7. With this mode, the clamp circuit works as a sync tip clamp with CL_{out} connected to V_{in}, and clamps the input video signal internally to the fixed digital value ($08).

Table 3 shows the relationship between the MODE pins and MODE condition.

Table 3. Operating MODE Switching Function

Mode	MODE 1	MODE 0
Normal Mode	L	L
CCF Mode	L	H
Digital Input Comb Filtering Mode	H	L
Digital Output Comb Filtering Mode	H	H

APPLICATION DESIGN CONSIDERATIONS

V_{CC}, GND

To maximize the performance of the MC141625, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC141625. Separate analog and digital grounds will reduce noise and conversion errors. In addition, separate filters on analog V_{CC} and digital V_{DD} will also help to minimize noise and conversion errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device with the performance and speed of the MC141625, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DD} and V_{CC} can be done by bussing, to do so with the ground system is disastrous.

A 1-inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1-inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. 47 μF tantalum capacitors are recommended. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 μF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD (electrostatic discharge) susceptibility. Connect the high-capacity and high-frequency capacitors as close as possible to all analog V_{CC}, digital V_{DD}, and ground pins. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 μF capacitance on V_{CC} and V_{DD} at each device, and keep all leads as short as possible.

V_{in}

In order to prevent flyback noise on the video input, it is necessary to keep the bandwidth to less than 1/2 the clock frequency by using an area filter. Here the amplifier used as an input buffer needs a wide bandwidth and driving capability. Moreover, to minimize external noise effects, drive the V_{in} pin with a low impedance amplifier and keep the V_{in} pin as close as possible to the amplifier output.

When using the built-in clamp circuit, connect CL_{out} to V_{in} and input signals after ac coupling by using a high-performance, high-frequency capacitor of 1 to 0.1 μF capacitance. In this case, keep the V_{in}, CL_{out}, coupling capacitor, and buffer-amplifier wiring as short as possible. Pay attention to the external noise and parasitic impedance.

CLC

The CLC pin sets the clamp circuit speed with an external capacitor and resistor.

Generally, the capacitor and resistor are arranged in a row and connected to GND(AD). Select a capacitor that minimizes the dielectric absorbing error. When the capacitor capacity is reduced, the shift speed of the video signal to $V_{CC(AD)}$ side is accelerated. If the resistor value is too small at this point, sagging will appear in the video signal. Also, if the capacitor's capacity is too large, the clamp speed will slow down; therefore, it is very important to pay attention to the setup of the resistor and capacitor values.

DA REFERENCE

REF(DA) is a DA converter reference decoupling pin for both the Y_{out} and C_{out}. Bypass to GND(DA) by applying a high-performance, high-frequency capacitor as close to the pin as possible. A 0.1 μF multilayer ceramic capacitor is recommended.

AD REFERENCE

The RTP and RBT pins have a self-bias function that internally generates V_{TP} = 4.6 V and V_{BT} = 1.55 V. It acknowledges the A/D converter analog input dynamic range. A stable performance can be achieved by applying a high performance frequency capacitor as close as possible to the RTP and RBT pins and bypassing to GND(AD).

A 0.1 μF multilayer ceramic capacitor and a 10 μF tantalum capacitor are recommended.

CLOCK INPUT

The clock frequency inputs is 17.734475 MHz during PAL B, G, H, I modes; 14.32823 MHz during PAL N mode; 14.30245 MHz during PAL M mode; or 14.31818 MHz during NTSC mode; which is four times the frequency of the subcarrier. The minimum input level is 500 mV p-p. It should be synchronized with the subcarrier of the video signal.

The clock line should be wired with the shortest wire and be separated from other circuits to minimize cross coupling to other signals. The CLK(AD) pin is used only during digital input comb filtering mode; therefore, it should be at GND level unless the device is used in the digital input comb filtering mode.

I_{bias}

The I_{bias} pin is used to set up the bias current for the AD and DA converters. Connect an external resistor between the I_{bias} and GND(DA).

DIGITAL INPUT COMB FILTERING MODE

Connect CLK(AD) to GND(D) when the AD converter is not being used. Connect D0 – D7 to GND(D) when the DA converter and filter are not being used. This is to eliminate any unnecessary operation of blocks that are not being used.

LATCH–UP

The $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins connect to power supplies that are independent from each other. Therefore, latch-up may occur when the power is applied. To eliminate latch-up, apply power to the $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins simultaneously.

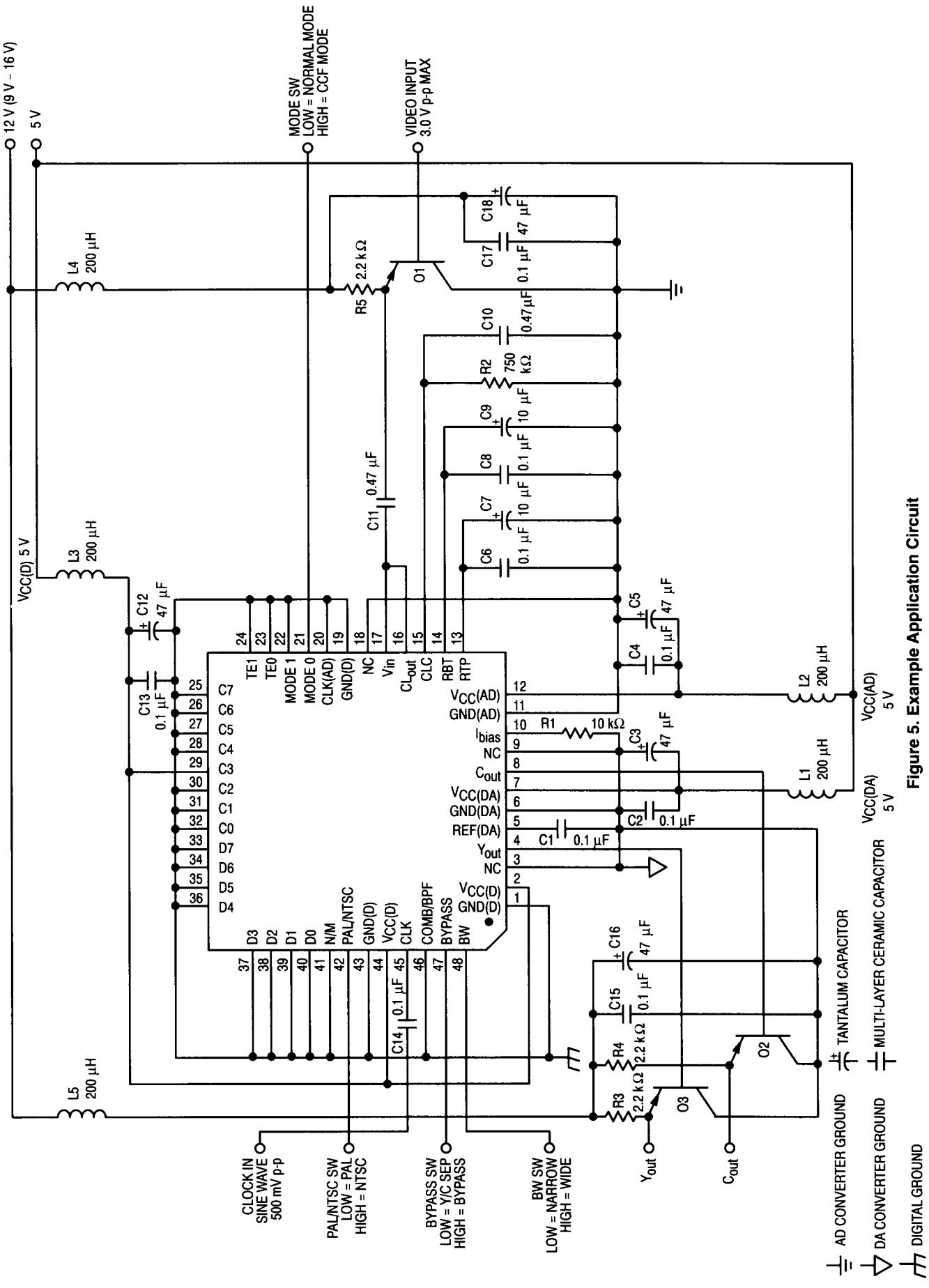
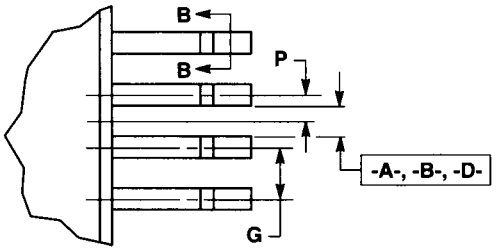


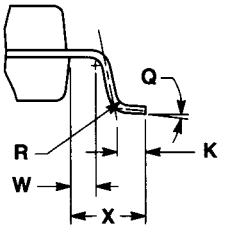
Figure 5. Example Application Circuit

PACKAGE DIMENSIONS

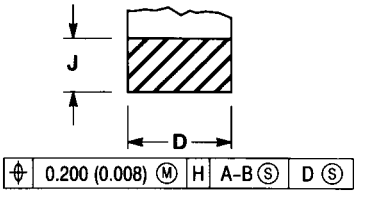
FU SUFFIX
48-LEAD QFP
CASE 898-01



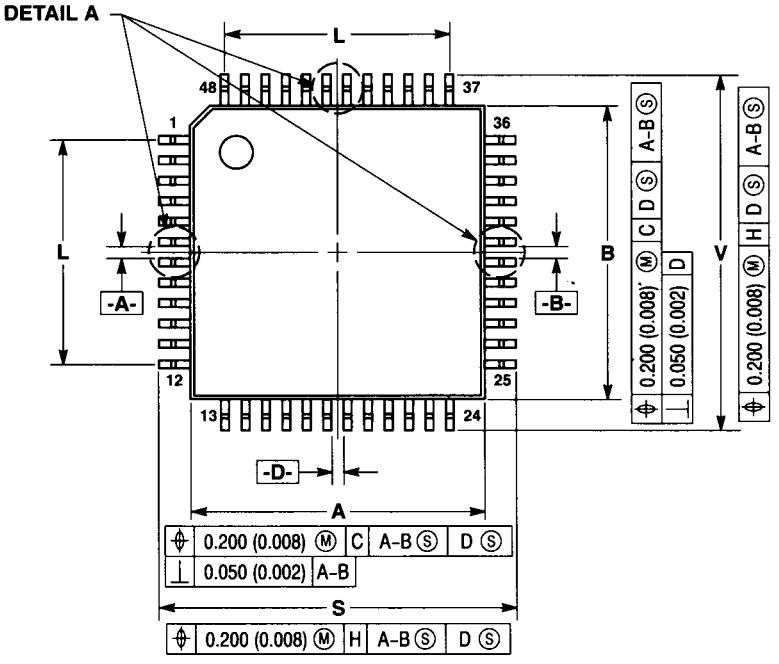
DETAIL A

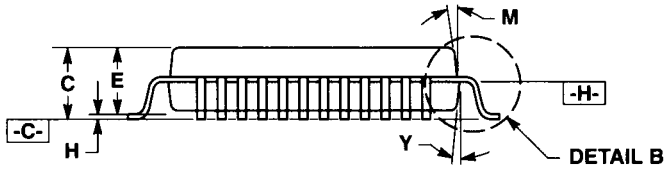


DETAIL B



SECTION B–B
ROTATED 90°





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.48 (0.019).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.90	12.10	0.469	0.476
B	11.90	12.10	0.469	0.476
C	2.05	2.55	0.026	0.041
D	0.20	0.40	0.081	0.100
E	2.00	2.30	0.079	0.091
G	0.80 BASIC		0.031 BASIC	
H	0.00	0.30	0.000	0.011
J	0.10	0.20	0.005	0.008
K	0.65	1.05	0.026	0.041
L	8.80 BASIC		0.346 BASIC	
M	13° REF		13° REF	
P	0.40 BASIC		0.016 BASIC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.006	0.011
S	14.90	15.70	0.587	0.618
V	14.90	15.70	0.587	0.618
W	0.65 REF		0.026 REF	
X	1.60 REF		0.063 REF	
Y	5° REF		5° REF	