

16M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE

REGISTERED TYPE

Description

The MC-4516DA727 is an 16,777,216 words by 72 bits synchronous dynamic RAM module on which 18 pieces of 64M SDRAM : μ PD4564441 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 16,777,216 words by 72 bits organization (ECC type)
- Clock frequency and Access time from CLK.

Part number	/CAS latency	Clock frequency (MAX.)	Access time from CLK (MAX.)
MC-4516DA727-A75	CL = 3	133 MHz	5.4 ns

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- All DQs have $10\ \Omega \pm 10\%$ of series resistor
- Single 3.3 V ± 0.3 V power supply
- LVTTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Registered type
- Serial PD

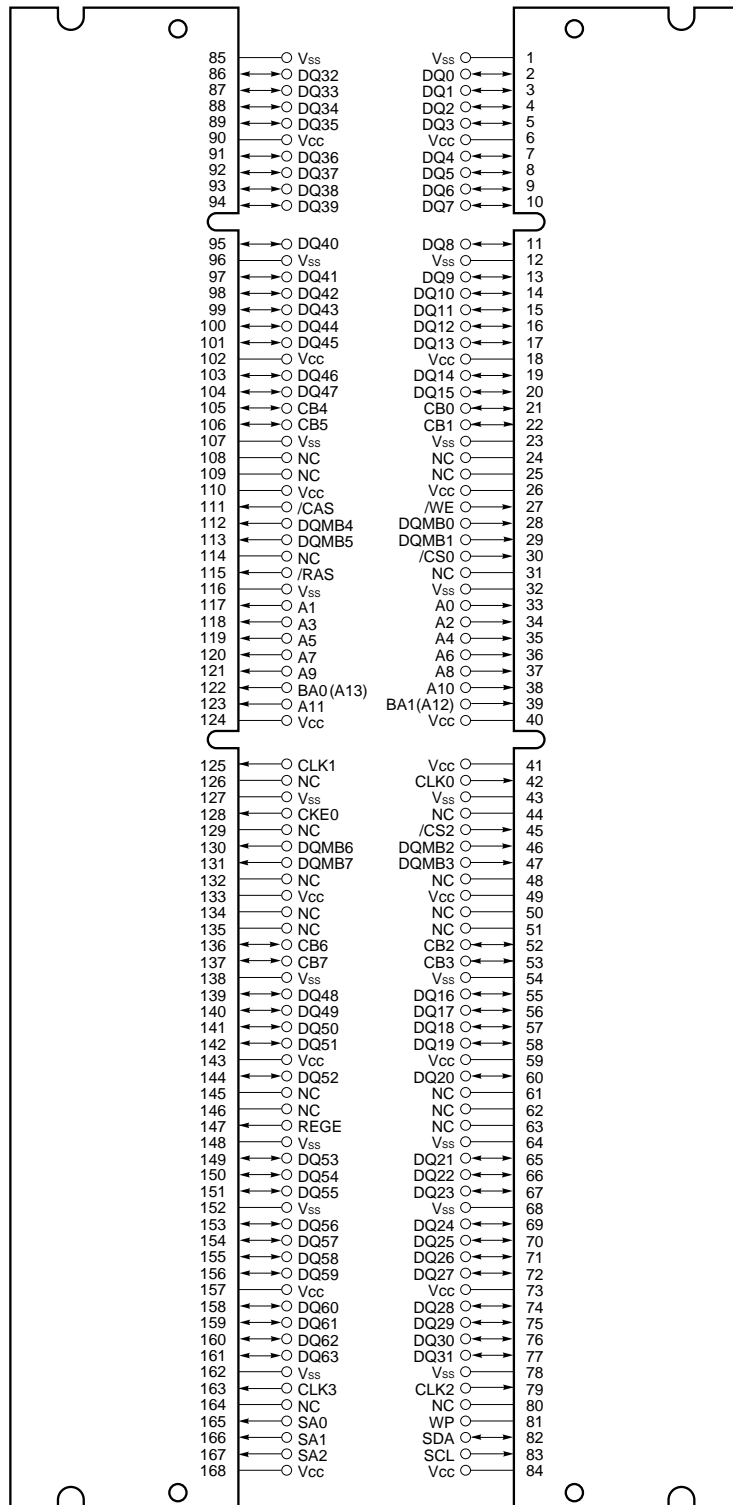
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Ordering Information

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-4516DA727LF-A75	133 MHz	168-pin Dual In-line Memory Module (Socket Type) Edge connector : Gold plated 43.18 mm (1.7 inch) height	18 pieces of μ PD4564441G5 (Revision L) (400 mil TSOP (II))

Pin Configuration

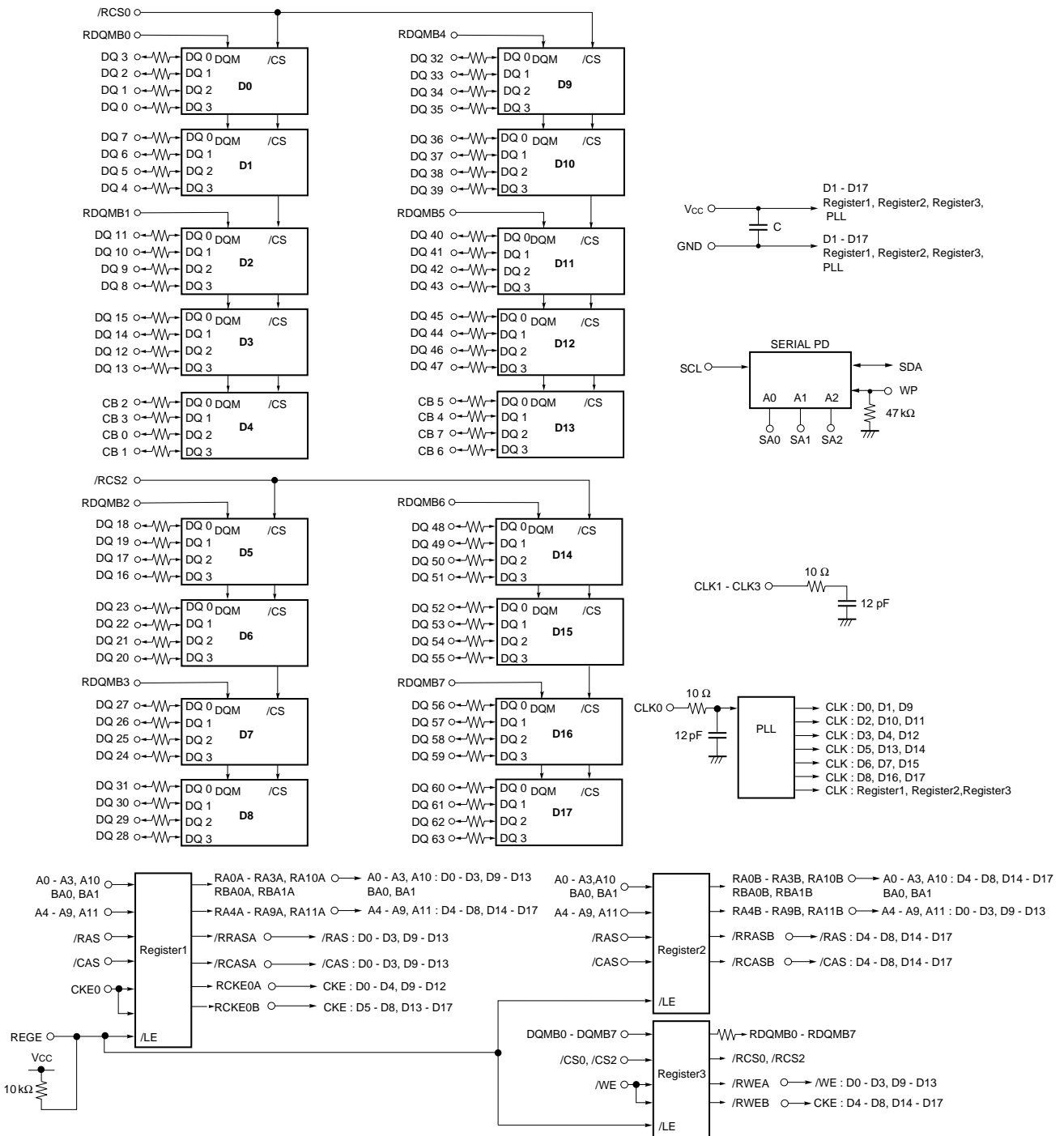
168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plated)



/xxx indicates active low signal.

- A0 - A11 : Address Inputs
- [Row : A0 - A11, Column : A0 - A9]
- BA0 (A13), BA1 (A12) : SDRAM Bank Select
- DQ0-DQ63, CB0-CB7: Data Inputs/Outputs
- CLK0 - CLK3 : Clock Input
- CKE0 : Clock Enable Input
- WP : Write Protect
- /CS0, /CS2 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SA0 - SA2 : Address Input for EEPROM
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- REGE : Register / Buffer Enable
- NC : No Connection

Block Diagram



- Remarks**
1. The value of all resistors of DQs is 10 Ω.
 2. D0 - D17 : μPD4564441(4M words × 4 bits × 4 banks)
 3. REGE ≤ V_{IL} : Buffer mode
REGE ≥ V_{IH} : Register mode
 4. Register : HD74ALVCF162834
PLL : HD74CDCF2510B

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 1 ms and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V _{CC}		-0.5 to +4.6	V
Voltage on input pin relative to GND	V _I		-0.5 to +4.6	V
Short circuit output current	I _O		50	mA
Power dissipation	P _D		21	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		V _{CC} + 0.3	V
Low level input voltage	V _{IL}		-0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE	T.B.D.		T.B.D.	pF
	C _{I2}	CLK0 - CLK3	T.B.D.		T.B.D.	
	C _{I3}	CKE0	T.B.D.		T.B.D.	
	C _{I4}	/CS0, /CS2	T.B.D.		T.B.D.	
	C _{I5}	DQMB0 - DQMB7	T.B.D.		T.B.D.	
Data input/output capacitance	C _{I/O}	DQ0 - DQ63, CB0 - CB7	T.B.D.		T.B.D.	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

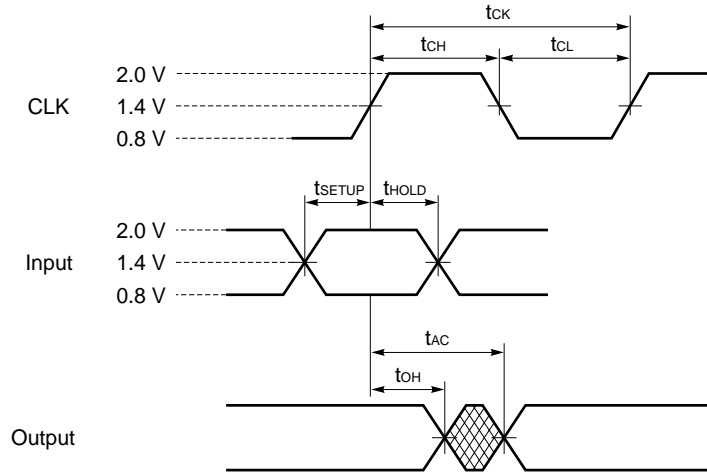
Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	Burst length = 1, t _{RC} ≥ t _{RC(MIN.)} , I _O = 0 mA		1,930	mA	1
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns		268	mA	
	I _{CC2PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞		85		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.		610	mA	
	I _{CC2NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.		188		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns		340	mA	
	I _{CC3PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞		132		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.		700	mA	
	I _{CC3NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.		350		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} , I _O = 0 mA		2,470	mA	2
CBR (Auto) refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN.)}		2,920	mA	3
Self refresh current	I _{CC6}	CKE ≤ 0.2 V, t _{CK} = 15 ns		268	mA	
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V	-20	+20	μA	
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V	-1.5	+1.5	μA	
High level output voltage	V _{OH}	I _O = -4.0 mA	2.4		V	
Low level output voltage	V _{OL}	I _O = +4.0 mA		0.4	V	

- Notes**
1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 3. I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

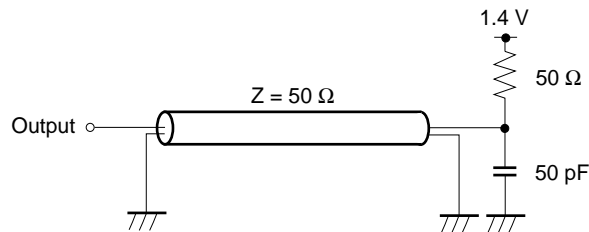
- AC measurements assume $t_r = 1$ ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL} .
- If t_r is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics (Registered Mode)

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
Clock cycle time	t _{CK}	7.5	(133 MHz)	ns	
Access time from CLK	t _{AC}		5.4	ns	1
Input clock frequency		50	133	MHz	
Input CLK duty cycle		45	55	%	
Data-out hold time	t _{OH}	2.7		ns	1
Data-out low-impedance time	t _{LZ}	0		ns	
Data-out high- impedance time	t _{HZ}	3	6	ns	
Data-in setup time	t _{DS}	1.5		ns	
Data-in hold time	t _{DH}	0.8		ns	
Address setup time	t _{AS}	1.5		ns	
Address hold time	t _{AH}	0.8		ns	
CKE setup time	t _{CKS}	1.5		ns	
CKE hold time	t _{CKH}	0.8		ns	
CKE setup time (Power down exit)	t _{CKSP}	1.5		ns	
Command (/CS0 - /CS3, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time	t _{CMS}	1.5		ns	
Command (/CS0 - /CS3, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time	t _{CMH}	0.8		ns	

Note 1. Output load



Remark These specifications are applied to the monolithic device.

Asynchronous Characteristics (Registered Mode)

Parameter	Symbol	-A75		Unit	Note
		MIN.	MAX.		
REF to REF/ACT command period	t _{RC}	9		CLK	
ACT to PRE command period	t _{RAS}	6	16,000	CLK	
PRE to ACT command period	t _{RP}	3		CLK	
Delay time ACT to READ/WRITE command	t _{RCD}	3		CLK	
ACT(0) to ACT(1) command period	t _{RRD}	2		CLK	
Data-in to PRE command period	t _{DPL}	1		CLK	
Data-in to ACT(REF) command period(Auto precharge)	t _{DAL}	20		ns	
Mode register set cycle time	t _{RSC}	2		CLK	
Transition time	t _T	0.5	30	ns	
Refresh time (4,096 refresh cycles)	t _{REF}		64	ms	

Serial PD

(1/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM	
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows	
4	Number of columns	0AH	0	0	0	0	1	0	1	0	10 columns	
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank	
6	Data width	48H	0	1	0	0	1	0	0	0	72 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTTL	
9	CL = 3 Cycle time	-A75	75H	0	1	1	1	0	1	1	0	7.5 ns
10	CL = 3 Access time	-A75	54H	0	1	0	1	0	1	0	0	5.4 ns
11	DIMM configuration type	02H	0	0	0	0	0	0	0	1	0	ECC
12	Refresh rate/type	80H	1	0	0	0	0	0	0	0	0	Normal
13	SDRAM width	04H	0	0	0	0	0	0	1	0	0	×4
14	Error checking SDRAM width	04H	0	0	0	0	0	0	1	0	0	×4
15	Minimum clock delay	01H	0	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM	04H	0	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported	04H	0	0	0	0	0	0	1	0	0	3
19	/CS latency supported	01H	0	0	0	0	0	0	0	0	1	0
20	/WE latency supported	01H	0	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes	1FH	0	0	0	1	1	1	1	1	1	Registered
22	SDRAM device attributes : General	0EH	0	0	0	0	1	1	1	0		
23-26		00H	0	0	0	0	0	0	0	0		
27	t _{RP} (MIN.)	-A75	17H	0	0	0	1	0	1	1	1	23 ns(22.5ns)
28	t _{RRD} (MIN.)	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
29	t _{RCD} (MIN.)	-A75	17H	0	0	0	1	0	1	1	1	23 ns(22.5ns)
30	t _{RAS} (MIN.)	-A75	2DH	0	0	1	0	1	1	0	1	45 ns
31	Module bank density	20H	0	0	1	0	0	0	0	0	0	128M bytes

(2/2)

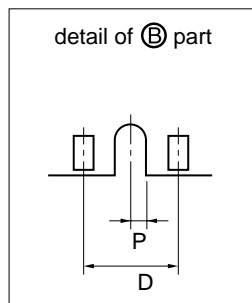
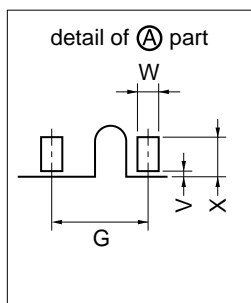
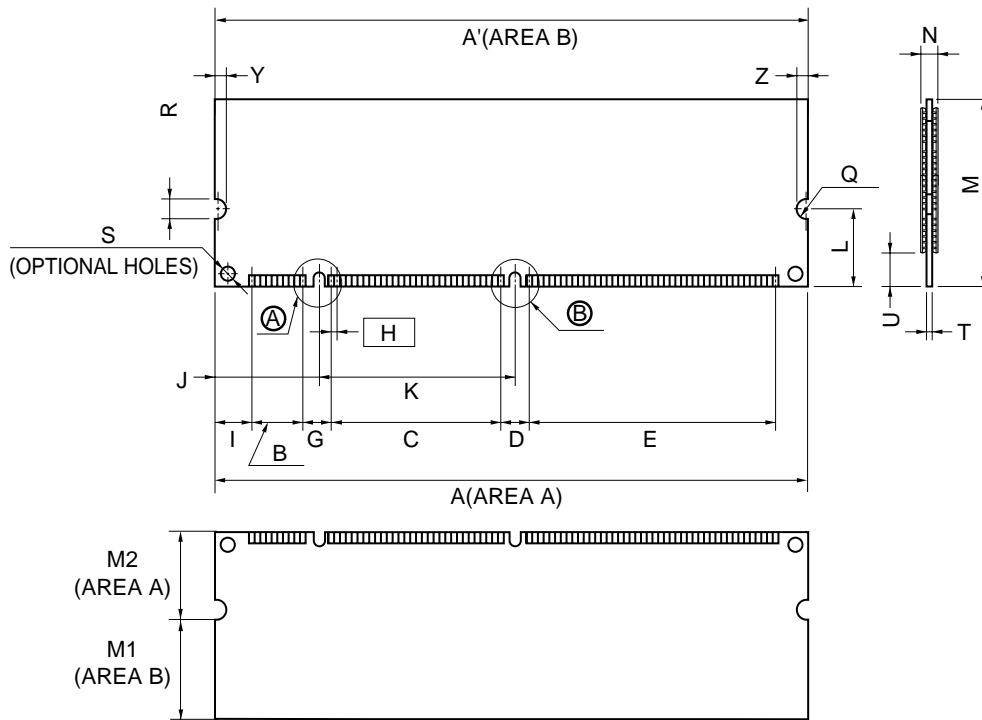
Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32	Command and address signal input setup time	15H	0	0	0	1	0	1	0	1	1.5 ns
33	Command and address signal input hold time	08H	0	0	0	0	1	0	0	0	0.8 ns
34	Data signal input setup time	15H	0	0	0	1	0	1	0	1	1.5 ns
35	Data signal input hold time	08H	0	0	0	0	1	0	0	0	0.8 ns
36-61		00H	0	0	0	0	0	0	0	0	
62	SPD revision	02H	0	0	0	0	0	0	1	0	JEDEC 2
63	Checksum for bytes 0 - 62	-A75	CCH	1	1	0	0	1	1	0	0
64-71	Manufacture's JEDEC ID code										
72	Manufacturing location										
73-90	Manufacture's P/N										
91	Revision Code										
93-94	Manufacturing date										
95-98	Assembly serial number										
99-125	Mfg specific										
126	Intel specification frequency	64H	0	1	1	0	0	1	0	0	100 MHz
127	Intel specification /CAS latency support	-A75	85H	1	0	0	0	0	1	0	1

Timing Chart

Refer to the SYNCHRONOUS DRAM MODULE TIMING CHART Information (M13348X).

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS
A	133.35±0.13
A'	133.35
B	11.43
B'	73.406
C	36.83
C'	29.972
D	6.35
E	54.61
G	6.35
H	1.27 (T.P.)
I	8.89
J	24.495
K	42.18
L	17.78
M	43.18
M1	23.4
M2	19.78
N	4.0 MAX.
P	1.0
Q	R2.0
R	4.0±0.1
S	∅3.0
T	1.27±0.1
U	4.0 MIN.
V	0.2±0.15
W	1.0±0.05
X	2.54 MIN.
Y	3.0 MIN.
Z	3.0 MIN.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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