

DATA SHEET

AS227-000LF/099LF: 20 MHz-2.0 GHz, 4 W pHEMT SP3T Switch

Applications

- Transmit/receive switching for telematic systems at elevated power levels

Features

- Broadband frequency range: 20 MHz to 2.0 GHz
- Very low insertion loss, 0.5 dB typical @ 0.9 GHz
- High isolation: 26 dB typical @ 0.9 GHz
- High input power compression: 0.1 dB @ > +37 dBm
- Low current consumption: <50 μ A @ 3 V
- Bare pHEMT die: 1015 x 1015 x 200 μ m
- Chips supplied on Gel-Pak® or singulated wafers on film frame



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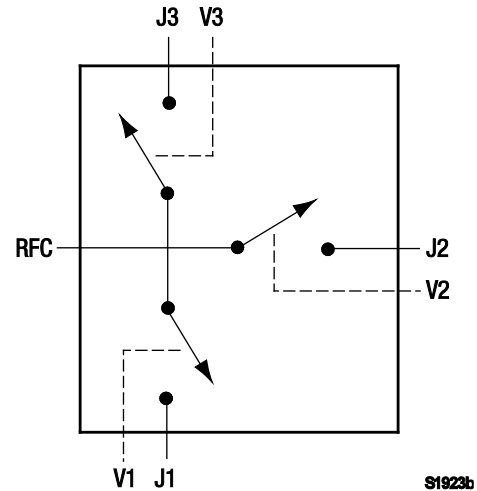


Figure 1. AS227-000LF Block Diagram

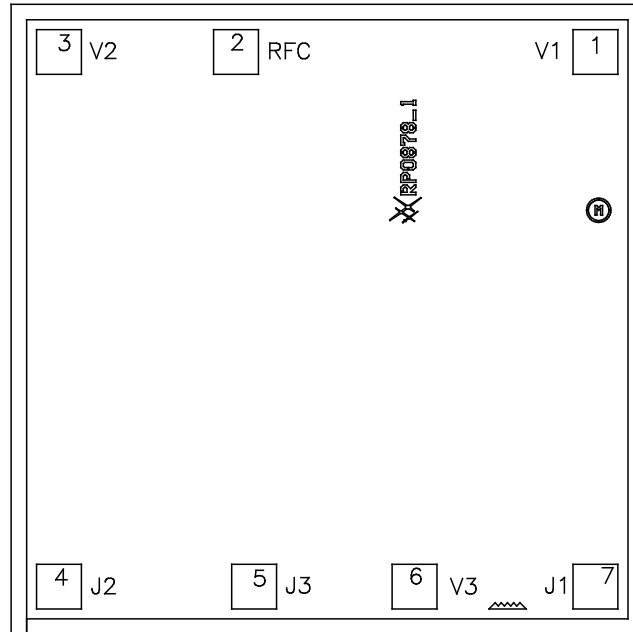
Description

The AS227-000LF/099LF is a high power, pHEMT Single Pole Triple Throw (SP3T) switch. The switch is designed for use in systems operating from 20 MHz to 2.0 GHz for which low loss, high isolation, low control voltage, and chip scale size are required.

The device is controlled with positive, negative, or a combination of both voltages. The RF signal paths within the device are fully bilateral.

The AS227-000LF/099LF is provided as a bare die in an ultra-compact 1015 x 1015 x 200 μ m design. Chips are shipped in quantities of 100 per 2 x 2 inch Gel-Pak (use part number AS227-000LF). For high volume orders, chips can be supplied on a film frame (use part number AS227-099LF).

A functional block diagram is shown in Figure 1. The pin configuration is shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.



Note: Pin 8 is the backside of chip and should be grounded.

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Figure 2. AS227-000LF/099LF Pinout (Top View)

Table 1. AS227-000LF/099LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	V1	DC control voltage.	5	J3	RF port. Must be DC blocked for positive voltage operation (Note 1).
2	RFC	RF common port. Must be DC blocked for positive voltage operation (Note 1).	6	V3	DC control voltage.
3	V2	DC control voltage	7	J1	RF port. Must be DC blocked for positive voltage operation (Note 1).
4	J2	RF port. Must be DC blocked for positive voltage operation (Note 1).	8	GND	Ground. Backside of chip. Mount with conductive epoxy.

Note 1: A 47 pF blocking capacitor is required for >500 MHz operation. Use larger value capacitors for lower frequency operation.

Technical Description

The AS227-000LF/099LF is controlled using three voltage inputs, V1, V2, and V3 (pins 1, 3, and 6, respectively). Depending on the voltage level applied to these pins, the common RF port (RFC) is connected to one of three RF ports (J1, J2, or J3) using a low insertion loss path, while the path between RFC and the other RF ports are in an isolation state.

When the control voltages are toggled, the states between RFC and the other RF ports are also toggled.

Electrical and Mechanical Specifications

The absolute maximum ratings of the AS227-000LF/099LF are provided in Table 2. Electrical specifications are provided in Table 3 and the operating characteristics are specified in Table 4.

Typical performance characteristics of the AS227-000LF/099LF are illustrated in Figures 3 through 7.

The state of the AS227-000LF is determined by the logic provided in Table 5.

Table 2. AS227-000LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Control voltage	V _{CTL}	0	+6	V
RF input power (V _{CTL} > 0.9 GHz)	P _{IN}		+36	dBm
Operating temperature	T _{OP}	-40	+85	°C
Storage temperature	T _{STG}	-65	+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 3. AS227-000LF/099LF Electrical Specifications (Note 1)
(V_{CTL} = 0-3 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Insertion loss		0.02 to 0.5 GHz		0.45	0.60	dB
		0.5 to 1.0 GHz		0.50	0.70	dB
		1.0 to 2.0 GHz		0.70	0.90	dB
Isolation		0.02 to 0.5 GHz	30	32		dB
		0.5 to 1.0 GHz	24	26		dB
		1.0 to 2.0 GHz	18	20		dB
Return loss (Note 2)		0.02 to 1.0 GHz		18		dB
		1.0 to 2.0 GHz		14		dB
Switching characteristics: Rise/fall On/off		10/90% or 90/10% RF		200		ns
		50% V _{CTL} to 90/10% RF		300		ns
0.1 dB Input Compression Point	IPO.1dB	@ 48 MHz		+35		dBm
		@ 900 MHz		+38		dBm
Control voltage: Low (@ 20 μA max) High (@100 μA max) High (@ 200 μA max)	V _{CTL_L}		0			V
	V _{CTL_H}				2.7	V
	V _{CTL_H}				5.0	V

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Return loss state. Lower frequency return loss is dependent on value of the DC blocking capacitors.

Typical Performance Characteristics

($V_{CTL} = 0-3\text{ V}$, $T_{OP} = +25\text{ }^\circ\text{C}$, $P_{IN} = 0\text{ dBm}$, Characteristic Impedance [Z_0] = $50\ \Omega$, $C_{BL} = 100\text{ pF}$, Unless Otherwise Noted)

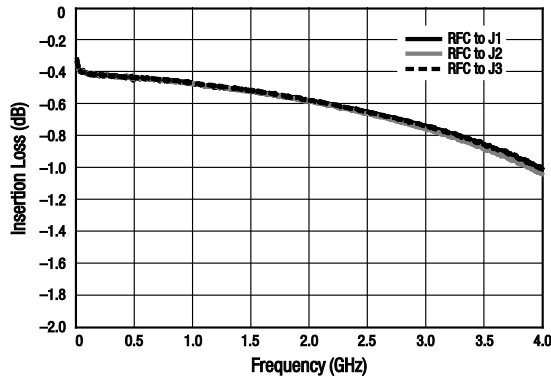


Figure 3. Insertion Loss vs Frequency

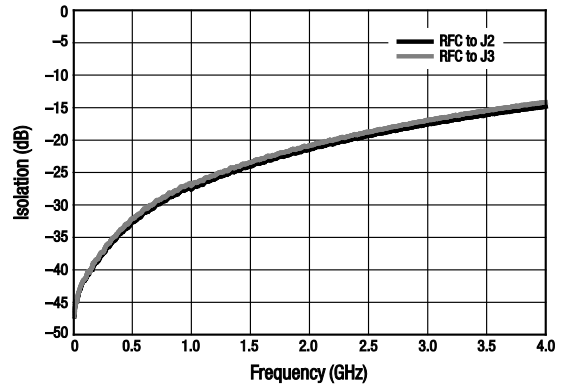


Figure 4. Isolation vs Frequency (RFC to J1 in Insertion Loss)

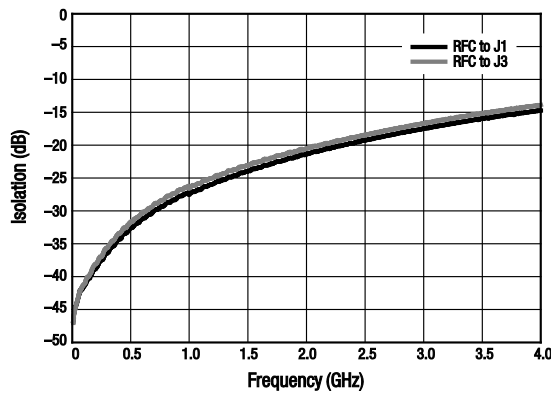


Figure 5. Isolation vs Frequency (RFC to J2 in Insertion Loss)

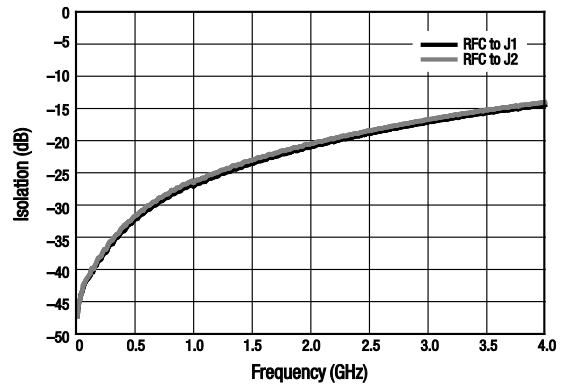


Figure 6. Isolation vs Frequency (RFC to J3 in Insertion Loss)

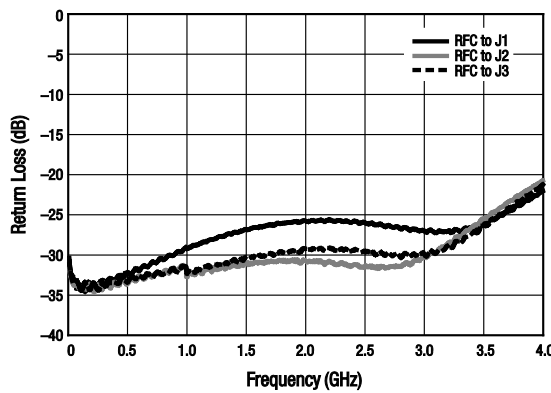


Figure 7. Return Loss vs Frequency (Insertion Loss State)

Table 4. Truth Table

V1 (Pin 1)	V2 (Pin 3)	V3 (Pin 6)	RFC to J1 Path	RFC to J2 Path	RFC to J3 Path
V _{HIGH}	V _{LOW}	V _{LOW}	Insertion Loss	Isolation	Isolation
V _{LOW}	V _{HIGH}	V _{LOW}	Isolation	Insertion Loss	Isolation
V _{LOW}	V _{LOW}	V _{HIGH}	Isolation	Isolation	Insertion Loss

Note: V_{LOW} = 0 to 0.2 V, V_{HIGH} = 2.7 to 5 V. Any state other than described in this Table places the device in an undefined state. An undefined state does not damage the device.

Evaluation Board Description

The AS227-000LF/099LF is evaluated in a plastic package format to determine its performance characteristics. An Evaluation Board schematic diagram is provided in Figure 8. An assembly drawing for the Evaluation Board is shown in Figure 9.

Chip Dimensions

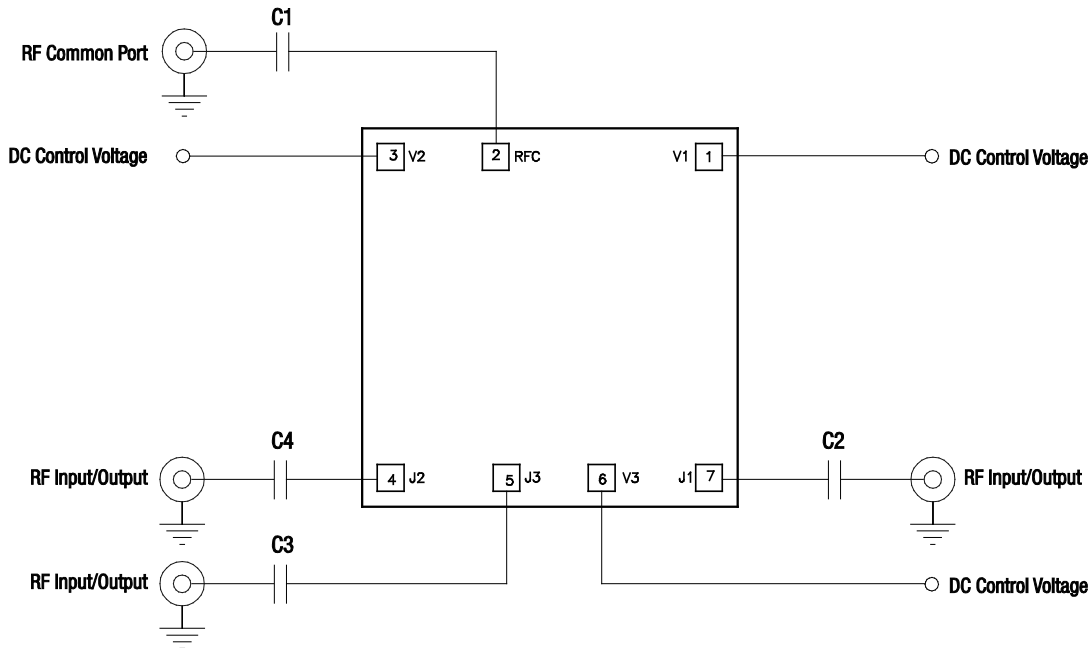
Chip dimensions are shown in Figure 10.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The AS227-000LF chips are shipped in Gel-Paks. The AS227-099LF wafers are shipped on film frames (see singulated wafer format dimensions in Figure 11).

The AS227-000LF/099LF has no backside metal and must be attached using conductive epoxy.



Note: Use 47 pF blocking capacitors (C1, C2, C3, C4) for >500 MHz operation. Higher values recommended for lower frequency operation. Exposed paddle must be grounded.

Use 10 nF blocking capacitors (C1, C2, C3, C4) for <50 MHz operation.

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Figure 7. AS227-000LF/099LF Evaluation Board Schematic

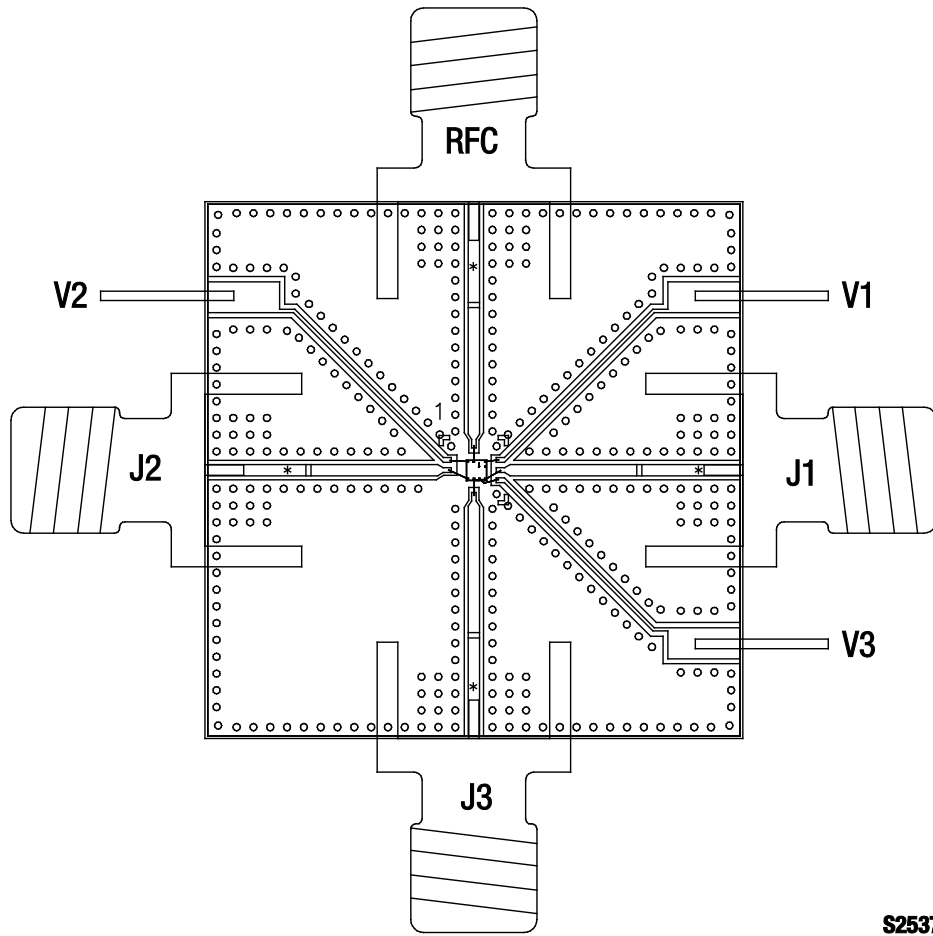
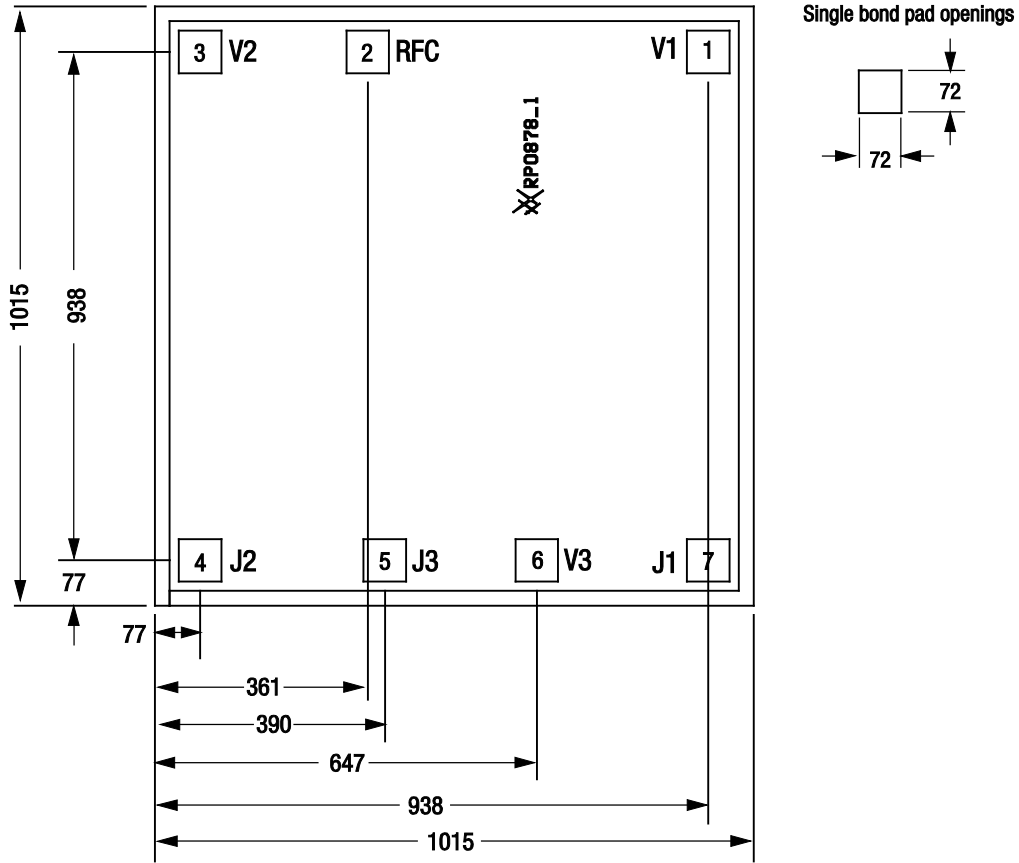


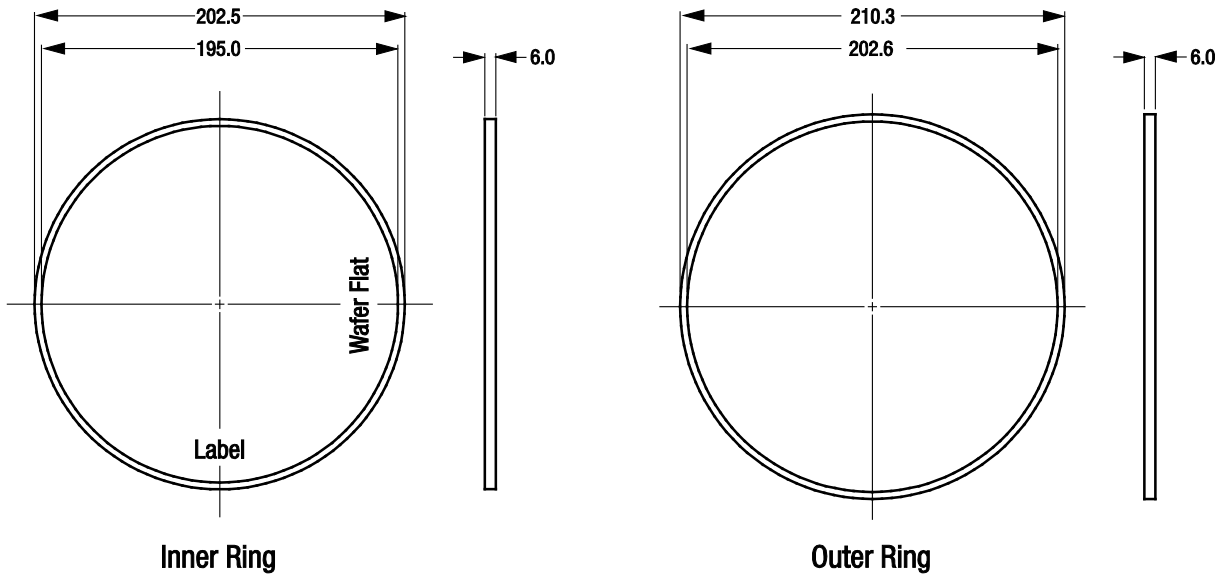
Figure 8. AS227-000LF/099LF Evaluation Board Assembly Diagram



Notes: All dimensions are in microns.
 Pin 8 is ground pad on backside of chip.
 Bond pads are gold metalized.
 Chip backside metalization: none.
 Chip thickness: 200 microns

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Figure 9. AS227-000LF/099LF Chip Dimensions



Grip Ring Number: GRP-2620-6

- Notes:
1. All dimensions in millimeters.
2. Tape material: unexposed UV tape.

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Figure 10. AS227-099LF (Singulated Wafer Format)

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
AS227 SPDT Switch	AS227-000LF (100 chips per 2 x 2 inch Gel-Pak)	AS227-000LF-EVB
	AS227-099LF (singulated wafers on film frame)	

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