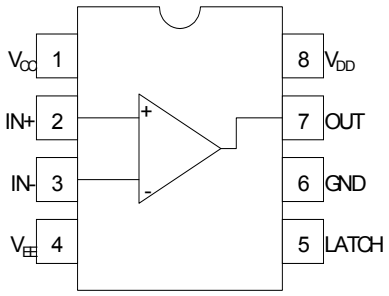
903
High Speed Comparator



FEATURES:

- High-speed, low-power voltage comparator
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness: 100 krad (Si) typical; dependent upon orbit
- 8ns typ propagation delay
- 18mW power consumption (typ at +5V)
- Separate analog and digital supplies
- Flexible analog supply: +5V to +10V or ±5V
- Input range includes negative supply rail
- TTL compatible outputs
- TTL compatible latch inputs

DESCRIPTION:

DDC's 903 high-speed, low-power voltage comparator features differential analog inputs and TTL logic outputs with active internal pull-ups. The 903 can be powered from separate analog and digital power supplies or from a single combined supple voltage. The analog input common-mode range includes the negative rail, allowing ground sensing when powered from a single supply. When powered from +5V, the 903 consumes 18mW. The 903 is equipped with a TTL compatible latch input. The comparator output is latched when the latch input is driven low. Capable of surviving space environments, the 903 is ideal for satellite, spacecraft, and space probe missions. DDC's patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit or space mission. In GEO orbit, RAD-PAK® provides greater than 100 krad(Si) radiation dose rate. This product is available with screening up to Class S.

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TABLE 1. PINOUT DESCRIPTION

PIN	NAME	FUNCTION
1	V_{CC}	Positive Analog Supply
2	IN+	Positive input
3	IN-	Negative input
4	V_{EE}	Negative analog supply and substrate
5	LATCH	Latch input
6	GND	Ground terminal
7	OUT	Output
8	V_{DD}	Positive digital supply

TABLE 2. ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
Analog Supply Voltage (V_{CC} to V_{EE})	--	+12	V
Digital Supply Voltage (V_{DD} to GND)	--	+7	V
Differential Input Voltage	V_{EE} - 0.2	V_{CC} + 0.2	V
Common-mode Input Voltage	V_{EE} - 0.2	V_{CC} + 0.2	V
Latch Input Voltage	-0.2	V_{DD} + 0.2	V
Output Short-circuit Duration to GND	Indefinite		
Output Short-circuit Duration to V_{DD}	--	1	min.
Operating Temperature Ranges	-55	+125	°C
Junction Temperature (Tj)	-65	+160	°C
Storage Temperature Range	-65	+150	°C

TABLE 3. AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, LATCH = LOGIC HIGH, T_A = T_{MIN} TO T_{MAX}, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNITS
Input-to-output High Response Time	tpd+	VOD = 5mV, CL = 15pF, IO = 2mA[1]	9, 10, 11	--	10	15	ns
Input-to-output Low Response Time	tpd-	VOD = 5mV, CL = 15pF, IO = 2mA[1]	9, 10, 11	--	10	15	ns

TABLE 3. AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, LATCH = LOGIC HIGH, T_A = T_{MIN} TO T_{MAX}, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNITS
Latch Disable to Output High Delay	tpd+	[2]	9, 10, 11		10		ns
Latch Disable to Output Low Delay	tpd-	[2]	9, 10, 11		12		ns
Minimum Setup Time	ts	[2]	9, 10, 11		2		ns
Minimum Hold Time	th	[2]	9, 10, 11		1		ns
Minimum Latch Disable Pulse Width	tpw	[2]	9, 10, 11		10		ns

1. Guaranteed by design.

2. Owing to the difficult and critical nature of switching measurements involving the latch, these parameters cannot be tested in a production environment. Typical specifications listed are taken from measurements using a high-speed test fixture.

TABLE 4. DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, LATCH = LOGIC HIGH, T_A = T_{MIN} TO T_{MAX} UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = 0V, V_O = 1.4V	1, 2, 3	--	2	6	mV
Input Bias Current	I_B	I_{IN+} or I_{IN-}	1, 2, 3	--	6	15	µA
Input Offset Current	I_{OS}	V_{CM} = 0V, V_O = 1.4V	1, 2, 3	--	200	800	nA
Input Voltage Range	V_{CM}	[1]	1, 2, 3	V_{EE} - 0.1	--	V_{CC} - 2.25	V
Common-mode Rejection Ratio	CMRR	-5V < V_{CM} < +2.75, V_O = 1.4V,[2]	1, 2, 3	--	120	500	µV/V
Power-supply Rejection Ratio	PSRR	[2]	1, 2, 3	--	150	500	µV/V
Output High Voltage	V_{OH}	V_{IN} > 250mV, I_{SRC} = 1mA	1, 2, 3	2.4	3.5	--	V
Output Low Voltage	V_{OL}	V_{IN} > 250mV, I_{SINK} = 8mA	1, 2, 3	--	0.3	0.4	V
Latch Input Voltage High	V_{LH}		1, 2, 3	--	1.4	2.0	V
Latch Input Voltage Low	V_{LL}		1, 2, 3	0.8	1.4	--	V
Latch Input Current High	I_{LH}	V_{LH} = 3.0V	1, 2, 3	--	1	20	µA
Latch Input Current Low	I_{LL}	V_{LL} = 0.3V	1, 2, 3	--	1	20	µA

TABLE 4. DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, LATCH = LOGIC HIGH, T_A = T_{MIN} TO T_{MAX} UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNITS
Positive Analog Supply Current	I_{CC}		1, 2, 3	--	2.5	6	mA
Negative Analog Supply Current	I_{EE}		1, 2, 3	--	2	5	mA
Digital Supply Current	I_{DD}		1, 2, 3	--	1	2.5	mA
Power Dissipation	P_D	V_{CC} = V_{DD} = +5V, V_{EE} = 0V	1, 2, 3	--	18	28	mW

1. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.2V below V_{EE}. The upper end of the common-mode voltage range is typically V_{CC} -0.2V, but either or both inputs can go to a maximum of V_{CC} +0.2V without damage.
2. Tested for +4.75V<V_{CC}<+5.25V, and -5.25V<V_{EE}<-4.75V with V_{DD} = +5V, although permissible analog power-supply range is +4.75V<V_{CC}<+10.5V for single-supply operation with V_{EE} grounded.

FIGURE 1. INPUT OFFSET VOLTAGE VS. TEMPERATURE

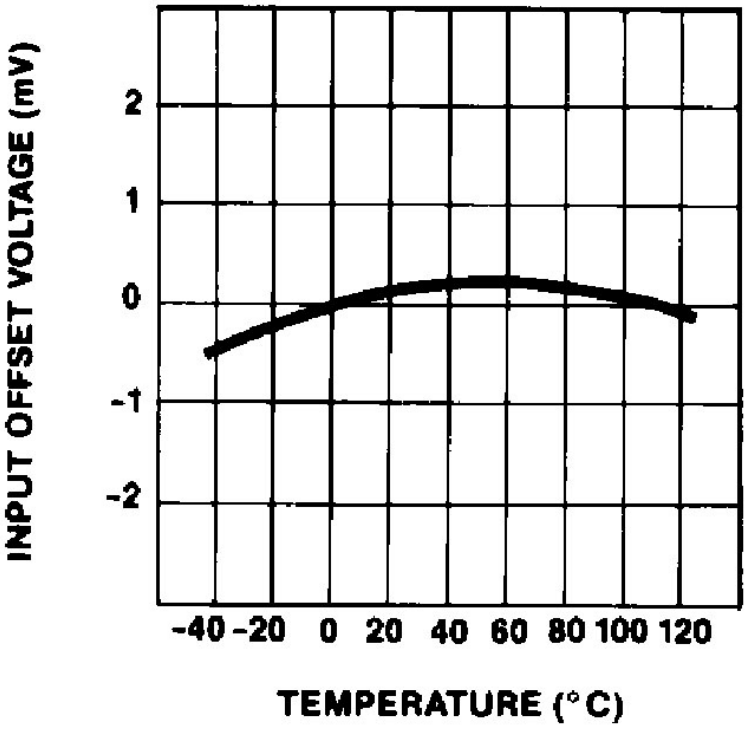


FIGURE 2. INPUT BIAS CURRENT VS. TEMPERATURE

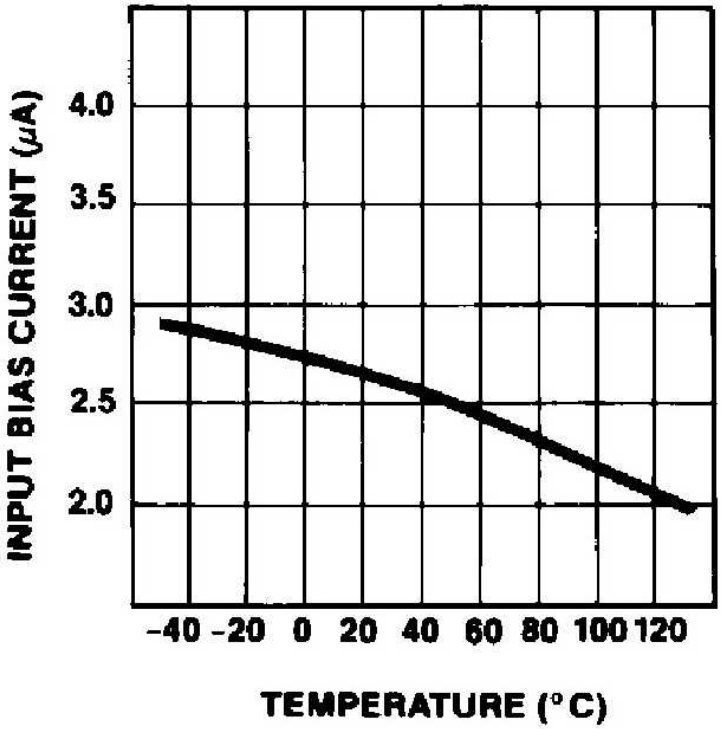


FIGURE 3. OUTPUT LOW VOLTAGE (V_{OL}) VS. LOAD CURRENT

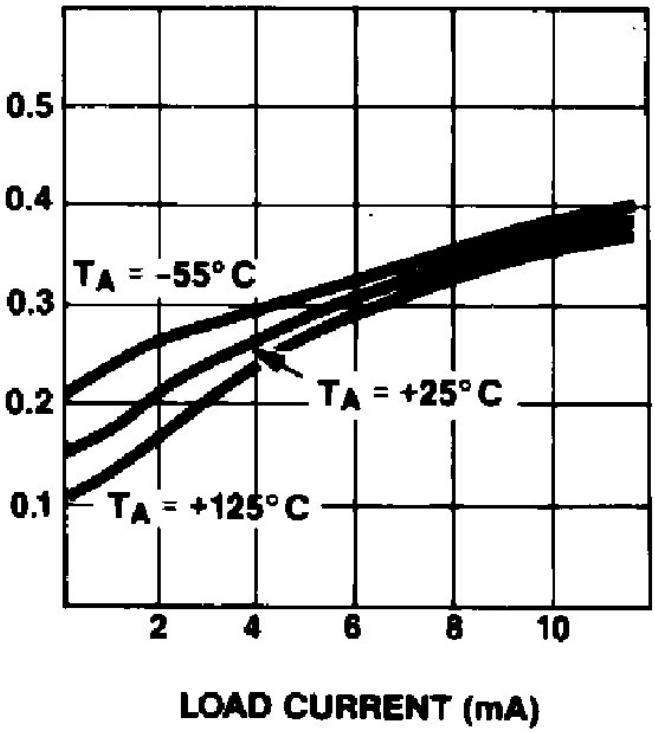


FIGURE 4. I_{CC} SUPPLY CURRENT (PER COMPARATOR) VS. V_{CC} SUPPLY VOLTAGE (V_{DD} = +5V)

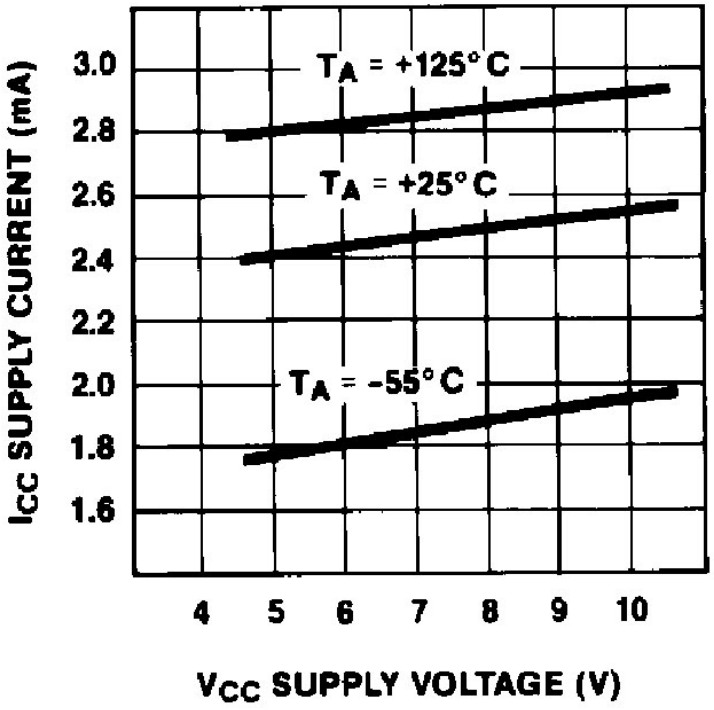


FIGURE 5. INPUT OVERDRIVE VS. tpd+ RESPONSE TIME

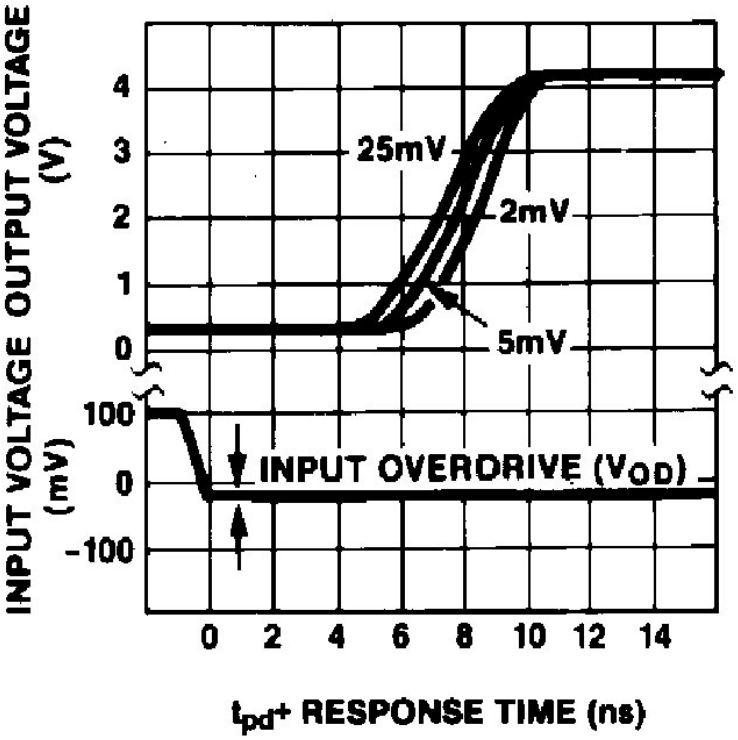


FIGURE 6. INPUT OVERDRIVE VS. tpd- RESPONSE TIME

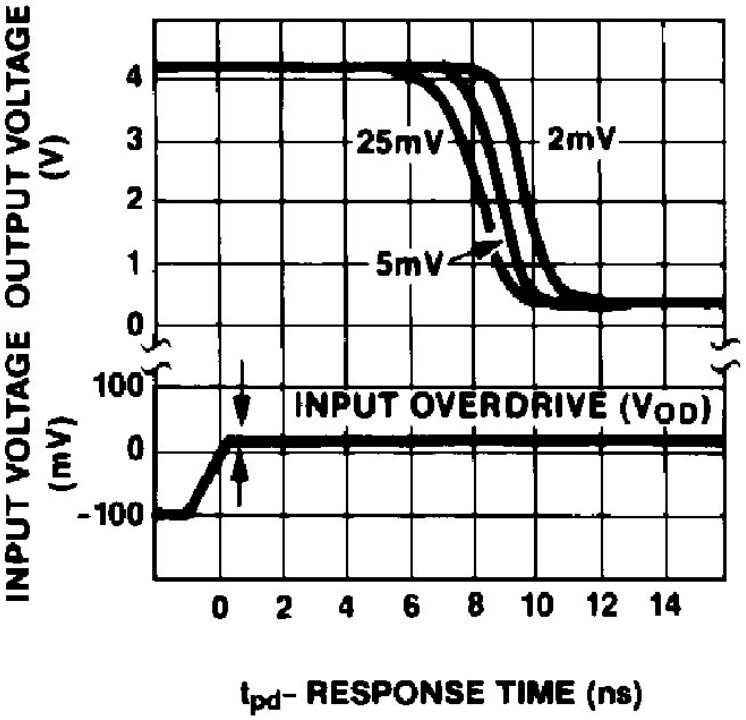


FIGURE 7. RESPONSE TIME VS. TEMPERATURE (5MV OVERDRIVE)

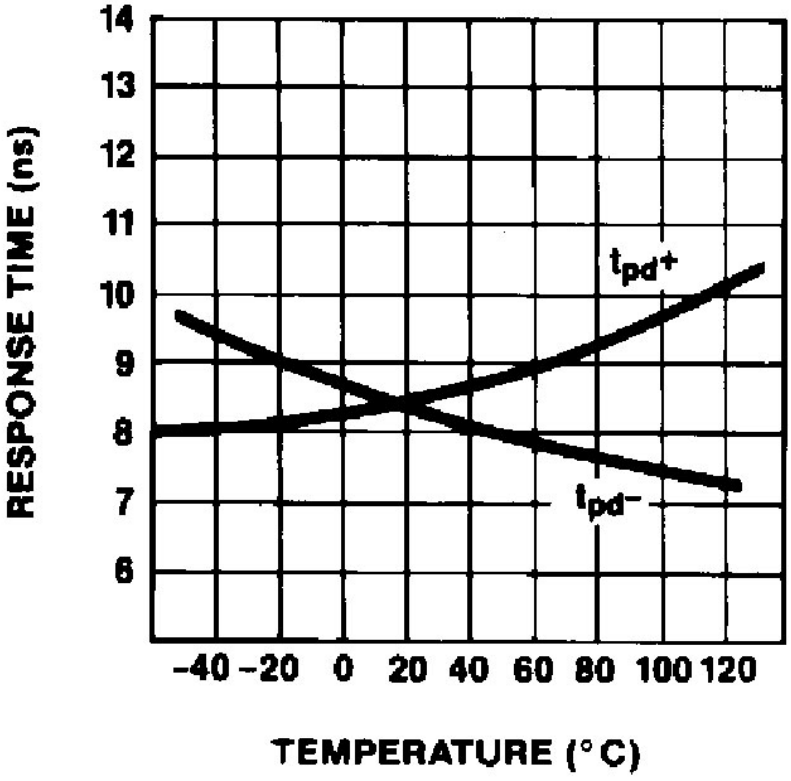


FIGURE 8. RESPONSE TIME VS. LOAD CAPACITANCE
(5MV OVERDRIVE, RLOAD = 2.4KΩ)

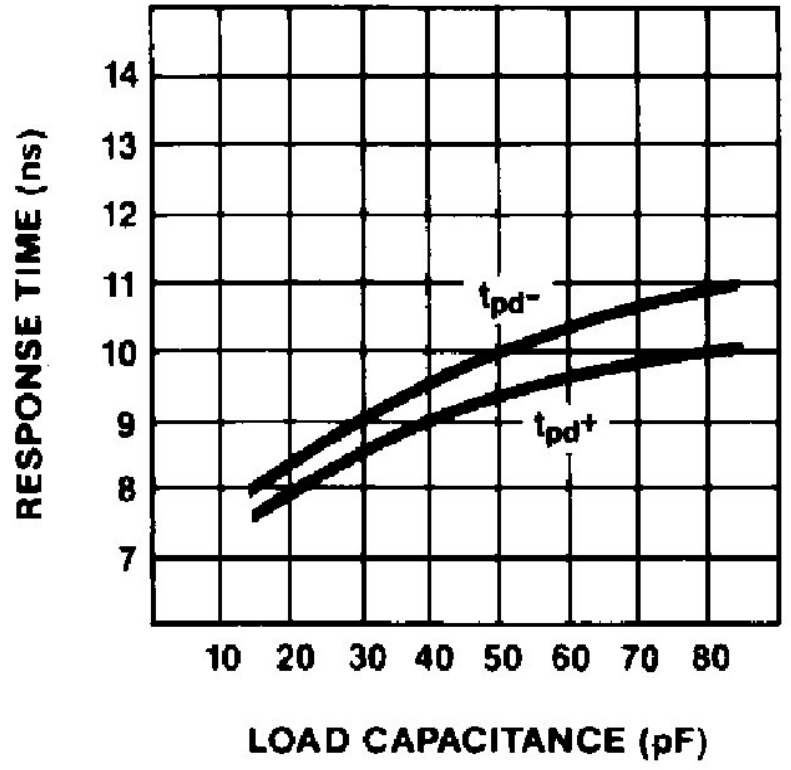


FIGURE 9. TIMING DIAGRAM

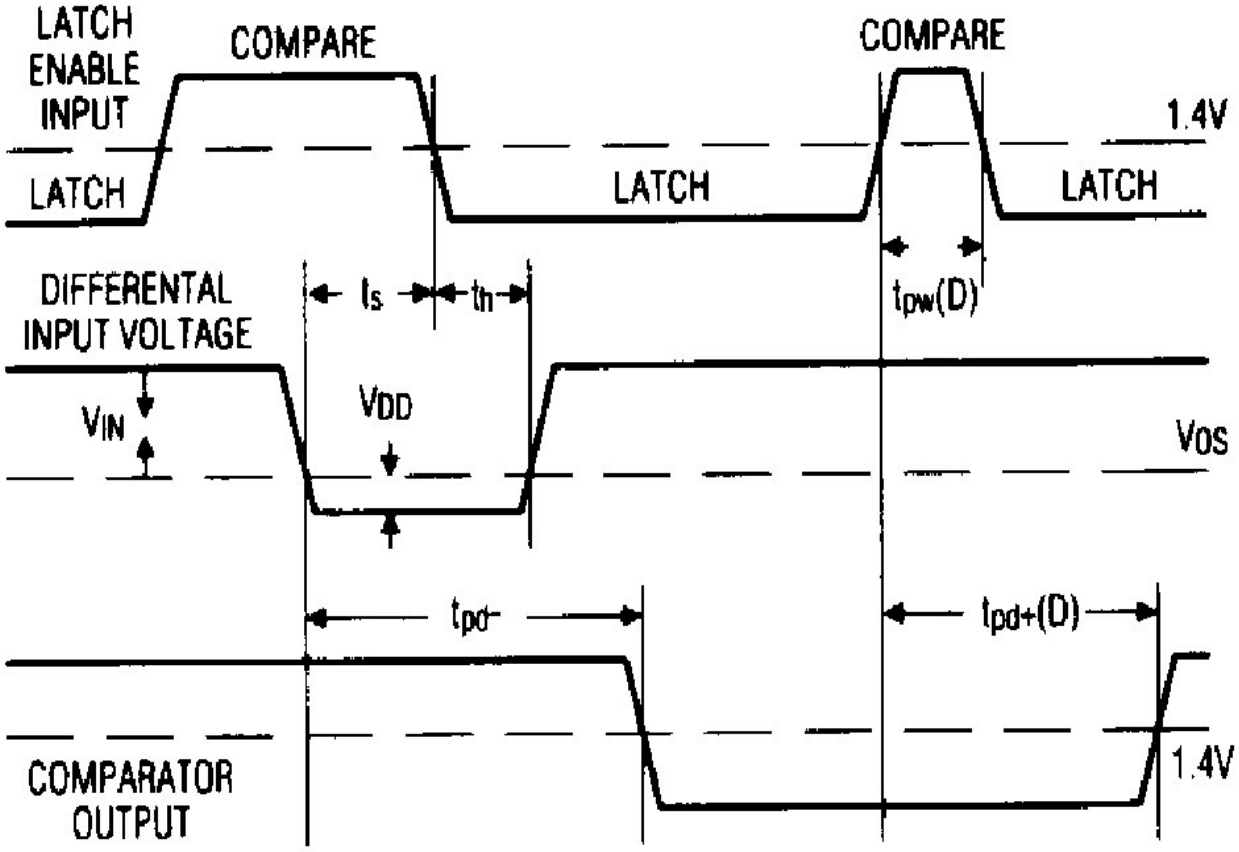


FIGURE 10. t_{pd+} RESPONSE TIME TO 5mV OVERDRIVE

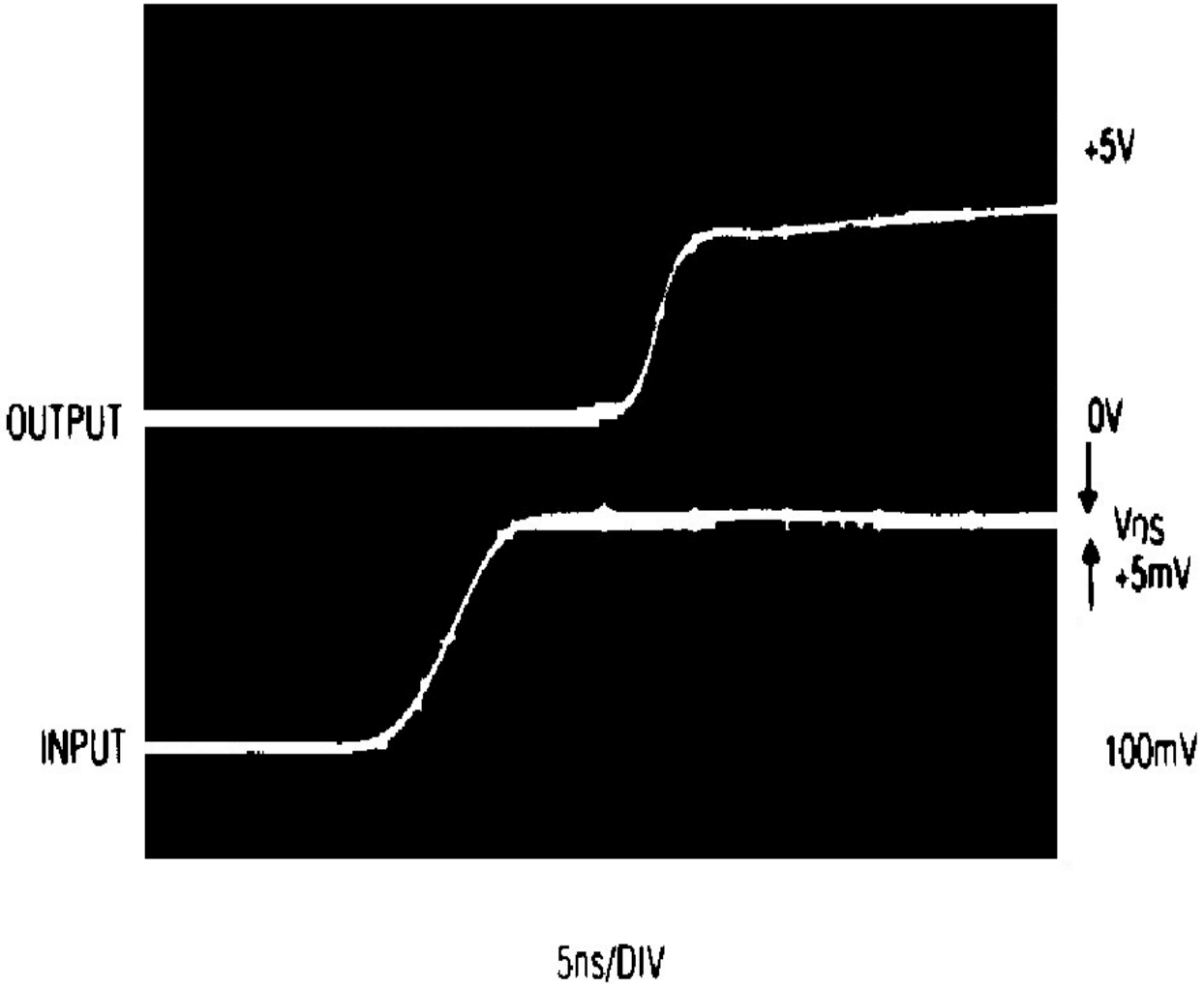


FIGURE 11. tpd- RESPONSE TIME TO 5mV O

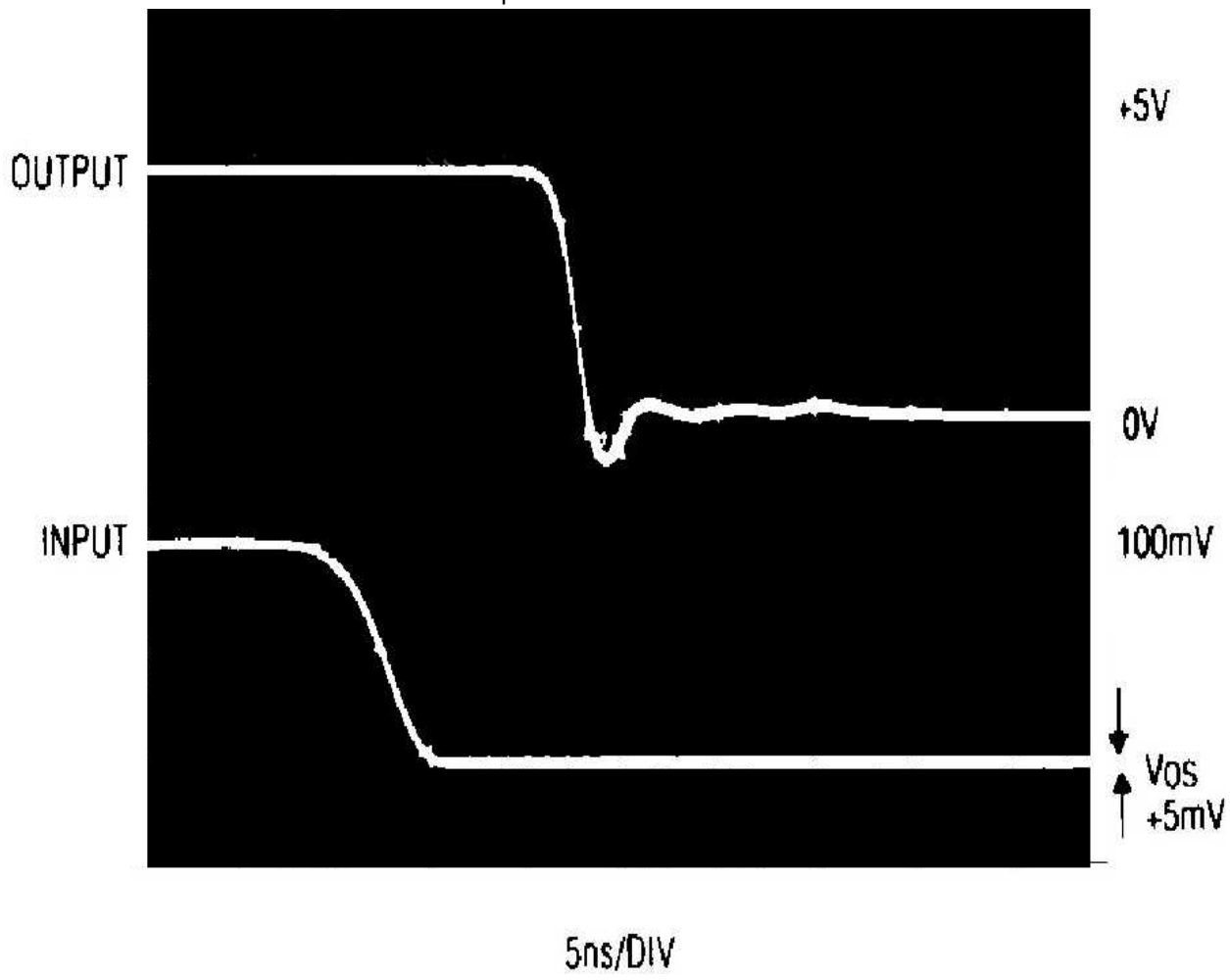
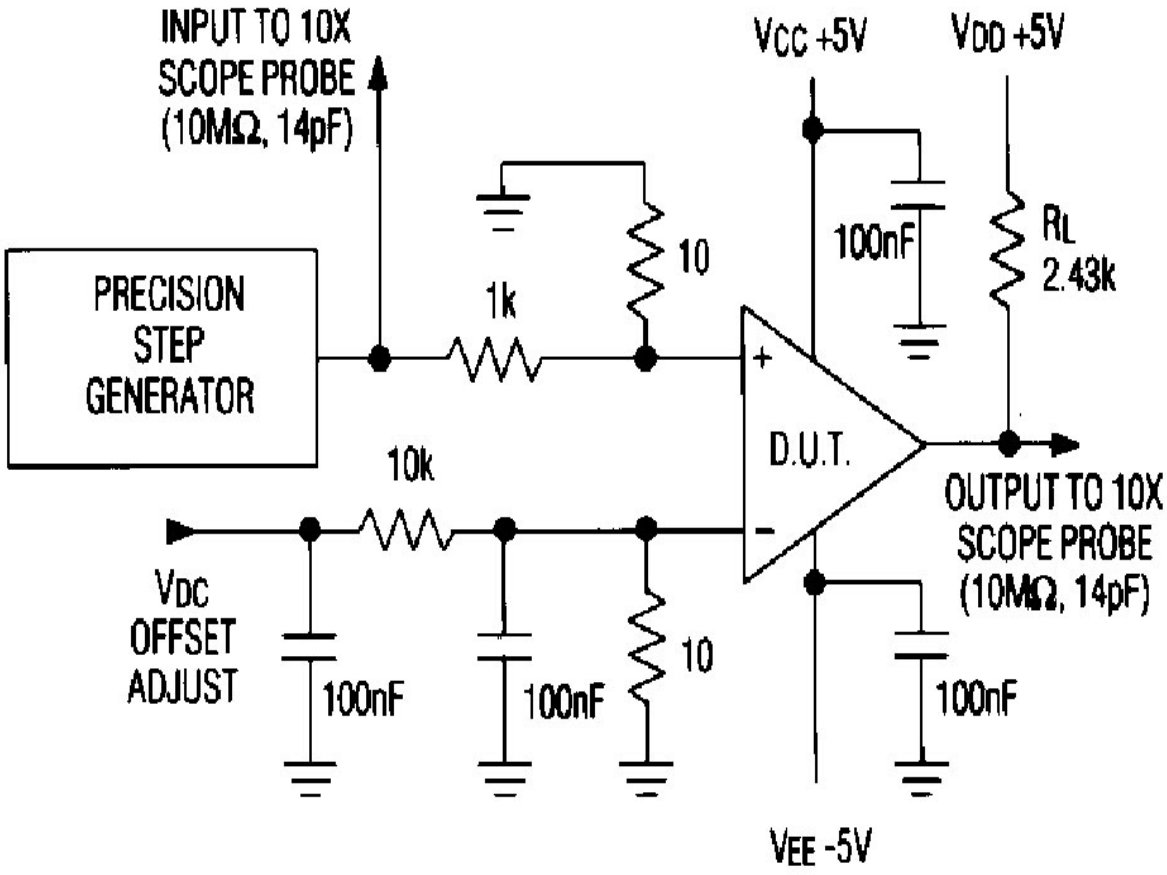


FIGURE 12. RESPONSE-TIME SETUP



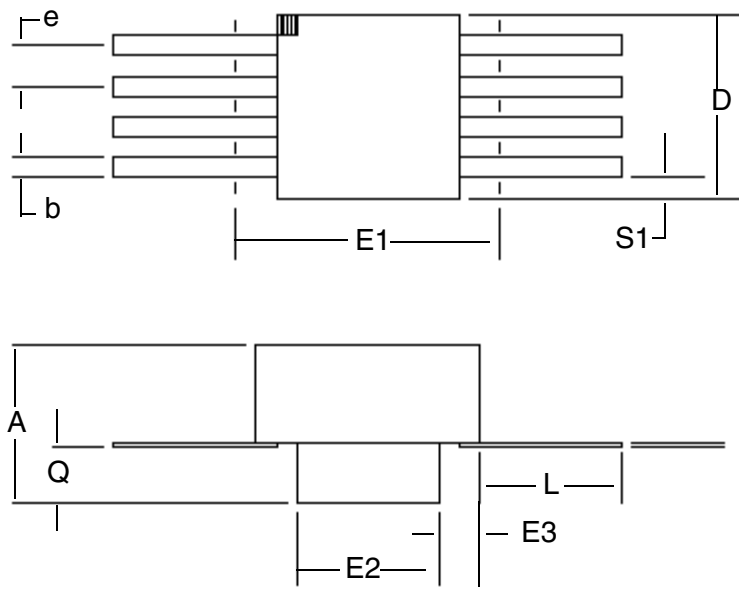


TABLE 13. 8 LEAD RAD-PAK FLAT PACKAGE

SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	.209	.227	.245
b	.015	.017	.019
c	.004	.005	.006
D	.250	.255	.260
E	.250	.255	.260
E1			.290
E2	.140	.145	.150
E3	.045	.055	--
e	.050 BSC		
L	.338	.348	.358
Q	.066	.070	.074
S1	.005	.044	--
N	8		

Important Notice:
These data sheets are created using the chip manufacturer's published specifications. DDC verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.
The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and DDC assumes no responsibility for the use of this information.
DDC's products are not authorized for use as critical components in life support devices or systems without express written approval from DDC.
Any claim against DDC must be made within 90 days from the date of shipment from DDC.
DDC's liability shall be limited to replacement of defective parts.

Product Ordering Information