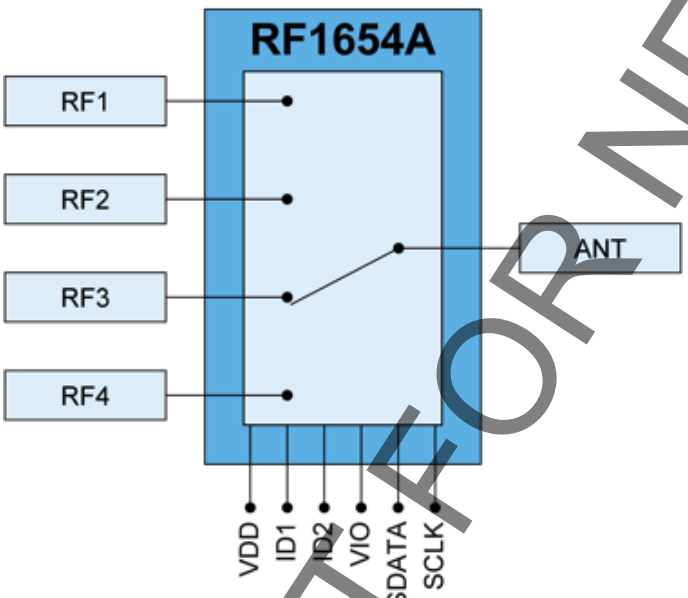
RF1654A

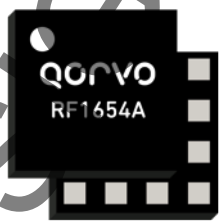
SP4T RFFE Addressable GSM High Power Switch

Product Overview

The RF1654A is a low loss, high isolation SP4T switch with performance optimized for GSM, CDMA, WCDMA, & LTE applications requiring high linearity and high power handling. The RF1654A is compatible with +1.3 V control logic, which is a key requirement for most cellular transceivers. Two select lines (ID0 & ID1) provide USID addressability and up to four placements of the RF1654A on the same design. The RF1654A is packaged in a compact 1.9 mm x 1.9 mm, 12-pin, module which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Functional Block Diagram





Package: 12 pin, 1.9 mm x 1.9 mm x 0.775 mm

Key Features

- Excellent insertion loss and isolation performance
- Multi-Band operation 400 MHz to 2700 MHz
- RFFE Serial Control Interface
- Low Band GSM Power handling +36 dBm into 50 Ω
- Addressability allows up to four placements of the RF1654A on the same platform
- Compact 1.9 mm x 1.9 mm module
- No DC blocking capacitors required (unless external DC is applied to the RF ports)

Applications

- Cellular Handset Applications
- Cellular Modems and USB Devices
- Multi-Mode GSM, EDGE, WCDMA Applications
- LTE Applications

Ordering Information

Part Number	Description
RF1654ASB	5-pc Sample Bag + Evaluation Board PCBA-410
RF1654ASQ	25-pc Sample Bag
RF1654ASR	100-pc Reel
RF1654ATR13-5K	5000-pc 13” Reel
RF1654APCK-410	Fully Assembled Evaluation Board

Absolute Maximum Ratings

Parameter	Rating	Unit
V_{DD}	6.0	V
V_{IO}, SDATA, SCLK	3.0	V
Maximum Input Power		
Momentary, infrequent occurrence, 50 Ω	+37	dBm
Momentary, infrequent occurrence, 6:1	+35	dBm
Continuous Operation, 50 Ω	+36	dBm
Continuous Operation, 6:1	+34	dBm
Operating Temperature	-30 to +90	°C
Storage Temperature	-65 to +150	°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					Nominal conditions unless otherwise stated. V_{DD} = 2.7 V, Temp. = 25 °C, 50 Ω., SDATA & SCLK = 1.8 V/0 V, V_{IO} = 1.8 V
Insertion Loss					
Insertion Loss RF1/2/3/4 - ANT		0.35	0.47	dB	400 MHz to 824 MHz
Insertion Loss RF1/2/3/4 - ANT		0.40	0.48	dB	824 MHz to 960 MHz
Insertion Loss RF1/2/3/4 - ANT		0.55	0.65	dB	1710 MHz to 1880 MHz
Insertion Loss RF1/2/3/4 - ANT		0.60	0.67	dB	1880 MHz to 2170 MHz
Insertion Loss RF1/2/3/4 - ANT		0.60	0.69	dB	2170 MHz to 2690 MHz
Isolation					
RF1 to 2 – 4, RF2 to 3/4, ANT to RF1/4	30	44		dB	400 MHz to 800 MHz
RF1 to 2 – 4, RF2 to 3/4, ANT to RF1/4	32	43		dB	800 MHz to 960 MHz
RF1 to 2 – 4, RF2 to 3/4, ANT to RF1/4	21	34		dB	1710 MHz to 2170 MHz
RF1 to 2 – 4, RF2 to 3/4, ANT to RF1/4	19	30		dB	2170 MHz to 2690 MHz
Harmonics (ANT to RF1/2/3/4)					
Low Band, $2F_o$ (GSM)		-66	-55	dBm	P_{IN} = +35 dBm, 50 Ω, f_o = 824 MHz
Low Band, $3F_o$ (GSM)		-57	-52	dBm	P_{IN} = +35 dBm, 50 Ω, f_o = 824 MHz
Low Band, ≥ $4F_o$ (GSM)		-82	-78	dBm	P_{IN} = +35 dBm, 50 Ω, f_o = 824 MHz
High Band, $2F_o$ (PCS)		-73	-61	dBm	P_{IN} = +32 dBm, 50 Ω, f_o = 1880 MHz
High Band, $3F_o$ (PCS)		-72	-60	dBm	P_{IN} = +32 dBm, 50 Ω, f_o = 1880 MHz
High Band, ≥ $4F_o$ (PCS)		-73	-60	dBm	P_{IN} = +32 dBm, 50 Ω, f_o = 1880 MHz
Low Band, $2F_o$ (B5)		-82	-78	dBm	P_{IN} = +26 dBm, 50 Ω, f_o = 824 MHz
Low Band, $3F_o$ (B5)		-80	-76	dBm	P_{IN} = +26 dBm, 50 Ω, f_o = 824 MHz
Low Band, ≥ $4F_o$ (B5)		-82	-78	dBm	P_{IN} = +26 dBm, 50 Ω, f_o = 824 MHz

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					Nominal conditions unless otherwise stated. V_{DD} = 2.7 V, Temp. = 25 °C, 50 Ω., SDATA & SCLK = 1.8 V/0 V, V_{IO} = 1.8 V
Harmonics (ANT to RF1/2/3/4) (continued)					
High Band, $2F_o$ (B10)		-74	-68	dBm	Pin = +26 dBm, 50 Ω, f_o = 1747.5 MHz
High Band, $3F_o$ (B10)		-73	-68	dBm	Pin = +26 dBm, 50 Ω, f_o = 1747.5 MHz
High Band, ≥ $4F_o$ (B10)		-74	-70	dBm	Pin = +26 dBm, 50 Ω, f_o = 1747.5 MHz
Low Band, $2F_o$ (B13)		-88	-84	dBm	Pin = +25 dBm, 50 Ω, f_o = 786.5 MHz
Low Band, $3F_o$ (B17)		-87	-82	dBm	Pin = +25 dBm, 50 Ω, f_o = 710 MHz @ 50 Ω.
Low Band, $3F_o$ (B17)		-82	-75	dBm	Pin = +25 dBm, 50 Ω, f_o = 710 MHz @ 3:1 VSWR
IMD2 (ANT to RF1/2/3/4)					
Low Band (B8)		-122	-119	dBm	F1 = 897.5 MHz at +20 dBm, F2= 1840 MHz at -15 dBm, Rx = 942.5 MHz
High Band (B2)		-125	-117	dBm	F1 = 1880 MHz at +20 dBm, F2 = 3840 MHz at -15 dBm, Rx = 1960 MHz
Low Band (C2K)		-123	-118	dBm	F1 = 824 MHz at +26 dBm, F2= 1693 MHz at -20 dBm, Rx = 869 MHz
High Band (C2K)		-122	-119	dBm	F1 = 1850 MHz at +26 dBm, F2 = 3780 MHz at -20 dBm, Rx = 1930 MHz
IMD3 (ANT to RF1/2/3/4)					
Low Band (BCO)		-143	-130	dBm	F1 = 782 MHz at +23 dBm, F2 = 827 MHz at +14 dBm, Rx = 872 MHz
Low Band (B13)		-126	-124	dBm	F1 = 786 MHz at +23 dBm, F2 = 825 MHz at +14 dBm, Rx = 747 MHz
Low Band (B8)		-128	-119	dBm	F1 = 897.5 MHz at +20 dBm, F2= 852.5 MHz at -15 dBm, Rx = 942.5 MHz
High Band (B2)		-123	-114	dBm	F1 = 1880 MHz at +20 dBm, F2= 1800 MHz at -15 dBm, Rx = 1960 MHz
VSWR					
		1.15	1.4	:1	400 MHz to 960 MHz
		1.25	1.5	:1	1710 MHz to 2690 MHz
Triple Beat Ratio (TBR) (ANT to RF1/2/3/4)					
BC0 (GSM800)	81	93		dBc	VSWR = 2:1
BC1 (PCS)	81	95		dBc	VSWR = 2:1
BC4	81	96		dBc	VSWR = 2:1
BC5 (GSM400)	81	94		dBc	VSWR = 2:1
BC14 (PCS)	81	95		dBc	VSWR = 2:1
BC15 (AWS)	81	97		dBc	VSWR = 2:1
DC Control and Electrical Specifications					
V_{DD} – Switch Supply Voltage	2.5	2.7	4.7	V	
V_{DD} – Supply Current		52	100	µA	Active Mode
V_{IO} – Interface Supply Voltage	1.65	1.8	1.95	V	
SDATA, SCLK – Voltage High	0.8x V_{IO}	1.8	V_{IO}	V	
SDATA, SCLK – Voltage Low	0		0.2x V_{IO}	V	
Switching Speed, one RF port to another		3	5	µs	10% to 90% RF

Control Logic

This SP12T switch is controlled by an RFFE bus interface, using V_{IO}, DATA, S–ID and CLK signals as defined by the truth table below:

		Register 0 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	Isolation	X	0	0	0	0	0	0	0
2	RF1	X	0	0	0	0	1	0	0
3	RF2	X	0	0	0	0	1	0	1
4	RF3	X	0	0	0	0	1	1	0
5	RF4	X	0	0	0	0	1	1	1

The ID0 and ID1 pins allow four possible placements of the RF1654A on the same platform by configuring the USID value.
The ID pins have internal pull-up resistors so a no-connect (NC) in the table below indicates the pin will be logic high.
The table below shows the product USID values that can be configured using the ID0 and ID1 inputs in Register 31.

Chip #	**IDO**	**ID1**	**USID [Reg 31 D3:D0]**
1	V_{IO}	V_{IO}	1011
2	GND	V_{IO}	1010
3	V_{IO}	GND	1001
4	GND	GND	1000

Note:
" NC (No Connection)" can be used instead of "V_{IO}" but increases the delay between V_{DD}/V_{IO} & data transfer from 10 µs to 35 µs. See "Power ON and OFF Sequence".

Logic ID

1. USID = See Table above (Reg 31 Bits 3:0)
2. Manufacturing ID = Hex 134 (Reg 30 Bits 7:0 & Reg 31 Bits 9:8)
3. Product ID = Hex 2C (Reg 29 Bits 7:0)

Power ON and OFF sequence

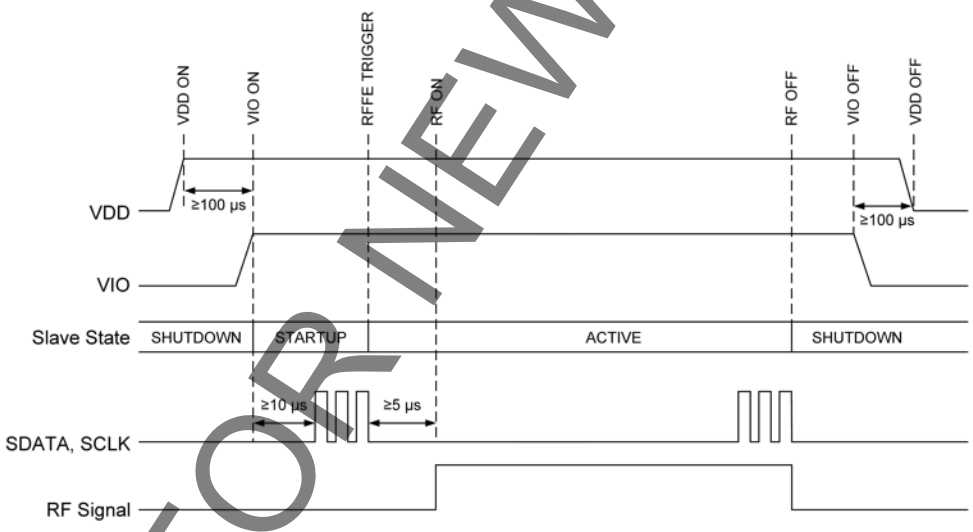
Power ON –

1. Apply voltage supply – V_{DD}
2. Wait 100 µs then apply logic supply – V_{IO}
3. Wait 10 µs or greater* and then apply RFFE bus signals (SCLK and SDATA)
4. Wait 5 µs or greater after RFFE bus goes idle and then apply the RF Signal

Note: * " NC (No Connection)" can be used instead of "V_{IO}" for ID0 and ID1 but increases the delay between V_{DD}/V_{IO} and data transfer from 10 to 35 µs.

Power OFF –

1. Remove the RF Signal
2. Remove RFFE bus signals (SCLK and SDATA)
3. Remove logic supply – V_{IO}
4. Wait 100 µs then remove voltage supply – V_{DD}



Note:
V_{IO} can be applied to the device before V_{DD} or removed after V_{DD} It is important to wait 10 µs after V_{IO} & V_{DD} are applied before sending SDATA to ensure correction data transmission.
The minimum time between a power up and power down sequence (and vice versa) is ≥ 10 ms.

Definitions of Programmable Registers

Register 0 (Zero) controls the Switch Paths

Writing to Register_0

Command Frame															Data Frame										
SSC		USID				WRITE			Register Address					P	Data Payload									P	BP
S1	S0	ID3	ID2	ID1	ID0	C2	C1	C0	A4	A3	A2	A1	A0	P	D7	D6	D5	D4	D3	D2	D1	D0	P	BP
1	0	1	0	0/1	0/1	0	1	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0
																	Switch Path-Table (1)							

Bit length for WRITE: 24 bits

Reading from Register_0

Register 0x0000 (Register_0); Zero																									
Command Frame																Data Frame									
SSC		USID				READ			Register Address					P	BP	Data Payload								P	BP
S1	S0	ID 3	ID 2	ID 1	ID 0	C2	C1	C0	A4	A3	A2	A1	A0	P	BP	D7	D6	D5	D4	D3	D2	D1	D0	P	BP
1	0	1	0	0/1	0/1	0	1	1	0	0	0	0	0	1	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0
																		Switch Path-Table (1)							

Bit length for READ: 25 bits

Contents of Register_0

USID configurable to 1000, 1001, 1010 & 1011 (refers to RFMD Antenna Switch Module with Carrier Aggregation)
WRITE or READ (WRITE = 010; READ = 011)
Register Address: 00000b
Switch Path: Total of six bits described in Table (1) for all 64 states [D5: D0]

Register 28 controls the Power Modes

There are three active states in the Power Mode selection (Active, Startup and Low Power).
Writing to Register 28

Command Frame															Data Frame										
SSC		USID				WRITE			Register Address					P	Data Payload									P	BP
S1	S0	ID3	ID2	ID1	ID0	C2	C1	C0	A4	A3	A2	A1	A0	P	D7	D6	D5	D4	D3	D2	D1	D0	P	BP
1	0	1	0	0/1	0/1	0	1	0	1	1	1	0	0	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0
															State		Trig Mask			Trigger					

Bit length for WRITE: 24 bits

Reading from Register 28

Register 0x001C (Register_1C); 28																									
Command Frame																Data Frame									
SSC		USID				READ			Register Address					P	BP	Data Payload								P	BP
S1	S0	ID 3	ID 2	ID 1	ID 0	C2	C1	C0	A4	A3	A2	A1	A0	P	BP	D7	D6	D5	D4	D3	D2	D1	D0	P	BP
1	0	1	0	0/1	0/1	0	1	1	1	1	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0
																State		Trig Mask			Trigger				

Bit length for READ: 25 bits

Contents of Register 28

USID is configurable to: 1000, 1001, 1010 & 1011 (refers to RFMD Antenna Switch Module with Carrier Aggregation)
WRITE or READ (WRITE = 010; READ = 011)
Register Address: 11100b

PWR_MODE STATE is defined by the two bits [7:6]

When the V_{IO} is applied to the RF1654A, the part will begin in START-UP mode, will then automatically go to ACTIVE mode and ready for programming the switch paths by performing writes to Register_0.

– Normal Operation (ACTIVE): 00b
– Default settings (STARTUP): 01b
– Low Power (LOW POWER): 11b

Definition of the Trigger Mask bits and the Trigger bits

Trigger_Mask_2, Trigger_Mask_1, Trigger_Mask_0: will use [5:3] bits with setting 000b.
Trigger_2, Trigger_1, Trigger_0: will use [2:0] bits with setting 000b.

Registers to Read Part Information

The following three registers can be read from to confirm Product ID, Manufacturer ID value and USID values.

Reading from Register 29

Register 0x001D (Register_1D)

Command Frame																Data Frame									
SSC		USID				READ			Register Address					P	BP	Data Payload								P	BP
S1	S0	ID 3	ID 2	ID 1	ID 0	C2	C1	C0	A4	A3	A2	A1	A0	P	BP	D7	D6	D5	D4	D3	D2	D1	D0	P	BP
1	0	1	0	0/1	0/1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	1	1	0	0	1	0
																Product_ID									

Bit length for READ: 25 bits

Product _ID defined as 00101100b (0 x 2C)
Register Address: 11101b

Reading from Register 30

Register 0x001E (Register_1E)

Command Frame																Data Frame									
SSC		USID				READ			Register Address					P	BP	Data Payload								P	BP
S1	S0	ID 3	ID 2	ID 1	ID 0	C2	C1	C0	A4	A3	A2	A1	A0	P	BP	D7	D6	D5	D4	D3	D2	D1	D0	P	BP
1	0	1	0	0/1	0/1	0	1	1	1	1	1	1	0	1	0	0	0	1	1	0	1	0	0	0	0
																Manufacturer_ID (lower 8 bits)									

Bit length for READ: 25 bits

Manufacturer _ID is defined for RFMD as **0 x 134.**
This is a 10 bit word with the **8 lower bits** [D7: D0] in Register 30.
Register Address: 11110b

Reading from Register 31

Register 0x001F (Register_1F)

Command Frame																Data Frame									
SSC		USID				READ			Register Address					P	BP	Data Payload								P	BP
S1	S0	ID 3	ID 2	ID 1	ID 0	C2	C1	C0	A4	A3	A2	A1	A0	P	BP	D7	D6	D5	D4	D3	D2	D1	D0	P	BP
1	0	1	0	0/1	0/1	0	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	0/1	0/1	0	0
																Reserved		Man_ID		USID					

Bit length for READ: 25 bits

Manufacturer_ID is defined for RFMD as **0 x 134**.
The Manufacturer_ID is a 10 bit word with the **2 upper bits** [D5: D4] in Register 31.
Bits [D1: D0] are configurable to: 00, 01, 10 & 11
Register Address: 11111b

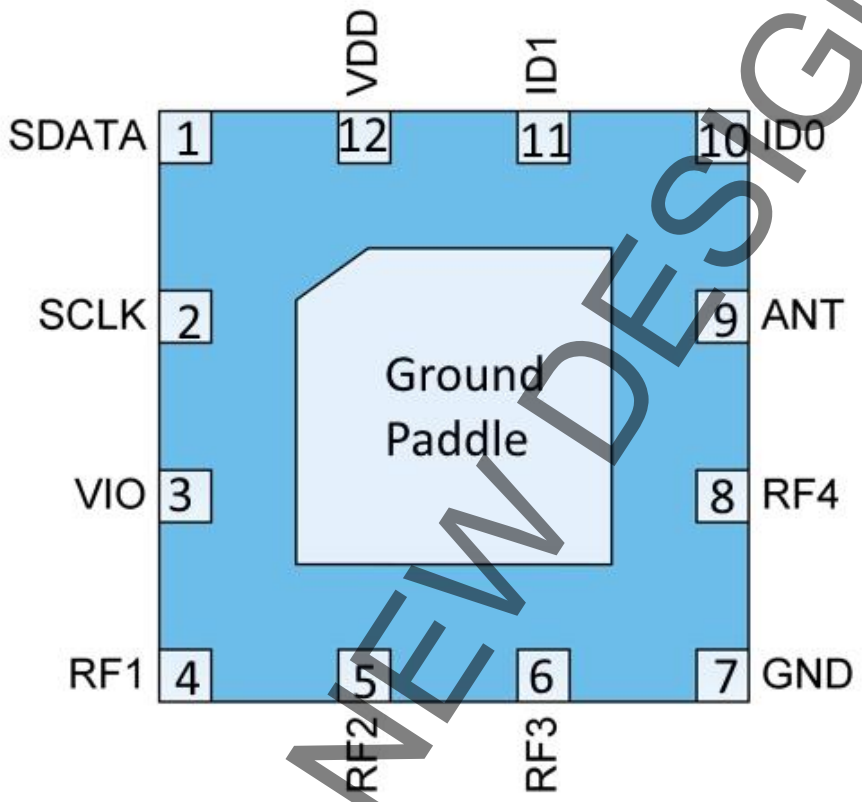
Register Definition Table

Register Address	Register Name	Data Bits	Function	Description	Default	BROADCAST_ID support	Trigger support	R/W
0x0000	REGISTER_0	6:0	MODE_CTRL	Device control (mission mode)	Device dependent	No	Yes	R/W
0x001C	PM_TRIG	7:6	PWR_MODE	00: Normal operation (ACTIVE) 01: Default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved	01	Yes	No	R/W
		5	Trigger_Mask_2	If this bit is set, trigger 2 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 2, the data goes directly to the destination register.	0	No	No	
		4	Trigger_Mask_1	If this bit is set, trigger 1 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 1, the data goes directly to the destination register.	0	No	No	
		3	Trigger_Mask_0	If this bit is set, trigger 0 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 0, the data goes directly to the destination register.	0	No	No	
		2	Trigger_2	A write of a one to this bit loads trigger 2's registers.	0	Yes	No	
		1	Trigger_1	A write of a one to this bit loads trigger 1's registers.	0	Yes	No	
		0	Trigger_0	A write of a one to this bit loads trigger 0's registers.	0	Yes	No	
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	See Register 29 Definition	No	No	R
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	See Register 30 Definition	No	No	R

Register Address	Register Name	Data Bits	Function	Description	Default	BROADCAST_ID support	Trigger support	R/W
0x001F	MAN_USID	7:6	SPARE	These are read-only bits that are reserved and yield a value of 0b00 at readback.	00	No	No	R
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	See Register 31 Definition			
		3:0	USID	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Register 31 Definition			
0x001A	RFFE_STATUS	7	SOFTWARE RESET	0: Normal operation; 1: Software reset (reset of all configurable registers to default values except for USID, GSID, or PM_TRIG.	0	No	No	R/W
		6	COMMAND_FRAME_PARITY_ERR	Command sequence received with parity error – discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame parity error = 1	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error	0			
		2	READ_UNUSED_REG	Read command to an invalid address	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_SID.	0			
0x001B	GROUP_SID	7:4	RESERVED			Not applicable	Not required	R/W
		3:0	GROUP_SID	Group slave ID	0x0			

Pin Out

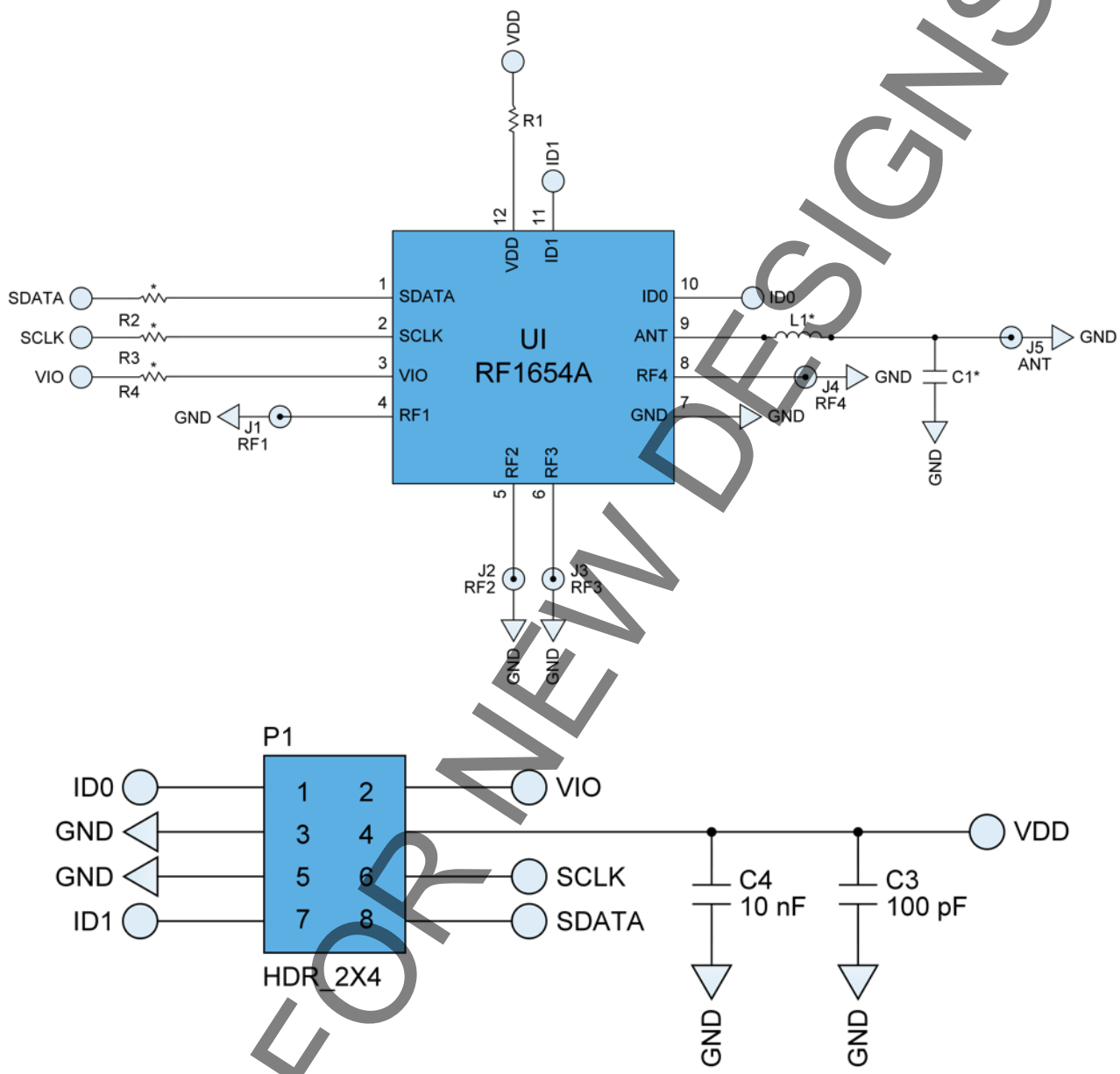
Top View



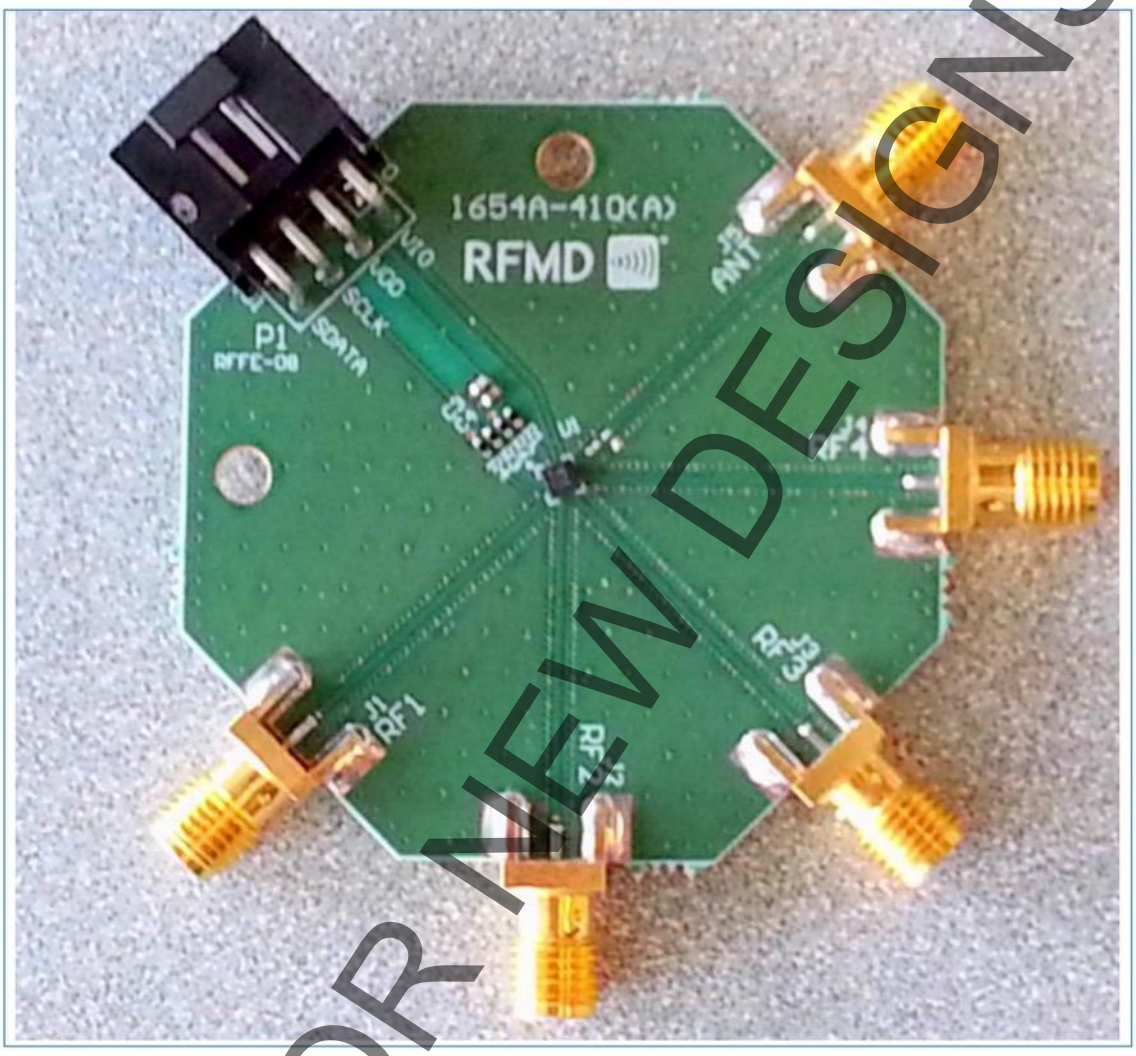
Pin – Out Description

Pin	Name	Description
1	SDATA	Serial Data
2	SCLK	Serial Clock
3	V_{IO}	Supply voltage for RFFE interface
4	RF1	RF I/O
5	RF2	RF I/O
6	RF3	RF I/O
7	GND	RF and DC Ground
8	RF4	RF I/O
9	ANT	RF signal in/out of Antenna
10	ID0	USID bit 0 configurable Address input
11	ID1	USID bit 1 configurable Address input
12	V_{DD}	Power Supply
Ground Paddle	GND	RF and DC Ground

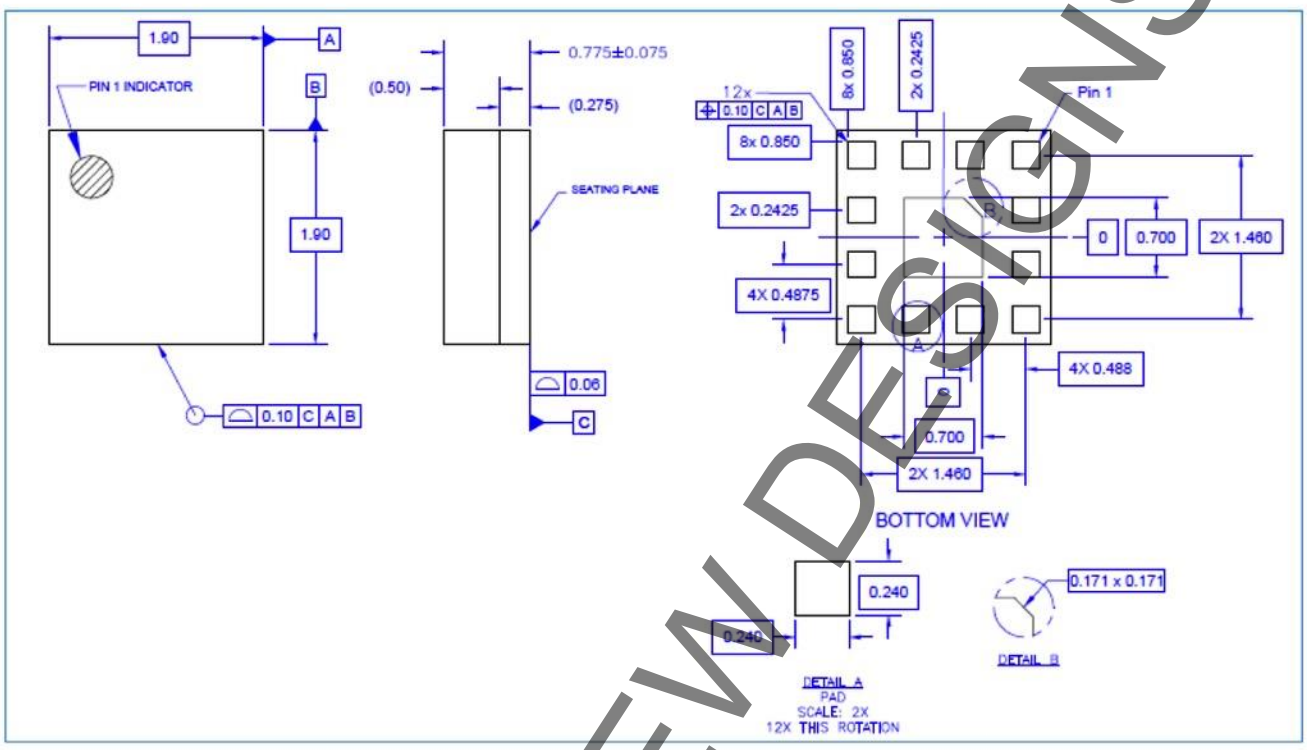
Evaluation Board Schematic



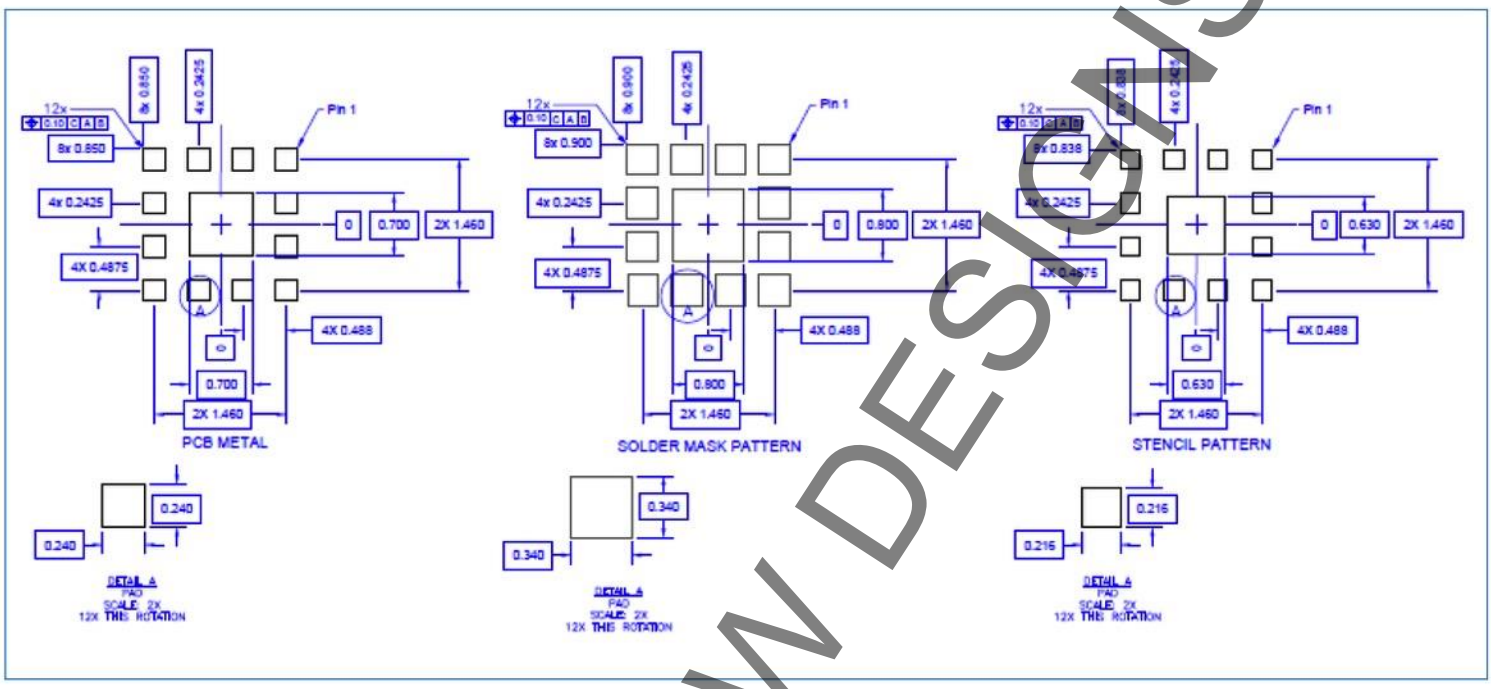
Evaluation Board



Package Drawing



PCB Metal and Stencil Patterns



Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

REVISION HISTORY

REVISION	DESCRIPTION
A	Initial release
J	Converted from RFMD to Qorvo template
K	Updated Orderable part #
L	Added Not Recommended for New Designs marks

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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