

## 74165 Shift Register

8-Bit Serial/Parallel-In, Serial-Out Shift Register  
Product Specification

### Logic Products

- Asynchronous 8-bit parallel load
- Synchronous Serial input
- Clock Enable for "do nothing" mode
- See '166 for fully synchronous operation

### DESCRIPTION

The '165 is an 8-bit parallel load or serial-in shift register with complementary Serial outputs ( $Q_7$  and  $\bar{Q}_7$ ) available from the last stage. When the Parallel Load ( $\bar{P}L$ ) input is LOW, parallel data from the  $D_0 - D_7$  inputs are loaded into the register asynchronously. When the  $\bar{P}L$  input is HIGH, data enters the register serially at the  $D_S$  input and shifts one place to the right ( $Q_0 \rightarrow Q_1 \rightarrow Q_2$ , etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the  $Q_7$  output to the  $D_S$  input of the succeeding stage.

The Clock input is a gated-OR structure which allows one input to be used as an active LOW Clock Enable ( $\bar{C}E$ ) input. The pin assignment for the CP and  $\bar{C}E$

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74165	26MHz	42mA

### ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74165N

#### NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
$\bar{P}L$	Input	2ul
Other	Inputs	1ul
All	Outputs	10ul

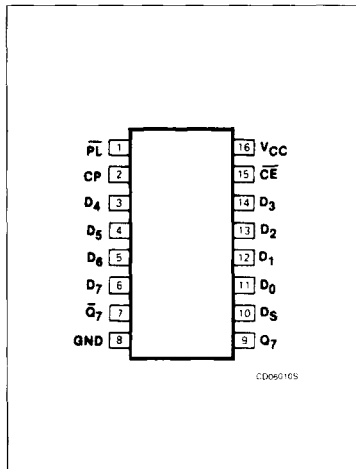
#### NOTE:

A 74 unit load (ul) is understood to be  $40\mu A I_{IH}$  and  $-1.6mA I_{IL}$ .

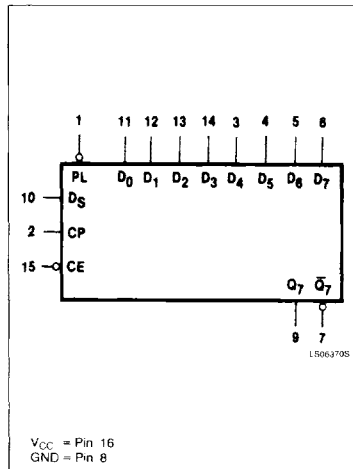
inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of  $\bar{C}E$  input should only take place while the CP is HIGH for predictable operation. Also, the CP and

$\bar{C}E$  inputs should be LOW before the LOW-to-HIGH transition of  $\bar{P}L$  to prevent shifting the data when  $\bar{P}L$  is released.

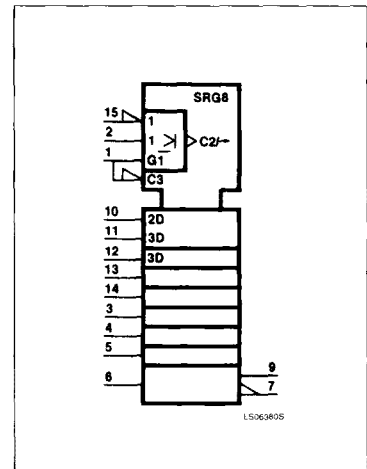
### PIN CONFIGURATION



### LOGIC SYMBOL



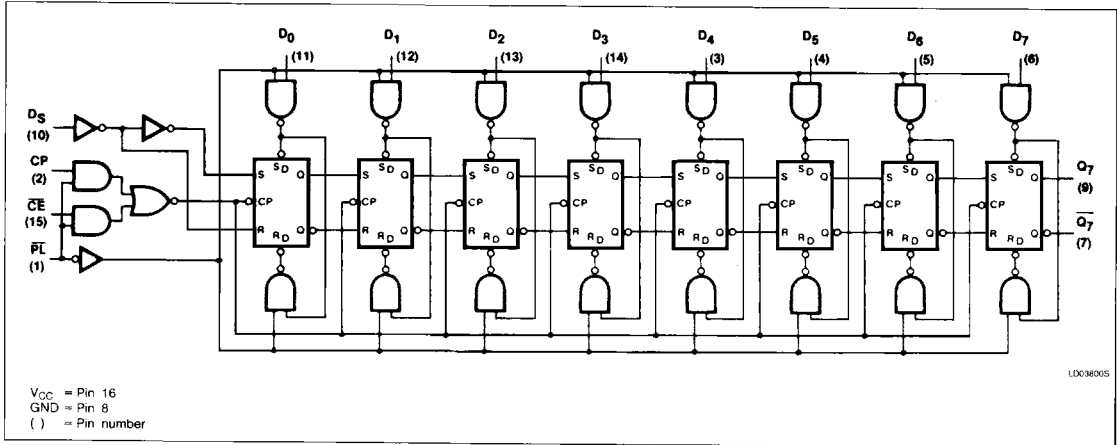
### LOGIC SYMBOL (IEEE/IEC)



# Shift Register

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## LOGIC DIAGRAM



## MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS					Q <sub>n</sub> REGISTER		OUTPUTS	
	PL	CE	CP	D <sub>S</sub>	D <sub>0</sub> - D <sub>7</sub>	Q <sub>0</sub>	Q <sub>1</sub> - Q <sub>6</sub>	Q <sub>7</sub>	$\bar{Q}_7$
Parallel load	L	X	X	X	L	L	L - L	L	H
	L	X	X	X	H	H	H - H	H	L
Serial shift	H	L	↑	l	X	L	q <sub>0</sub> - q <sub>5</sub>	q <sub>6</sub>	$\bar{q}_6$
	H	L	↑	h	X	H	q <sub>0</sub> - q <sub>5</sub>	q <sub>6</sub>	q <sub>6</sub>
Hold "do nothing"	H	H	X	X	X	q <sub>0</sub>	q <sub>1</sub> - q <sub>6</sub>	q <sub>7</sub>	$\bar{q}_7$

H = HIGH voltage level.

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.

L = LOW voltage level.

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

q<sub>n</sub> = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.

X = Don't care.

↑ = LOW-to-HIGH clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V <sub>CC</sub>	Supply voltage	7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +5.5	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in HIGH output state	-0.5 to +V <sub>CC</sub>	V
T <sub>A</sub>	Operating free-air temperature range	0 to 70	°C

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## RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	4.75	5.0	5.25	V
V <sub>IH</sub>	HIGH-level input voltage	2.0			V
V <sub>IL</sub>	LOW-level input voltage			+0.8	V
I <sub>IK</sub>	Input clamp current			-12	mA
I <sub>OH</sub>	HIGH-level output current			-800	μA
I <sub>OL</sub>	LOW-level output current			16	mA
T <sub>A</sub>	Operating free-air temperature	0		70	°C

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS <sup>1</sup>	74165			UNIT
			Min	Typ <sup>2</sup>	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OH</sub> = MAX	2.4	3.4		V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>OL</sub> = MAX		0.2	0.4	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-1.5	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V			1.0	mA
I <sub>IH</sub>	HIGH-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4V	PL input		80	μA
			Other inputs		40	μA
I <sub>IL</sub>	LOW-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4V	PL input		-3.2	mA
			Other inputs		-1.6	mA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX	-18		-55	mA
I <sub>CC</sub>	Supply current <sup>4</sup> (total)	V <sub>CC</sub> = MAX		42	63	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- I<sub>OS</sub> is tested with V<sub>OUT</sub> = +0.5V and V<sub>CC</sub> = V<sub>CC</sub> MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the outputs open, CE and CP at 4.5V, and a clock pulse applied to the PL input, I<sub>CC</sub> is measured first with the Parallel Data inputs at 4.5V, then with the Parallel Data inputs grounded.

AC ELECTRICAL CHARACTERISTICS T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V

PARAMETER		TEST CONDITIONS	74		UNIT
			C <sub>L</sub> = 15pF, R <sub>L</sub> = 400Ω		
			Min	Max	
f <sub>MAX</sub>	Maximum shift frequency	Waveform 1	20		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Clock to output	Waveform 1		24 31	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay PL to output	Waveform 2		31 40	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>7</sub> to Q <sub>7</sub>	Waveform 3		17 36	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay D <sub>7</sub> to Q <sub>7</sub>	Waveform 3		27 27	ns

## NOTE:

Per industry convention, f<sub>MAX</sub> is the worst case value of the maximum device operating frequency with no constraints on t<sub>r</sub>, t<sub>f</sub>, pulse width or duty cycle.

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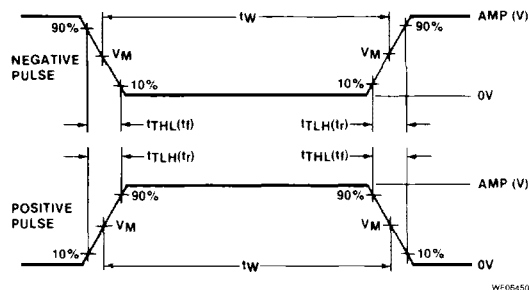
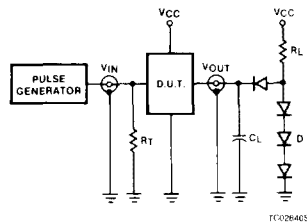
## AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		UNIT
		Min	Max	
$t_w$ Clock pulse width	Waveform 1	25		ns
$t_w$ $\overline{\text{PL}}$ pulse width	Waveform 2	15		ns
$t_s$ Set-up time, $D_S$ to clock	Waveform 4	20		ns
$t_h$ Hold time, $D_S$ to clock	Waveform 4	0		ns
$t_s(L)$ Set-up time, LOW $\overline{\text{CE}}$ to clock	Waveform 4	30		ns
$t_h$ Hold time, $\overline{\text{CE}}$ to clock	Waveform 4	0		ns
$t_s$ $\overline{\text{PL}}$ set-up time to clock	Waveform 2	45		ns
$t_s$ Set-up time, $D_5$ and $D_7$ <sup>(1)</sup> to $\overline{\text{PL}}$	Waveform 5	10		ns

**NOTE:**

1. The remaining six Data inputs and  $D_5$  are LOW. Prior to test, HIGH level data is loaded into  $D_7$  input.

## TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3\text{V}$  for 74LS;  $V_M = 1.5\text{V}$  for all other TTL families.

### Test Circuit For 74 Totem-Pole Outputs

**DEFINITIONS**

$R_L$  = Load resistor to  $V_{CC}$ ; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$t_{TLH}$ ,  $t_{THL}$  Values should be less than or equal to the table entries.

### Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	$t_{TLH}$	$t_{THL}$
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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## AC WAVEFORMS

