DRAM MODULE

1 MEG x 8 DRAM

FAST-PAGE-MODE (MT8D18)
LOW POWER,
EXTENDED REFRESH (MT8D18 L)

FEATURES

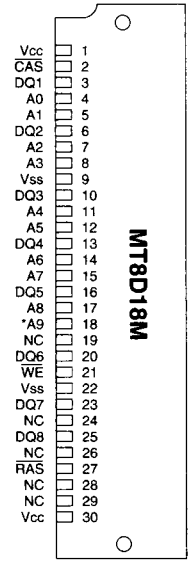
- Industry-standard pinout in a 30-pin single-in-line package
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- Low power, 24mW (2.4mW L-version) standby; 1,400mW active, typical
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- FAST-PAGE-MODE access cycle
- Low CMOS standby current, 1.6mA maximum (L-version)

OPTIONS MARKING

- Timing
  - 60ns access -6
  - 70ns access -7
  - 80ns access -8
- Packages
  - Leadless 30-pin SIMM M
- Power/Refresh
  - Normal Power/8ms Blank
  - Low Power/64ms L
- Part Number Example: MT8D18ML-6

PIN ASSIGNMENT (Top View)

30-Pin SIMM
(DE-3)



*Address not used for $\overline{RAS}$-ONLY REFRESH

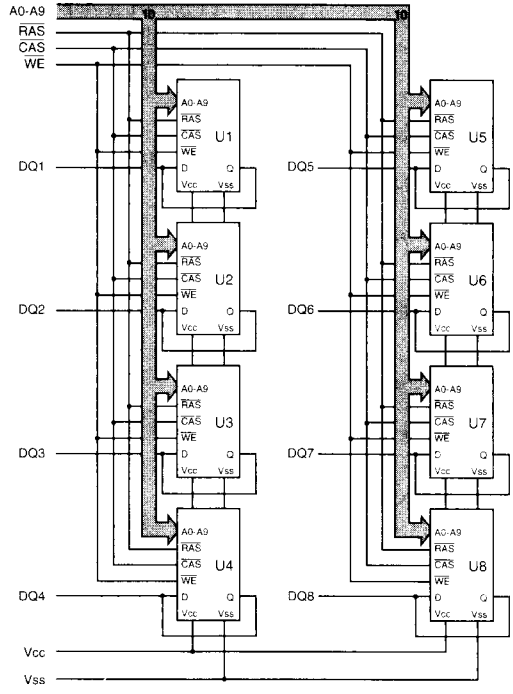
GENERAL DESCRIPTION

The MT8D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. READ or WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Early WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms (64ms on L-version only), regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



U1 - U8 = MT4C1024DJ
U1 - U8 = MT4C1024DJ L (L-version)

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA-IN/OUT
					t_R	t_C	DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY-WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data-In
WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	X	X	X	High-Z
BATTERY BACKUP (BBU) REFRESH (L-version)		H→L	L	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE: Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	D9, $\overline{CAS9}$	I_I	-2	2	µA	
	A0-A9, $\overline{RAS}$, $\overline{WE}$	I_I	-16	16	µA	
OUTPUT LEAKAGE: (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-8, Q9	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output HighVoltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	MAX -8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16	16	16	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	8	8	8	mA	23
		1.6	1.6	1.6	mA	23, 25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	720	640	560	mA	3, 4
		680	600	520	mA	3, 4, 25
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	560	480	400	mA	3, 4
		520	440	360	mA	3, 4, 25
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	720	640	560	mA	3
		680	600	520	mA	3, 25
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	720	640	560	mA	3, 5
		680	600	520	mA	3, 5, 25
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1µs; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (512 rows at 125µs = 64ms)	I_{CC7}	1.6	1.6	1.6	mA	25

DRAM MODULE

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}		51	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		67	pF	2
Input/Output Capacitance: DQ1-DQ8	C_{IO}		16	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	n/a		n/a		n/a		n/a	24
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	n/a		n/a		n/a		n/a	24
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	tCAC		20		20		20	ns	15
Access time from column-address	tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST-PAGE-MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST-PAGE-MODE)	tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	40	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	15		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	45		55		60		ns	
Column-address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		0		ns	19

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

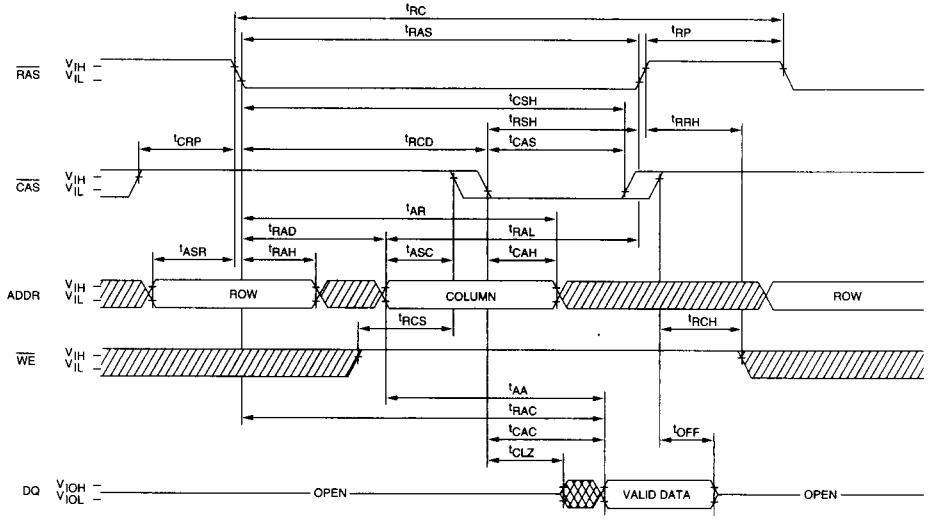
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ 75°C; Vcc = 5V ± 10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	
Output buffer turn-off delay	tOFF	3	20	3	20	3	20	ns	20, 26
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	21
Data-in hold time	tDH	15		15		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF		8/64		8/64		8/64	ms	7/25
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	10		15		15		ns	5

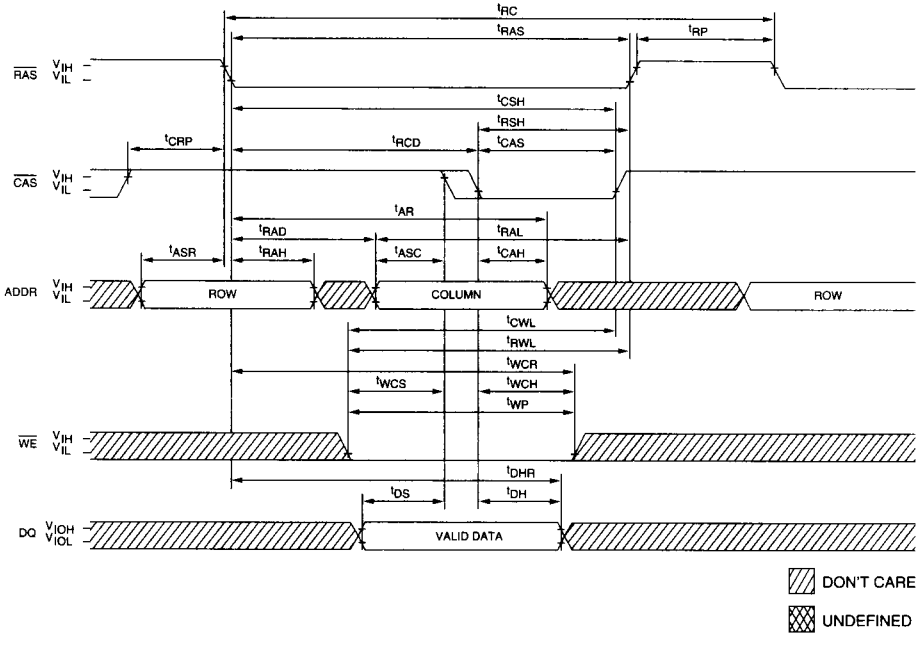
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, Vcc = 5V, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles.
22. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
23. All other inputs equal Vcc -0.2V.
24. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to the common DQ configuration of U1-U8.
25. Applies to the L-version only.
26. The 3ns minimum is a parameter guaranteed by design.

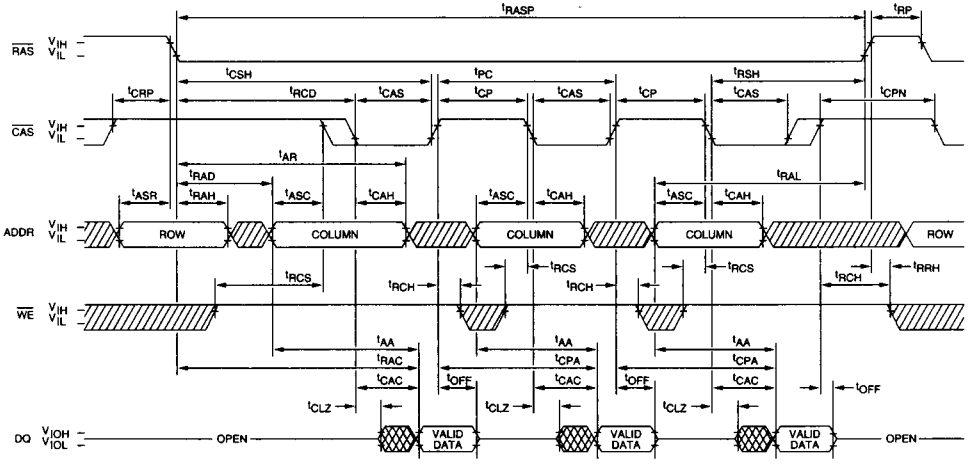
READ CYCLE



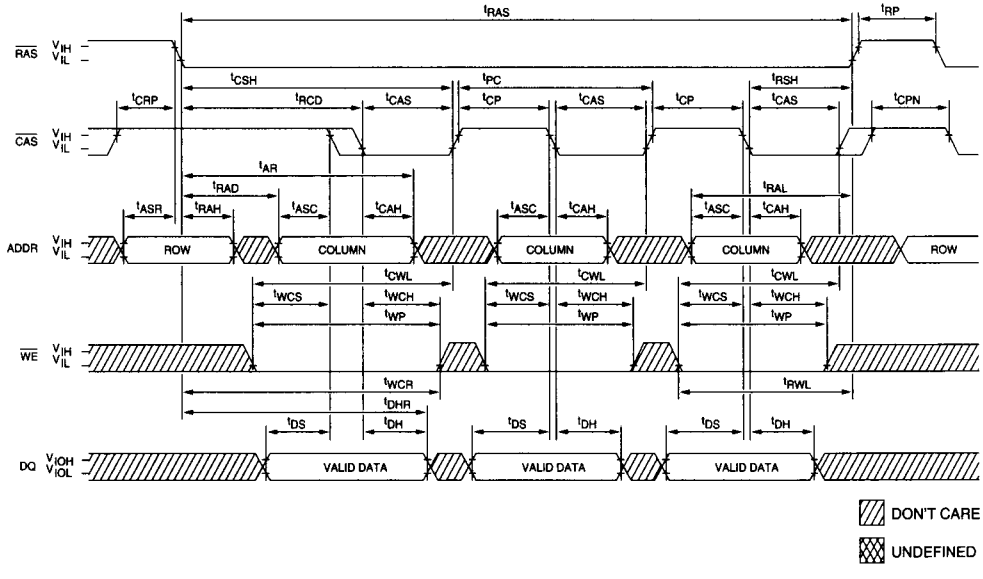
EARLY-WRITE CYCLE



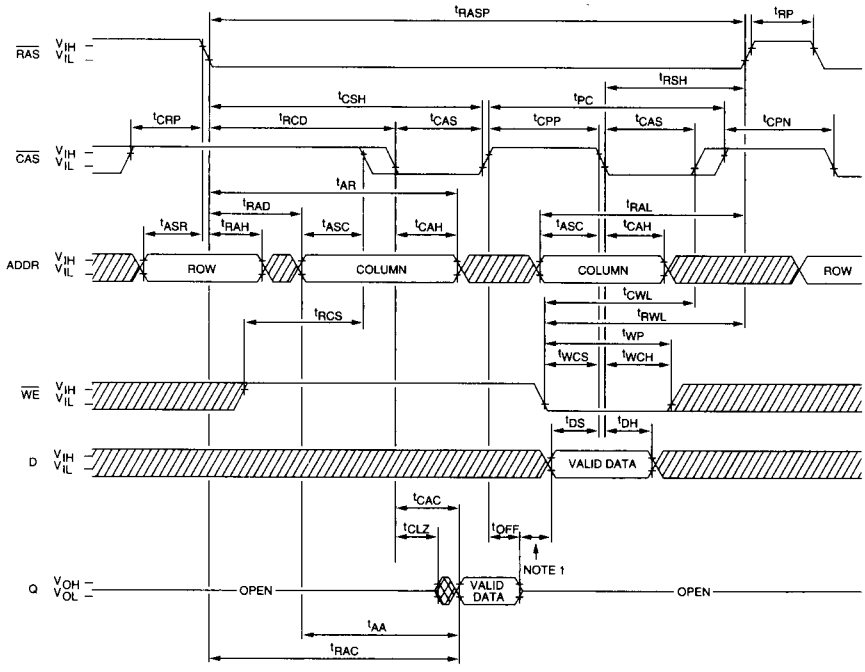
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE

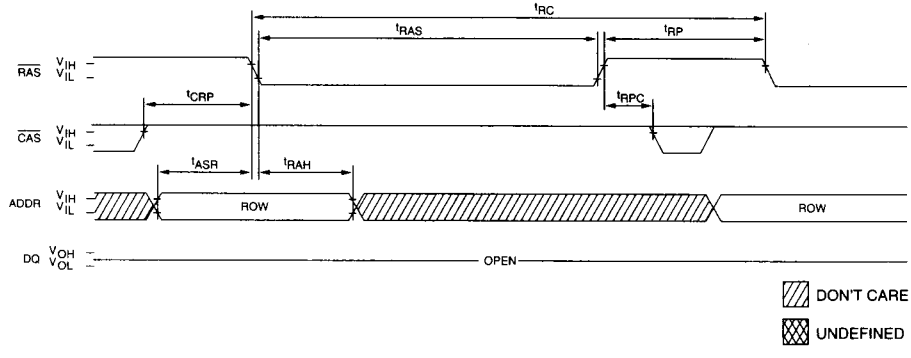


FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

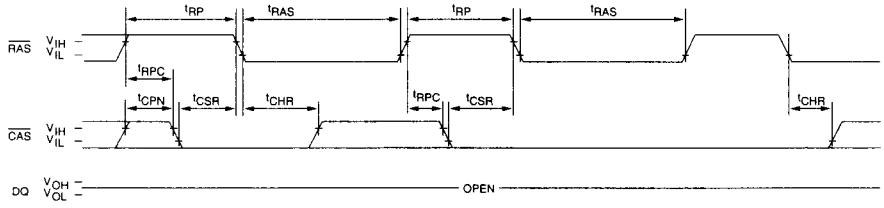


NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

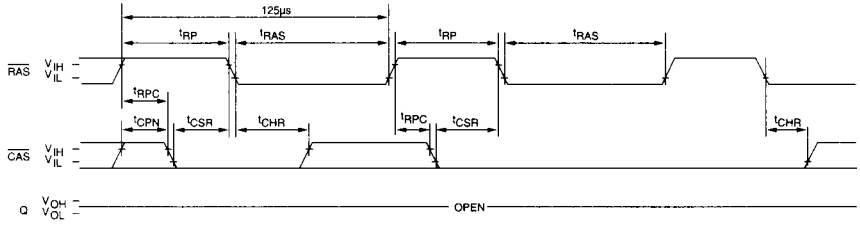
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and WE = DON'T CARE)



CBR REFRESH CYCLE
(A0-A9 and $\overline{WE}$ = DON'T CARE)



BBU REFRESH CYCLE [25]
(A0-A9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [22]
($\overline{WE}$ = HIGH)