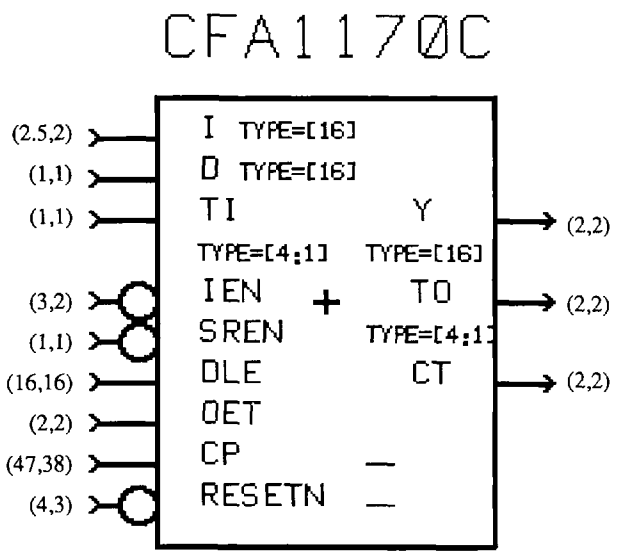
GENERAL DESCRIPTION: AM29117 - 16-BIT MICROPROCESSOR

CFA1170C is designed to be fully compatible with AM29117 with the exceptions that bidirectional pins are separated into input and output signals, and that three-state outputs are always enabled. The user can easily use OET and OEYN with bidirectional and three-state buffers to make the part work exactly as the standard chip does. Besides normal ALU operations, CFA1170C has Barrel Shifter, Priority Encoder, and Cyclic-Redundancy-Check circuits built in. The user can use RESETN input to reset the internal flip-flops or tie this signal to HIGH and enter two NO-OP instructions for initialization. Please refer to AM29117 datasheet for detailed instruction operations.

PIN CONNECTION DIAGRAM:



FEATURES:

- Master reset capability
- Built in Barrel Shifter, Priority Encode, and Cyclic-Redundancy-Check circuit
- No OEY signal and Y-bus always output enable
- For undefined Instruction, megafunction is not compatible with standard part
- During the first cycle of Two-Address Immediate Instruction, IEN can be any value before the destination address become effective

EQUIVALENT USED GATES: 4391 GATES
(for rough area estimates)

THIS MEGAFUNCTION CONSISTS OF :
One 22 cols x 108 rows metal megacell;
3321 soft-coded gates.

POWER: NOT AVAILABLE.

FAULT COVERAGE(%): 95.9%

This megafunction was designed to be 100% functionally compatible as specified in the vendor's data book. However, LSI LOGIC makes no warranty that this megafunction behaves identically to the standard part. It is the user's responsibility to assure that the megafunction operates correctly in his/her ASIC design and meets desired system requirements.

PIN DESCRIPTION:

Inputs:

D15:0 Data Input Lines
D15:0 are used as external data inputs which allow data to be directly loaded into the 16-bit Data Latch.

DLE Data Latch Enable
When DLE is HIGH, the 16-bit Data Latch is transparent and is latched when DLE is LOW.

I15:0 Instruction Inputs
Sixteen Instruction Inputs, used to select the operation to be performed in the CFA1170C. Also used as data inputs while performing immediate instructions.

$\overline{IEN}$ Instruction Enable (low)
When IEN is LOW, data can be written into RAM when the clock is LOW. The Accumulator can accept data during the LOW-to-HIGH transition of the clock. Having IEN LOW, the Status Register can be updated when SRE is LOW. With IEN HIGH, the conditional test output, CT, is disabled as a function of the instruction inputs.

SREN Status Register Enable (low)
When SRE and IEN are both LOW, the Status Register is updated at the end of all instruction with the exception of NO-OP, Save Status, and Test Status. Having either SRE or IEN HIGH will inhibit the Status Register from changing.

CP Clock Pulse
The clock input to the CFA1170C. The RAM latch is transparent when the clock is HIGH. When the clock goes LOW, the RAM output is latched. Data is written into the RAM during the LOW period of the clock, provided IEN is LOW, and if the instruction being executed designates the RAM as the destination of operation. The Accumulator and Status Register will accept data on the LOW-to-HIGH transition of the clock if IEN is also LOW. The Instruction Latch becomes transparent when it exits an immediate instruction mode during a LOW-to-HIGH transition of the clock.

OET Output Enable
When OET is LOW, 4-bit T outputs are disabled; when OET is HIGH, the 4-bit T outputs are enabled.

RESETN Reset Pin
This Reset Signal is used to reset the internal Flip-Flop.

Outputs:

Y15:0 Data Output Lines
The sixteen data output lines are always enabled in CFA1170C.

CT Conditional Test
The condition code multiplexer selects one of the twelve condition code signals and places it on the CT output. A HIGH on the CT output indicates a passed condition and a LOW indicates a failed condition.

Bidirections:

T4:1 Test I/O Pins (input/output)
Under the control of OET, the four lower status bits (Z,C,N, and OVR) become outputs on T4:1, respectively, when OET goes HIGH. When OET is HIGH, the OET is LOW, T4:1 are used as inputs to generate the CT output.

Characteristics (All delay numbers are preliminary)

** The following AC timing are from CMOS10K technology.

A. Combinational Delays

Inputs	Y31:0	TO4:1	CT
I4:0 (Addr)	33.4	37.5	-
I15:0(Data)	23.6	29.0	-
I15:0(Instr)	31.6	35.7	22.8
DLE	24.2	28.0	-
TI4:1	-	-	9.1
CP	27.0	31.5	10.7
D15:0	23.8	27.6	-
IEN	-	-	11.2

All delays are nominal case with fanout=2

B. Setup and Hold Times

Inputs	With Respect To	High-to-Low Transition Setup	High-to-Low Transition Hold	Low-to-High Transition Setup	Low-to-High Transition Hold
I4:0(Addr)	CP	ts1 13.0	th1 0	-	-
I4:0(Addr)	CP IEN low	ts2 6.8	-	-	th7 0
I15:0(Data)	CP	-	-	ts8 29	th8 0
I15:0(Instr)	CP	ts3 11.4	th3 0	ts9 35	th9 0
I15:0(Instr)	IEN	ts16 8.7	th16 0	-	-
IEN high	CP	ts4 5.5	-	-	th10 0
IEN low	CP	ts5 3.0	th5 0	ts11 7.6	th11 0
SREN	CP	-	-	ts12 7.6	th12 0
D15:0	CP	-	-	ts13 25	th13 0
D15:0	DLE	ts6 2	th6 2	-	-
DLE	CP	-	-	-	th14 26

C. Clock and Pulse Requirements

Inputs	Min. LOW Time	Min. HIGH Time
CP	20	21
DLE	-	2
IEN	15	-

*** The following AC timing are from CMOS100K technology.

A. Combinational Delays

Inputs	Y31:0	TO4:1	CT
I4:0 (Addr)	26.5	28.9	-
I15:0(Data)	12.5	14.7	-
I15:0(Instr)	24.2	26.6	12.5
DLE	17.4	19.8	-
TI4:1	-	-	4.3
CP	17.6	20.0	15.7
D15:0	17.6	20.0	-
IEN	-	-	6.6

All delays are nominal case with fanout=2

B. Setup and Hold Times

Inputs	With Respect To	High-to-Low Transition Setup	High-to-Low Transition Hold	Low-to-High Transition Setup	Low-to-High Transition Hold
I4:0(Addr)	CP	ts1 10.0	th1 0	-	-
I4:0(Addr)	CP IEN low	ts2 8.0	-	-	th7 0
I15:0(Data)	CP	-	-	ts8 15.0	th8 0
I15:0(Instr)	CP	ts3 6.0	th3 0	ts9 27.0	th9 0
I15:0(Instr)	IEN	ts16 0	th16 0	-	-
IEN high	CP	ts4 0	-	-	th10 0
IEN low	CP	ts5 2.5	th5 0	ts11 5.0	th11 0
SREN	CP	-	-	ts12 4.4	th12 0
D15:0	CP	-	-	ts13 21	th13 0
D15:0	DLE	ts6 2	th6 2	-	-
DLE	CP	-	-	-	th14 22

ALL DELAYS ARE NOMINAL CASE WITH FANOUT=2

C. Clock and Pulse Requirements

Inputs	Min. LOW Time	Min. HIGH Time
CP	17	18
DLE	-	2
IEN	13	-

MACRO TO STANDARD PART I/O CONVERSION