

9-Line SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 6pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging
- -400mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation Drivers
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 3%
- Trimmed Impedance to 3%
- Negative Clamping on all Signal Lines
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5603 provides 9 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5603 provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors, and disables the regulator; greatly reducing standby power. The output channels remain high impedance even without Tempwr applied. A low channel capacitance of 6pF allows units at interim points of the bus to have little to no effect on the signal integrity.

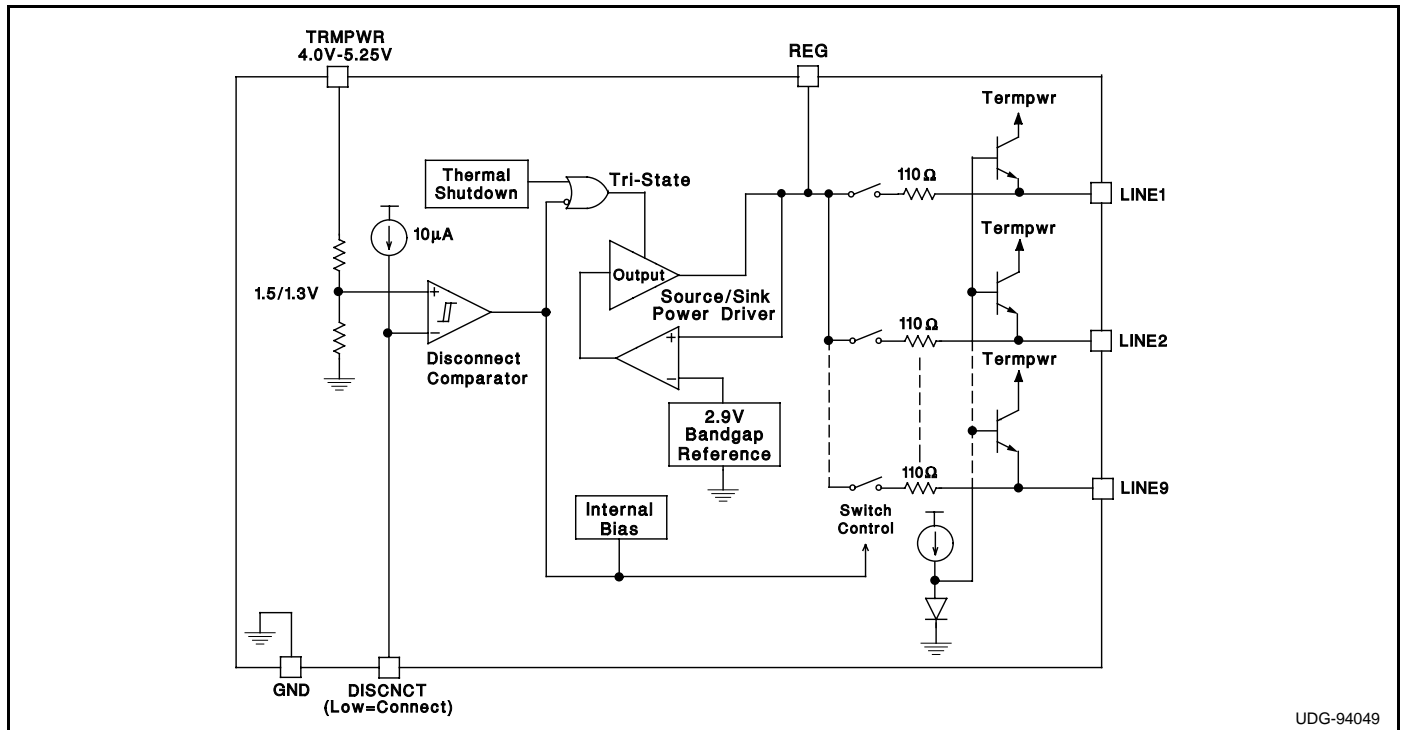
Functionally the UC5603 is similar to its predecessor, the UC5601 - 18 line Active Terminator. Several electrical enhancements were incorporated in the UC5603, such as a sink/source regulator output stage to accommodate all signal lines at +5V, while the regulator remains at its nominal value, reduced channel capacitance to 6pF typical, and as with the UC5601, custom power packages are utilized to allow normal operation at full power conditions (1.2 watts).

Internal circuit trimming is utilized, first to trim the impedance to a 3% tolerance, and then most importantly, to trim the output current to a 3% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include negative clamping on all signal lines to protect external circuitry from latch-up, thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Tempwr Voltage	+7V
Signal Line Voltage	0V to +7V
Regulator Output Current	0.5A
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	+300°C

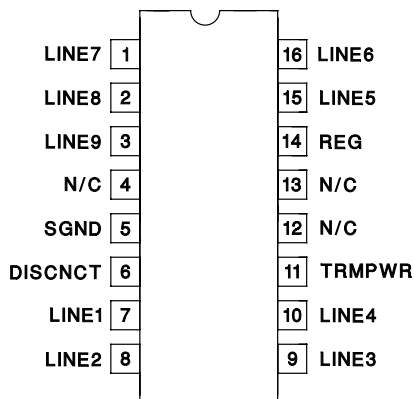
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
 Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

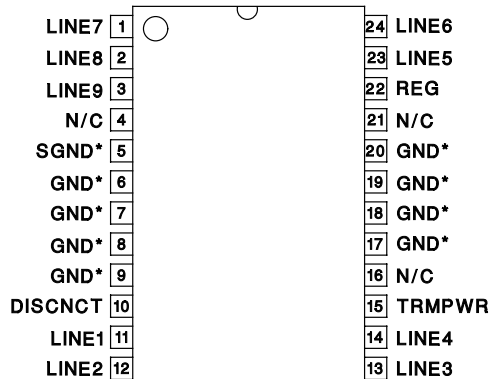
Tempwr Voltage	3.8V to 5.25V
Signal Line Voltage	0V to +5V
Disconnect Input Voltage	0V to Tempwr

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J Package

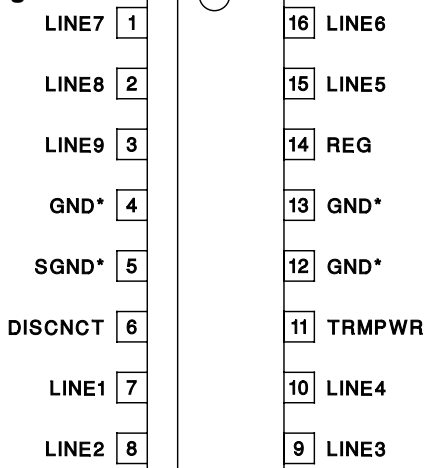


TSSOP-24 (Top View)
PWP Package



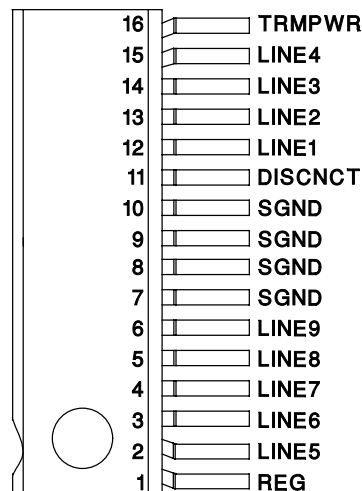
* PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.

SOIC-16 (Top View)
DP Package



* DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.

ZIP-16 (Top View)
Z Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = 0^\circ\text{C}$ to 70°C .
 $\text{TRMPWR} = 4.75\text{V}$ $\text{DISCNCT} = 0\text{V}$. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS		
Supply Current Section							
Tempwr Supply Current	All termination lines = Open		12	18	mA		
	All termination lines = 0.5V		200	220	mA		
Power Down Mode	DISCNCT = Open		100	150	μA		
Output Section (Terminator Lines)							
Terminator Impedance	$\Delta\text{LINE} = -5\text{mA}$ to -15mA	107	110	113	Ohms		
Output High Voltage	$\text{VTRMPWR} = 4\text{V}$ (Note 1)	2.7	2.9		V		
Max Output Current	$\text{VLINE} = 0.5\text{V}$	$T_J = 25^\circ\text{C}$	-21.1	-21.9	-22.4	mA	
		$0^\circ\text{C} < T_J < 70^\circ\text{C}$	-20.5	-21.9	-22.4	mA	
Max Output Current	$\text{VLINE} = 0.5\text{V}$, $\text{TRMPWR} = 4\text{V}$ (Note 1)	$T_J = 25^\circ\text{C}$	-20.3	-21.9	-22.4	mA	
		$0^\circ\text{C} < T_J < 70^\circ\text{C}$	-19.8	-21.9	-22.4	mA	
	$\text{VLINE} = 0.2\text{V}$, $\text{TRMPWR} = 4.0\text{V}$ to 5.25V	$0^\circ\text{C} < T_J < 70^\circ\text{C}$	-22.0	-24.0	-25.4	mA	
Output Clamp Level	$\text{ILINE} = -30\text{mA}$	-0.2	-0.05	0.1	V		
Output Leakage	DISCNCT = 4V	$\text{TRMPWR} = 0\text{V}$ to 5.25V $\text{REG} = 0\text{V}$	$\text{VLINE} = 0$ to 4V		10	400	nA
			$\text{VLINE} = 5.25\text{V}$			100	μA
		$\text{TRMPWR} = 0\text{V}$ to 5.25V , $\text{REG} = \text{Open}$ $\text{VLINE} = 0\text{V}$ to 5.25V		10	400	nA	
Output Capacitance	DISCNCT = Open (Note 2) (DP Package)		6	8	pF		
Regulator Section							
Regulator Output Voltage		2.8	2.9	3	V		
Regulator Output Voltage	All Termination Lines = 5V	2.8	2.9	3	V		
Line Regulation	$\text{TRMPWR} = 4\text{V}$ to 6V		10	20	mV		
Load Regulation	$\text{IREG} = +100\text{mA}$ to -100mA		20	50	mV		
Drop Out Voltage	All Termination Lines = 0.5V		0.7	1	V		
Short Circuit Current	$\text{VREG} = 0\text{V}$	-200	-400	-600	mA		
Sinking Current Capability	$\text{VREG} = 3.5\text{V}$	200	400	600	mA		
Thermal Shutdown			170		$^\circ\text{C}$		
Thermal Shutdown Hysteresis			10		$^\circ\text{C}$		
Disconnect Section							
Disconnect Threshold		1.3	1.5	1.7	V		
Threshold Hysteresis		100	160	250	mV		

Note 1: Measuring each termination line while other 8 are low (0.5V).

Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

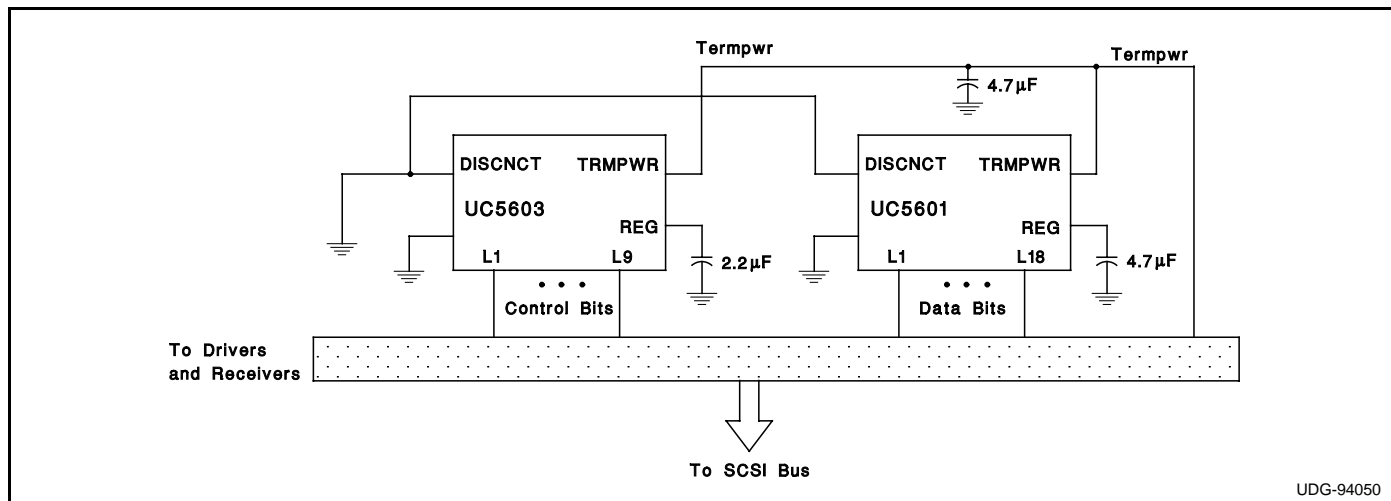


Figure 1: Typical Wide SCSI Bus Configurations Utilizing 1 UC5601 and 1 UC5603 Device

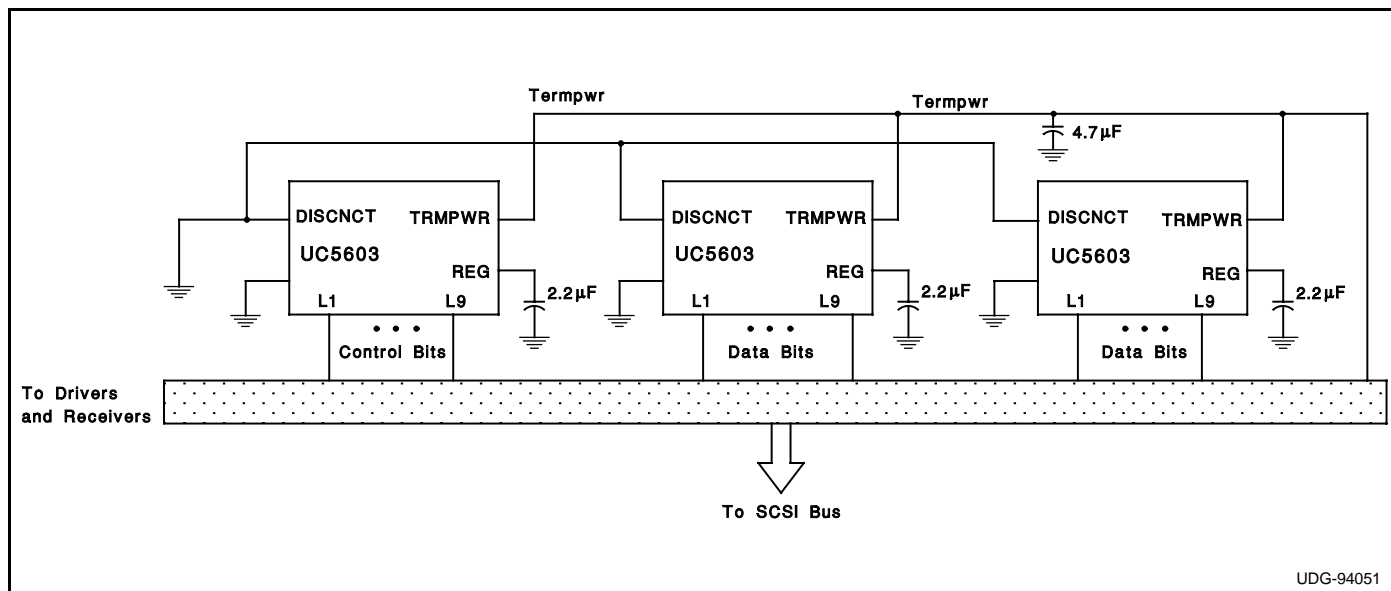


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5603 Devices.

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UC5603, 9-LINE 5V SE TERMINATOR FOR SCSI AND FAST SCSI

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Applications](#)

Parameter Name	UC5603
Number of Lines	9
Driver Types Supported	SE
TERMPWR Voltage (max) (V)	5.25
TERMPWR Voltage (min) (V)	4.0
Disconnect Active State	High
Integrated SPI-3 Mode Switching Filter/Delay	No
Process	Bi-Polar
Active Negation Support	Yes
Channel Capacitance (pF)	6
Resistor Tolerance (ppm)	50
Typical Sink Current (mA)	400
Current Tolerance (%)	3
Single-Ended Termination Impedance (ohms)	110
Single-Ended Tolerance (%)	3
Integrated TERMPWR Regulation	No

Description



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To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: [slus195.pdf](#) (255 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	DSCC Number	Availability / Samples
UC5603DP	<u>D</u>	16	0 TO 70	ACTIVE	3.52	1		Check stock or order
UC5603DPR	<u>D</u>	16	0 TO 70	ACTIVE	1.52	1		Check stock or order
UC5603DPRTR	<u>D</u>	16	0 TO 70	ACTIVE	1.60	1		Check stock or order
UC5603DPTR	<u>D</u>	16	0 TO 70	ACTIVE	3.10	1		Check stock or order

UC5603N	<u>N</u>	16	0 TO 70	ACTIVE	3.40	1		<u>Check stock or order</u>
UC5603QP	<u>FN</u>	28	0 TO 70	ACTIVE	5.53	1		<u>Check stock or order</u>
UC5603QPTR	<u>FN</u>	28	0 TO 70	ACTIVE	4.84	1		<u>Check stock or order</u>
UC5603Z	<u>SDZ</u>	16	0 TO 70	ACTIVE	3.53	1		<u>Check stock or order</u>

Application Reports

- [COMPARING BUS SOLUTIONS \(SLLA067 - Updated: 03/06/2000\)](#)
- [ELECTROSTATIC DISCHARGE APPLICATION NOTE \(SSYA008 - Updated: 05/05/1999\)](#)
- [JITTER ANALYSIS \(SLLA075 - Updated: 03/31/2000\)](#)
- [THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS \(SZZA017A - Updated: 09/10/1999\)](#)

Table Data Updated on: 8/16/2000