HD61604/HD61605
(Segment Type LCD Driver)

Description

The HD61604 and the HD61605 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microcomputers such as the HMCS6800 series.

Several types of liquid crystal displays can be connected to the HD61604 according to the applications because of the software-controlled liquid crystal dispay drive method.

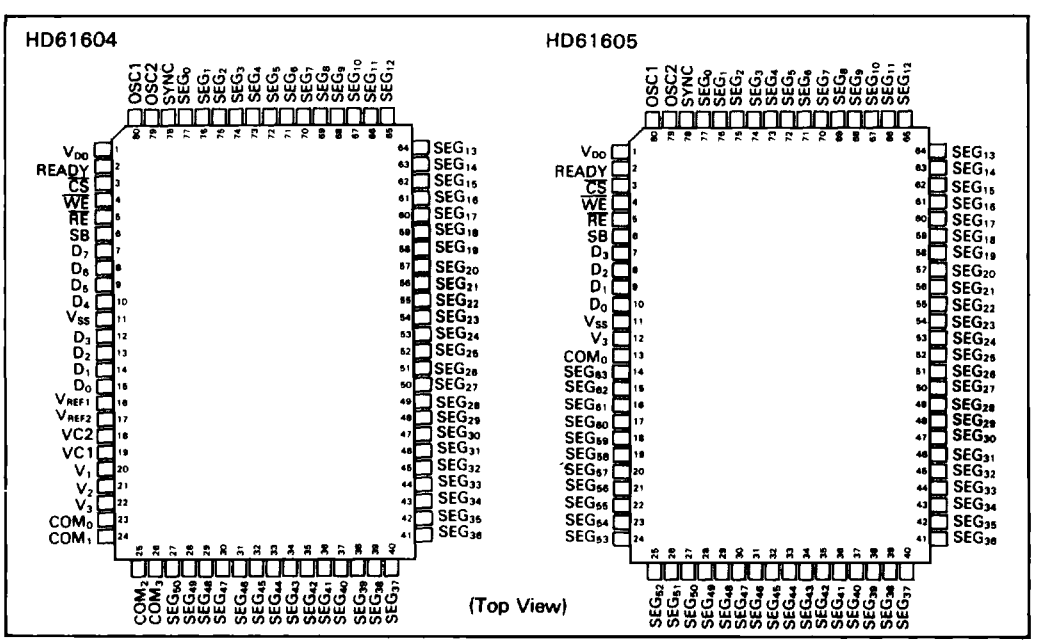
The HD61605 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Low current consumption
  - —Can drive from a battery power supply (100 μA max on 5 V).
  - —Standby input enables a standby operation at lower current consumption (5 μA max on 5 V).
- Versatile segment drive capacity

Type No.	Drive Method		Display Segments	Example of Use	Frame Freq (Hz) at fosc = 100 kHz
HD61604	Static		51	8 segments × 6 digits + 3 marks	98
	1/2 bias	1/2 duty	102	8 segments × 12 digits + 6 marks	195
	1/3 bias	1/3 duty	153	9 segments × 17 digits	521
		1/4 duty	204	8 segments × 25 digits + 4 marks	781
HD61605	Static		64	8 segments × 8 digits	98

Pin Arrangement



HITACHI
Hitachi America Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

SECTION 1

Block Diagram

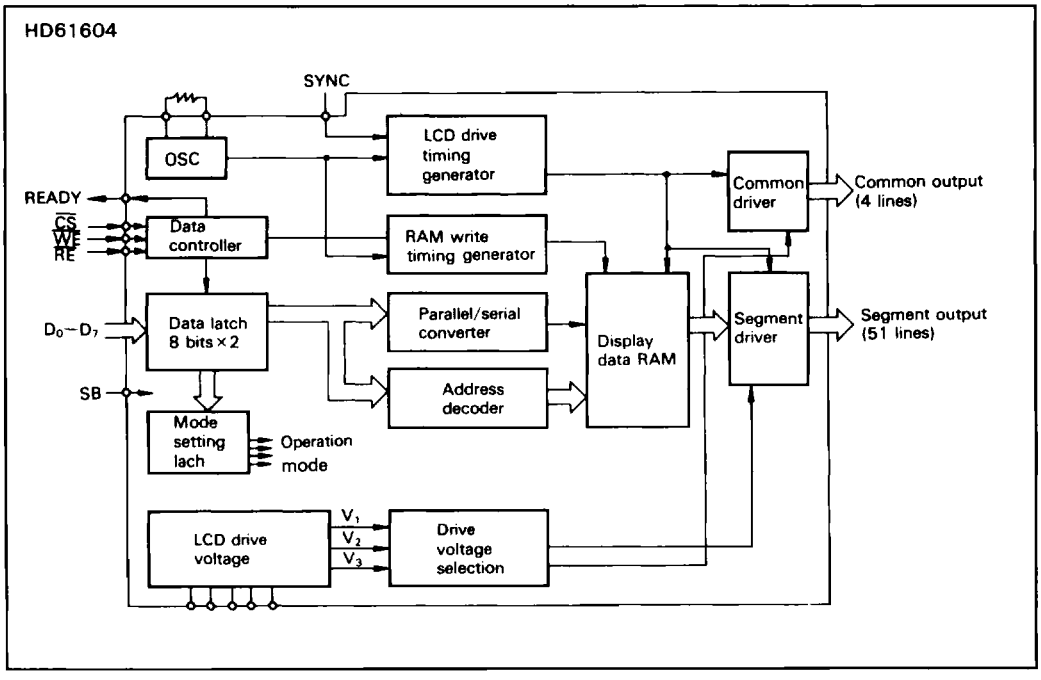


Figure 1. HD61604 Block Diagram

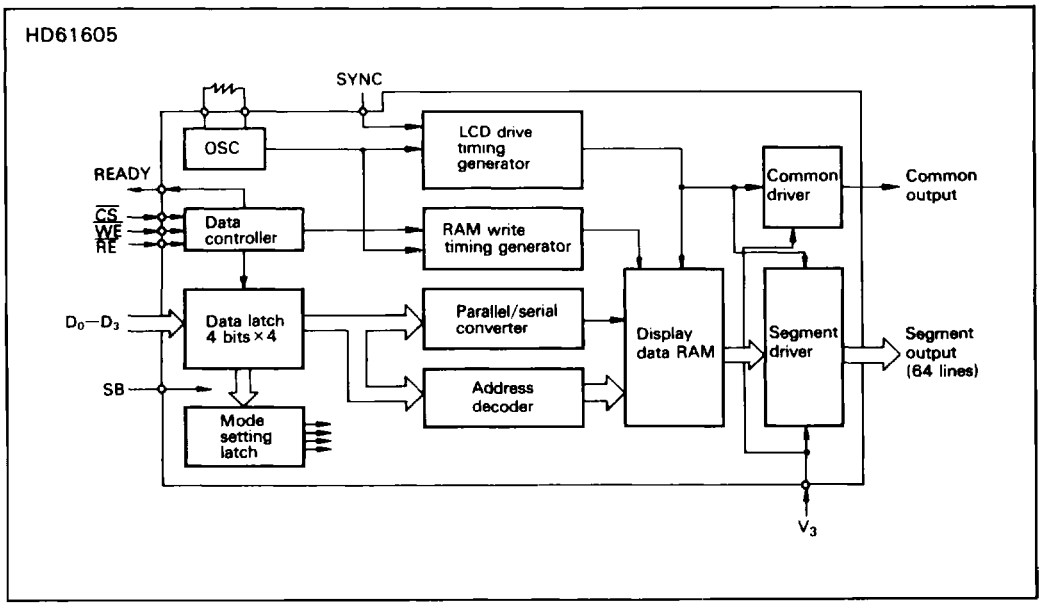


Figure 2. HD61605 Block Diagram

Pin Functions

Table 1 shows the HD61604 pin description. Table 2 shows the HD61605 pin description.

HD61604 Pin Function

READY (Ready): During setting data in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two types of modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_7 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.

SB (Standby): High level input stops the LSI operations.

(i) Stops oscillation and clock input.
(ii) Stops LCD driver.
(iii) Stops writing data into display RAM.

D_0-D_7 (Data Bus): Data input pin from which 8-bit × 2-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM_0-COM_3 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{50} (Segment): LCD segment drive output.

V_1, V_2, V_3 (LCD Voltage): Power supply for LCD drive.

OSC1, OSC2 (Oscillator): Attaches external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_{C1}, V_{C2}: Do not connect any wire.

V_{REF1}: Connect this pin to V1 pin.

V_{REF2}: Hold V_{DD} level.

V_{DD}: Positive power supply.

V_{SS}: Negative power supply.

HD61605 Pin Function

READY (Ready): During setting data in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two types of modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D_0 to D_3 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the first byte data.

SB (Standby): High level input stops the LSI operations.

(i) Stops oscillation and clock input.
(ii) Stops LCD driver.
(iii) Stops writing data into display RAM.

D_0-D_3: Data input pin from which 4-bit × 4 -byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM_0 (Common): LCD common (backplate) drive output.

SEG_0-SEG_{63} (Segment): LCD segment drive output.

OSC1, OSC2 (Oscillator): Attaches external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V_3 (LCD Voltage): Power supply input for LCD drive.

Voltage between V_{DD} and V_3 is used as drive voltage.

V_{SS}: Negative power supply.

HITACHI
Hitachi America Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

V_{DD}: Positive power supply.

Table 1. HD61604 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
$D_0 - D_7$	8	Input	MCU
SYNC	1	Input	MCU
$COM_0 - COM_3$	4	Output	LCD
$SEG_0 - SEG_{50}$	51	Output	LCD
V_1, V_2, V_3	3	Power supply	External R
OSC1, OSC2	2	Input, output	External R
V_{C1}, V_{C2}	2	Output	
V_{REF1}	1	Input	V_1
V_{REF2}	1	Input	V_{DD}
V_{DD}	1	Power supply	
V_{SS}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Table 2. HD61605 Pin Description

Pin Name	No.of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
$D_0 - D_3$	4	Input	MCU
SYNC	1	Input	MCU
COM_0[1]	Output	LCD	
$SEG_0 - SEG_{63}$	64	Output	LCD
OSC1, OSC2	2	Input, output	External R
V_3	1	Input	Power supply
V_{SS}	1	Power supply	
V_{DD}	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Display RAM

HD61604 Display RAM

The HD61604 has an internal display RAM shown in figure 3. Display data is stored in the RAM, or is read according to the LCD drive timing to display on the LCD. One bit of the RAM corresponds to the 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD drive modes.

Reading Data from HD61604 Display RAM

A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn pin.

A common address corresponds to the output timings of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

The following shows the correspondence between the 7-segment type LCD connection and the display RAM in each mode.

(1) **Static Drive:** In the static drive, only the column of COM_0 of display RAM is output. COM_1 to COM_3 are not displayed (figure 4).

(2) **1/2 Duty Drive:** In the 1/2 duty drive, the columns of COM_0 and COM_1 of display RAM are output in time sharing. The columns of COM_2 and COM_3 are not displayed (figure 5).

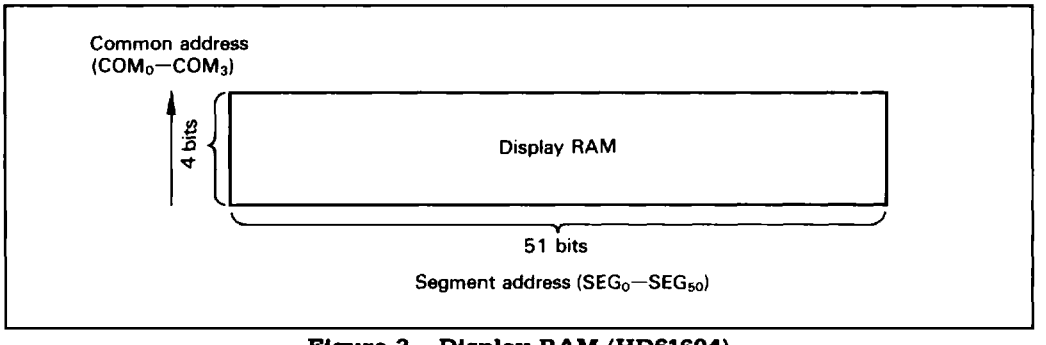


Figure 3. Display RAM (HD61604)

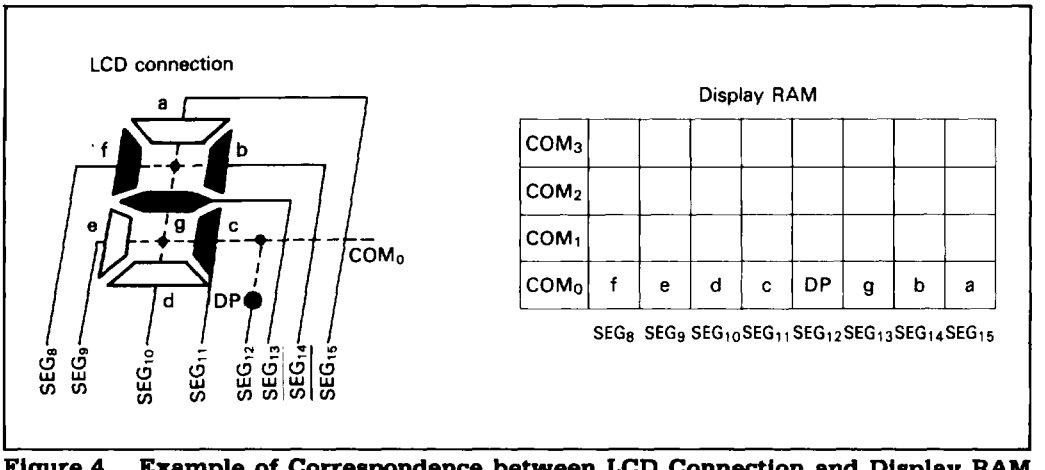


Figure 4. Example of Correspondence between LCD Connection and Display RAM (Static Drive, HD61604)

HITACHI
Hitachi America Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

(3) **1/3 Duty Drive:** In the 1/3 duty drive, the columns of COM_0 to COM_2 are output in time sharing. No column of COM_3 is displayed. "y" cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation in turning on/off the display of "y"(figure 6).

(4) **1/4 Duty Drive:** In the 1/4 duty drive, all the columns of COM_0 to COM_3 are displayed (figure 7).

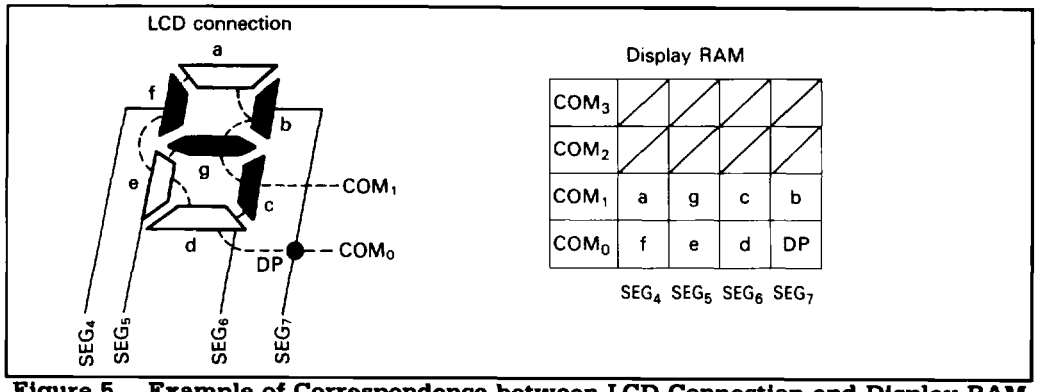


Figure 5. Example of Correspondence between LCD Connection and Display RAM (1/2 Duty, HD61604)

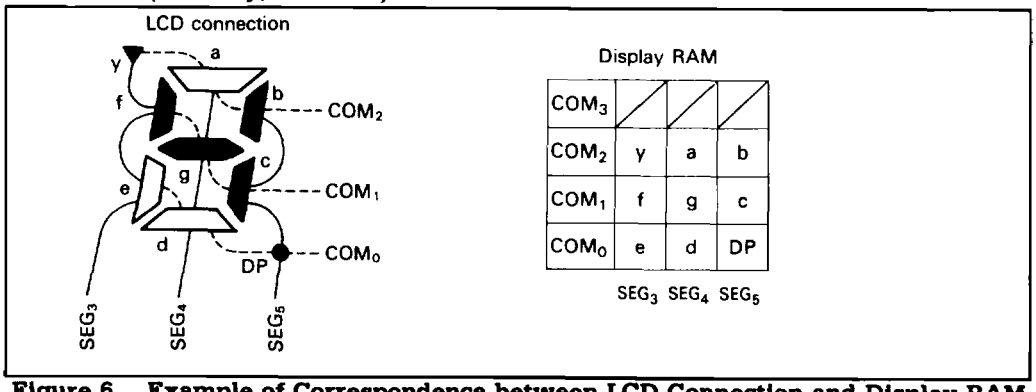


Figure 6. Example of Correspondence between LCD Connection and Display RAM (1/3 Duty, HD61604)

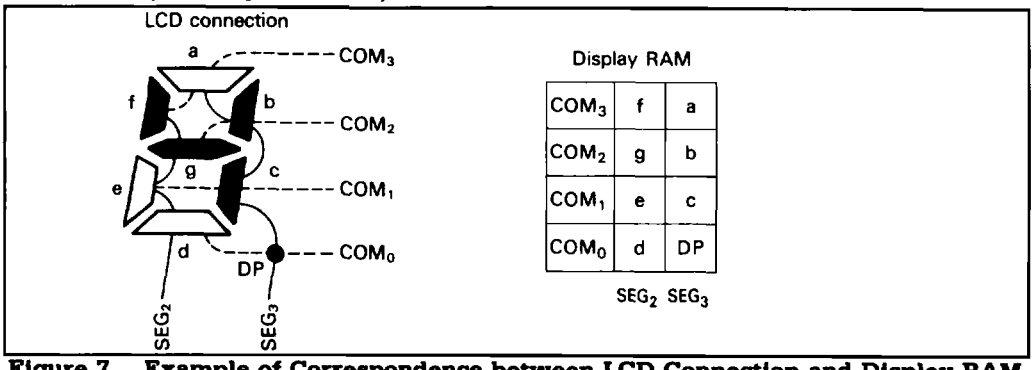


Figure 7. Example of Correspondence between LCD Connection and Display RAM (1/4 Duty, HD61604)

Writing Data into HD61604 Display RAM

Data is written into the display RAM in the following five methods:

(1) **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.

(2) **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

(3) **1/2 Duty Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty drive.

(4) **1/3 Duty Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty drive.

(5) **1/4 Duty Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the drive methods as described in the section of "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty drive methods. The digits are allocated as shown in figure 8.

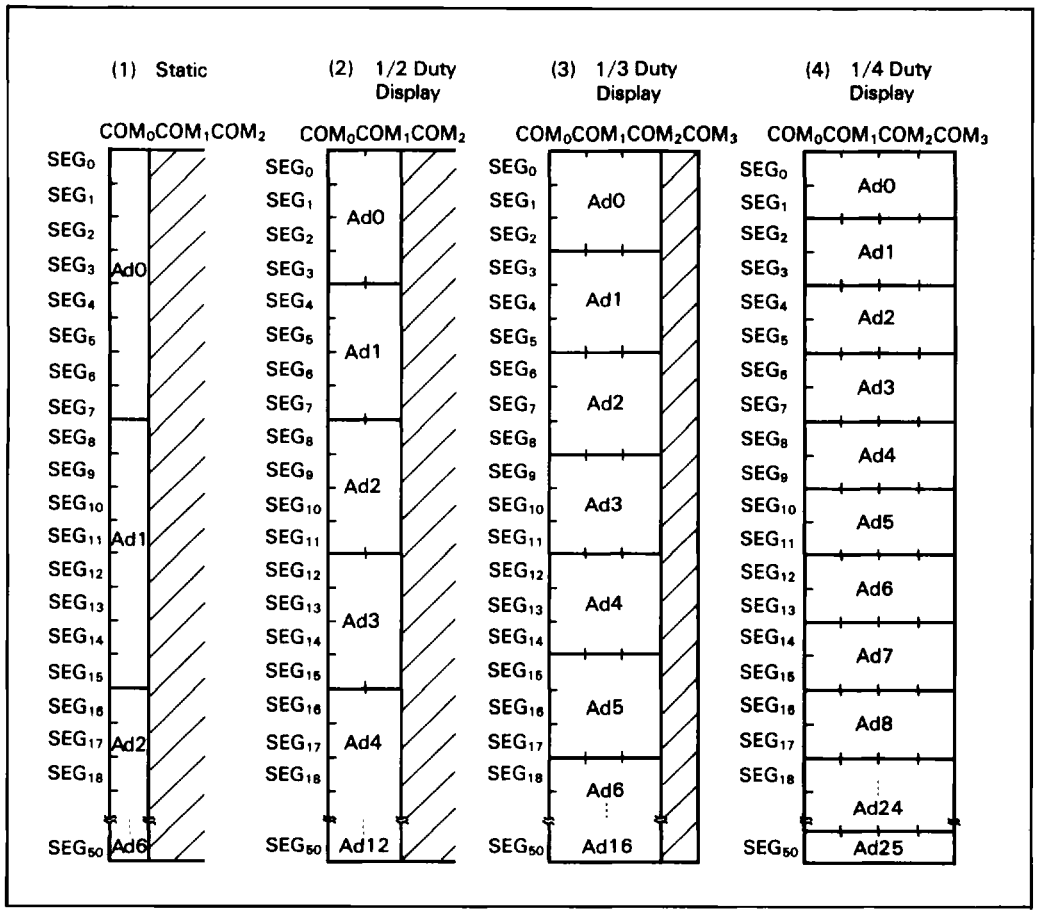


Figure 8. Allocation of Digit (HD61604)

As the data can be transferred on a digit basis from a microcomputer, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Figure 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Figure 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 of static, Ad12 of 1/2 duty, or Ad25 of 1/4 duty, display RAM does not have enough bits for the data. Thus the extra bits of the input 8-bit data are ignored.

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

HD61605 Display RAM

The HD61605 has an internal display RAM as shown in figure 10. Display data is stored in the RAM and output to the segment output pin.

(1) Static Display

	COM_0
SEG_8	Bit 7
SEG_{8n+1}	6
SEG_{8n+2}	5
SEG_{8n+3}	4
SEG_{8n+4}	3
SEG_{8n+5}	2
SEG_{8n+6}	1
SEG_{8n+7}	Bit 0

(2) 1/2 Duty Display

	COM_0	COM_1
SEG_{4n}	Bit 7	6
SEG_{4n+1}	5	4
SEG_{4n+2}	3	2
SEG_{4n+3}	1	Bit 0

(3) 1/3 Duty Display

	COM_0	COM_1	COM_2
SEG_{3n}	Bit 7	6	
SEG_{3n+1}	5	4	3
SEG_{3n+2}	2	1	Bit 0

(4) 1/4 Duty Display

	COM_0	COM_1	COM_2	COM_3
SEG_{2n}	Bit 7	6	5	4
SEG_{2n+1}	3	2	1	Bit 0

Figure 9. Bit Assignment in an Adn (HD61604)

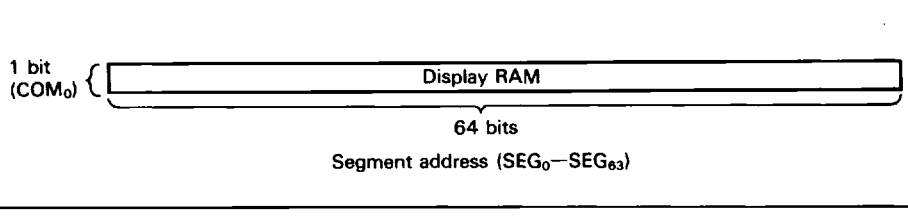


Figure 10. Display RAM (HD61605)

Reading Data from HD61605 Display RAM

Each bit of the display RAM corresponds to each LCD segment. The data at segment address SEGn is output to segment output SEGn pin. Figure 11 shows the correspondence between the 7-segment type LCD connection and the display RAM .

Writing Data into HD61605 Display RAM

Data is written into the display RAM in the following two methods:

(1) **Bit Manipulation:** Data is written into any bit of RAM on a bit basis.

(2) **Static Display Mode:** 8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in figure 12. When data is transferred from a microcomputer, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

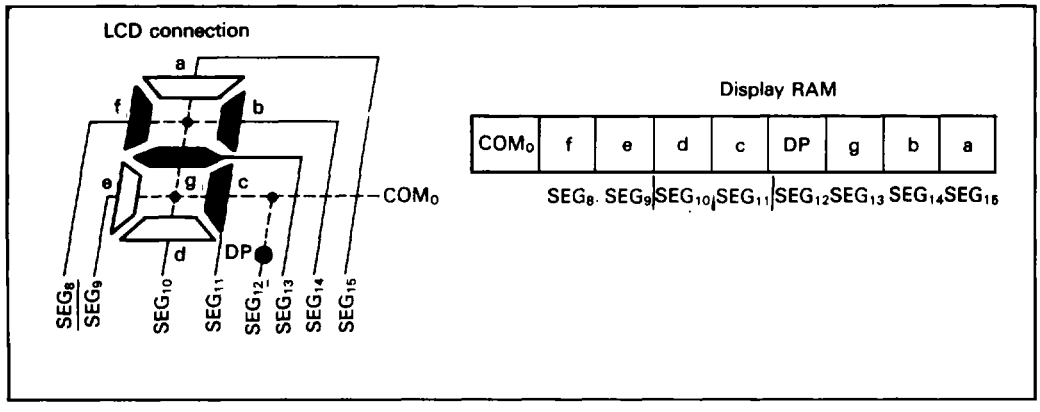


Figure 11. Example of Correspondence between LCD Connection and Display RAM (HD61605)

SECTION 1

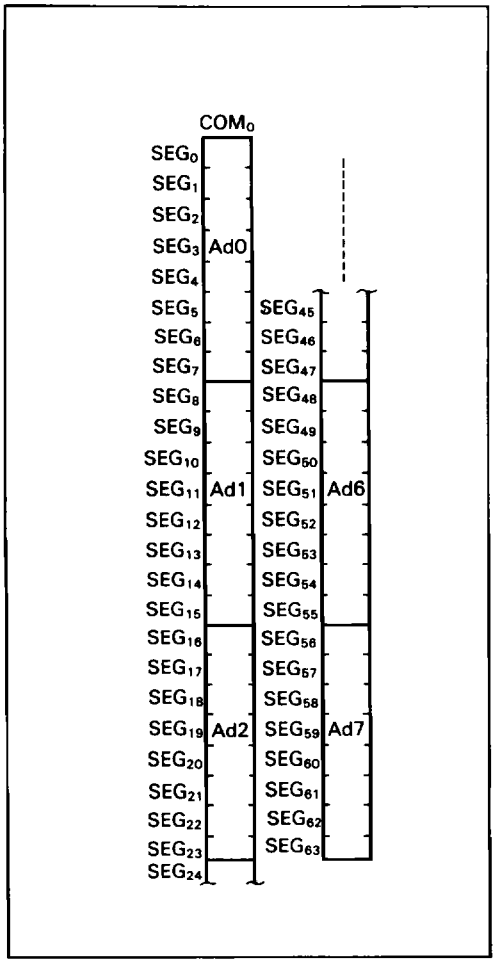


Figure 12. Allocation of Digit (HD61605)

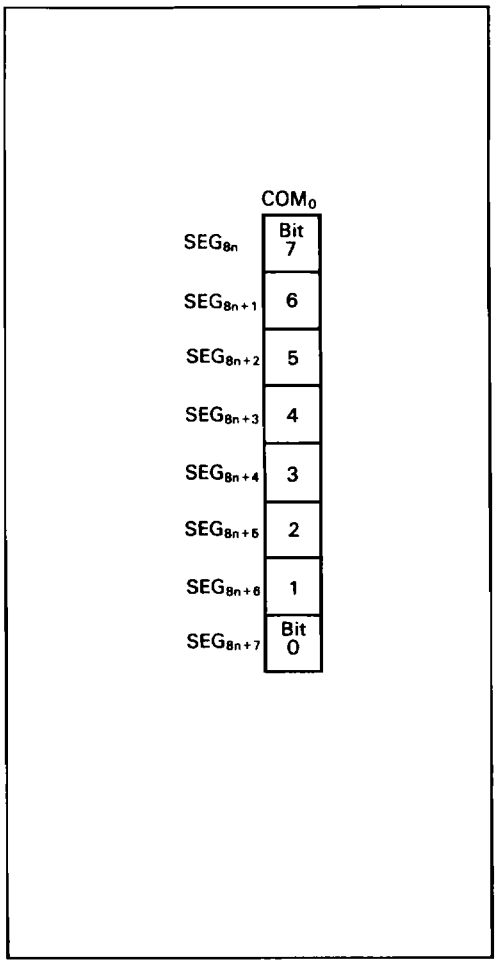


Figure 13. Bit Assignment in an Adn (HD 61605)

Operating Modes

HD61604 Operating Modes

The HD61604 has the following operating modes:

(1) **LCD Drive Mode:** Determines the LCD drive method.

- Static drive mode: LCD is driven statically.
- 1/2 duty drive mode: LCD is driven with 1/2 duty and 1/2 bias.
- 1/3 duty drive mode: LCD is driven with 1/3 duty and 1/3 bias.
- 1/4 duty drive mode: LCD is driven with 1/4 duty and 1/3 bias.

(2) **Data Display Mode:** Determines how to write display data into the data RAM.

- Static display mode: 8-bit data is written into the display RAM according to the digit in the static drive.
- 1/2 duty display mode: 8-bit data is written into the display RAM according to the digit in the 1/2 duty drive.
- 1/3 duty display mode: 8-bit data is written into the display RAM according to the digit in the 1/3 duty drive.
- 1/4 duty display mode: 8-bit data is written into the display RAM according to the digit in the 1/4 duty display drive.

(3) **READY Output Mode:** Determines the READY output timing.

After data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

- READY is always available (figure 14).
- READY is available by $\overline{CS}$ and $\overline{RE}$ (figure 15).

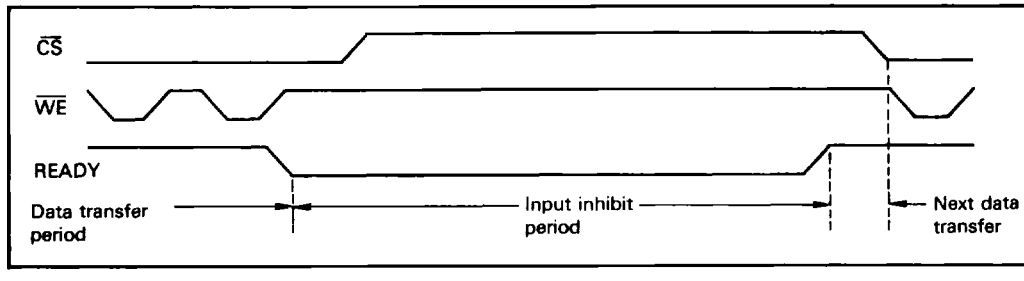


Figure 14. READY Output Timing (When It is Always Available)

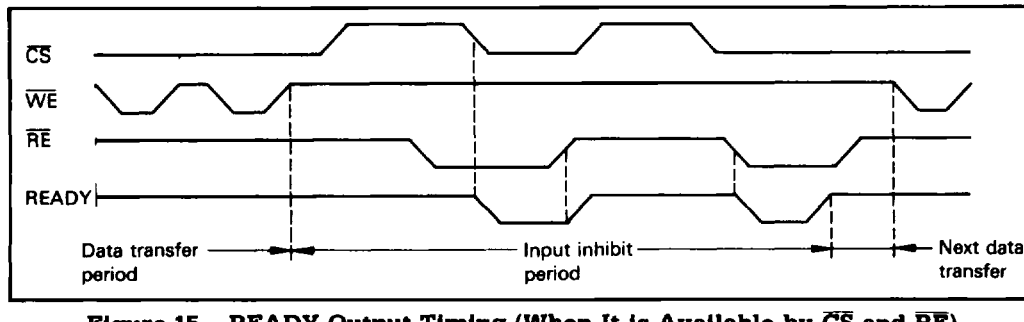


Figure 15. READY Output Timing (When It is Available by $\overline{CS}$ and $\overline{RE}$)

Hitachi America Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

(4) **LCD Off Mode:** In this mode, the HD61604 stops driving LCD and turns it off.

The above 4 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

HD61605 Operating Modes

The HD61605 has the following operating modes:

(1) **READY Output Mode:** Determines the READY output timing.

After data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

- READY is always available (figure 16).
- READY is available by $\overline{CS}$ and $\overline{RE}$ (figure 17).

(2) **LCD Off Mode:** In this mode, the HD61605 stops driving LCD and turns it off.

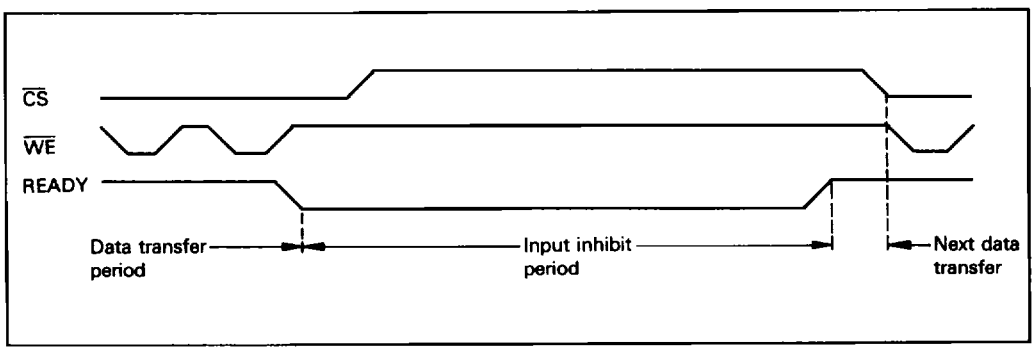


Figure 16. READY Output Timing (When It is Always Available)

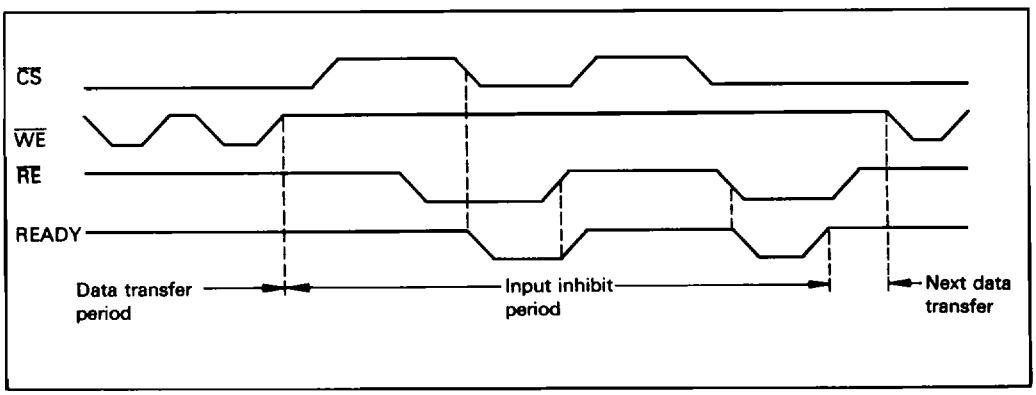


Figure 17. READY Output Timing (When It is Available by $\overline{CS}$ and $\overline{RE}$.)

Input Data Formats

HD61604 Input Data Formats

Input data is composed of 8 bits × 2 bytes. Input them as 2-byte data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

(1) **Display Data:** Updates display on an 8-segment basis.

1st byte

7	6	5	4	3	2	1	0
0	0	×	Display address (Digit address Adn)				

2nd byte

7	6	5	4	3	2	1	0
Display data							

- Display address: Digit address Adn in accordance with each display mode
- Display data: Pattern data written into the display RAM according to each display mode and the address

(2) **Bit Manipulation Data:** Updates display on a segment basis.

1st byte

7	6	5	4	3	2	1	0
0	1	Display data	×	×	×	COM address	

2nd byte

7	6	5	4	3	2	1	0
×	×	SEG address					

- Display data: Data written into 1 bit of the specified display RAM
- COM address: Common address of display RAM
- SEG address: Segment address of display RAM

(3) **Mode Setting Data:**

1st byte

7	6	5	4	3	2	1	0
1	0	×	0	1	READY bit	Drive mode bits	

2nd byte

7	6	5	4	3	2	1	0
×	×	×	×	×	OFF/ON bit	Display mode bits	

- Display mode bits:
  00: Static display mode
  01: 1/2 duty display mode
  10: 1/3 duty display mode
  11: 1/4 duty display mode
- OFF/ON bit:
  1: LCD off (It is set to 1 when SYNC is entered.)
  0: LCD on
- Drive mode bits:
  00: Static drive
  01: 1/2 duty drive
  10: 1/3 duty drive
  11: 1/4 duty drive
- READY bit:
  0: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (It is reset to 0 when SYNC is entered.) ···READY bus mode
  1: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$. ···READY port mode

Note: Input the same data to display mode bits and drive mode bits.

(4) **1-Byte Instruction:** The first data (first byte) is ignored when the bit 6 and bit 7 in the data are 1.

1st byte

7	6	5	4	3	2	1	0
1	1	×	×	×	×	×	×

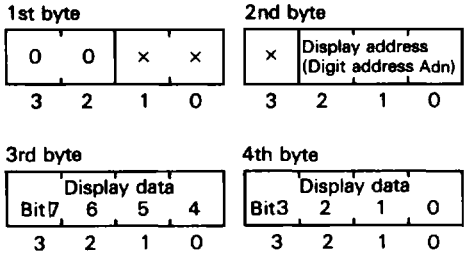
HITACHI
Hitachi America Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

SECTION 1

HD61605 Input Data Formats

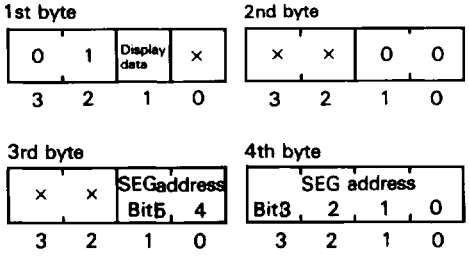
Input data is composed of 4 bits × 4 bytes. Input them as four 4-bit data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

(1) **Display Data:** Updates display on an 8-segment basis.



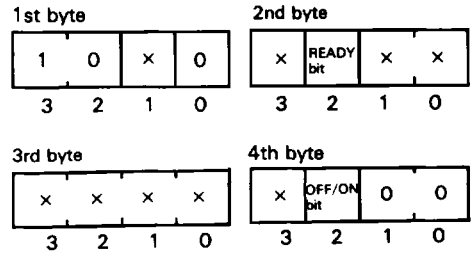
- Display address: Digit address Adn shown in figure 12.
- Display data: Pattern data written into the display RAM as shown in figure 13.

(2) **Bit Manipulation Data:** Updates display on a segment basis.



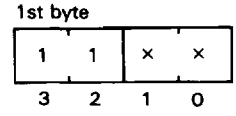
- Display data: Data written into the 1 bit of the specified display RAM.
- SEG address: Segment address of display RAM (segment output).

(3) **Mode Setting Data:**



- OFF/ON bit:
  1: LCD off (It is set to 1 when SYNC is entered.)
  0: LCD on
- READY bit:
  0: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0. (It is reset to 0 when SYNC is entered). ···READY bus mode
  1: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$. ···READY port mode

(4) **1-Byte Instruction:** The first data (4 bits) is ignored when the bit 3 and bit 2 in the data are 1.



How to Input Data

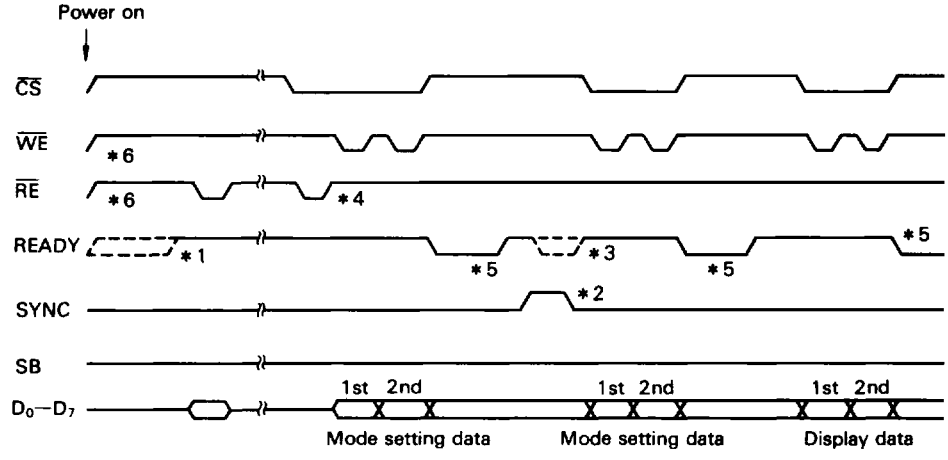
How to Input Data into HD61604

Input data is composed of 8 bits × 2 bytes. Take care that the data transfer is not interrupted because the first 8-bit data is distinguished from the second one depending on the sequence only.

When data transfer is interrupted, or at the power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

(1) Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes).
(2) Input 2 or more 1-byte instruction data whose bit 7 and 6 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$, D_0 to D_7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and figure 18.



*1: READY output is indefinite during 12 clocks after the oscillation starts when power on (clock: OSC2 clock).
*2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.
*3: In the mode in which READY is always available, READY output is indefinite while high is being appliad to SYNC.
*4: Reset the byte counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
*7: It is not always necessary to follow this example.

Figure 18. Example of Data Transfer Sequence

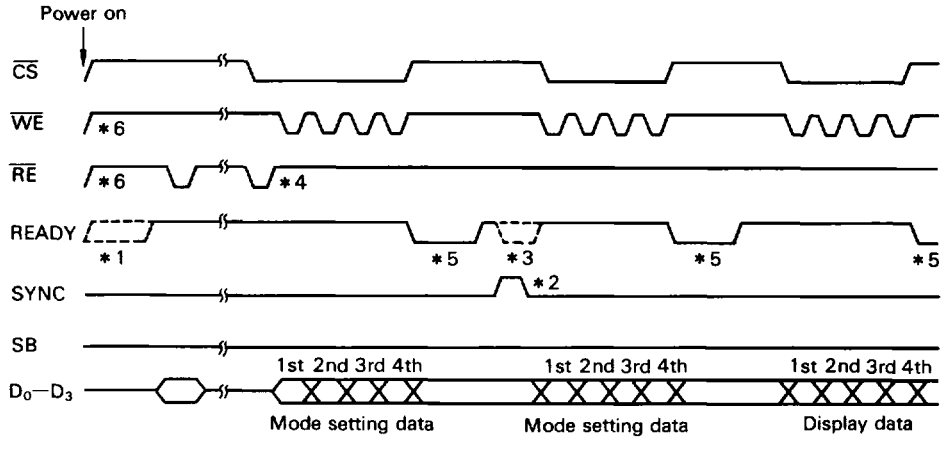
How to Input Data into HD61605

Input data is composed of 4 bits × 4 bytes. Take care that the data transfer is not interrupted because the first 4-bit data to the fourth 4-bit data are distinguished from each other depending on the sequence only.

When data transfer is interrupted, or at the power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

(1) Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes.)
(2) Input 4 or more 1-byte instruction data (4-bit data) whose bit 3 and 2 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$ D_0 to D_3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and figure 19.



*1: READY output is indefinite during 12 clocks after the oscillation starts when power on (clock: OSC2 clock).
*2: High pulse should be applied to SYNC pin when using two or more chips simultaneously.
*3: In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
*4: Reset the 4-bit data counter after power on.
*5: READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
*7: It is not always necessary to follow this example.

Figure 19. Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled untill the completion of mode setting.

There are two kinds of the READY output waveforms depending on the modes.

(1) READY bus mode (READY bit = 0)

(2) READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61604 and HD61605.

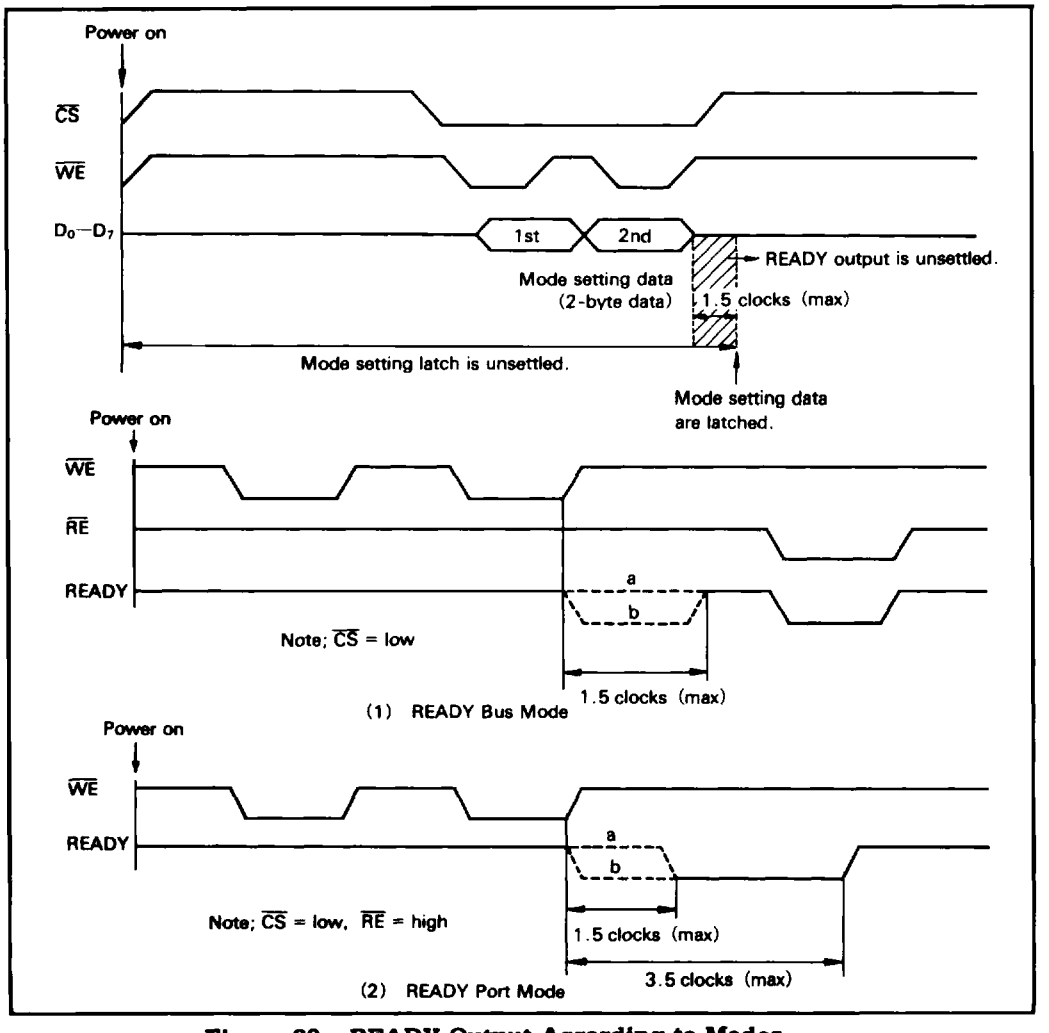


Figure 20. READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

(a) LCD driver is stopped (LCD is off).
(b) Display data and operating mode are held.
(c) The operation is suspended while changing display (= while READY is outputting low.) In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
(d) Oscillation is stopped.

When this mode is not used, connect pin SB to V_{SS}.

Multi-Chip Operation

When an LCD is driven with two or more chips, the driving timing of LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input causes the change of the mode setting data (The OFF/ON bit is set and the READY bit is reset. See (3) Mode Setting Data in "Input Data Formats".) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to V_{SS}.

In the case SB input is used, after standby mode is released, high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor ($\geq$ 1 μF) between V_{DD} and V_{SS} pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61604)

What is LCD Voltage?

HD61604 drives liquid crystal display using four levels of voltages; V_{DD}, V_1, V_2, and V_3 (V_{DD} is the highest and V_3 is the lowest). The voltage between V_{DD} and V_3 is called V_{LCD} and it is necessary to apply the appropriate V_{LCD} according to liquid crystal displays. V_3 always needs to be supplied power regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61604.

Connecting R2−R5 in series between V_{DD} and V_{SS} generates ΔV or V_{LCD} by using this resistance ratio to supply these voltage to pins V_1, V_2, V_3. C2−C4 are the capacitors for smoothing. Connect a trimmer potentiometer for R5 and change its resistance value to control the contrast.

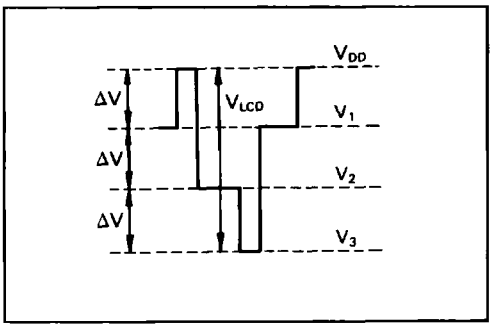
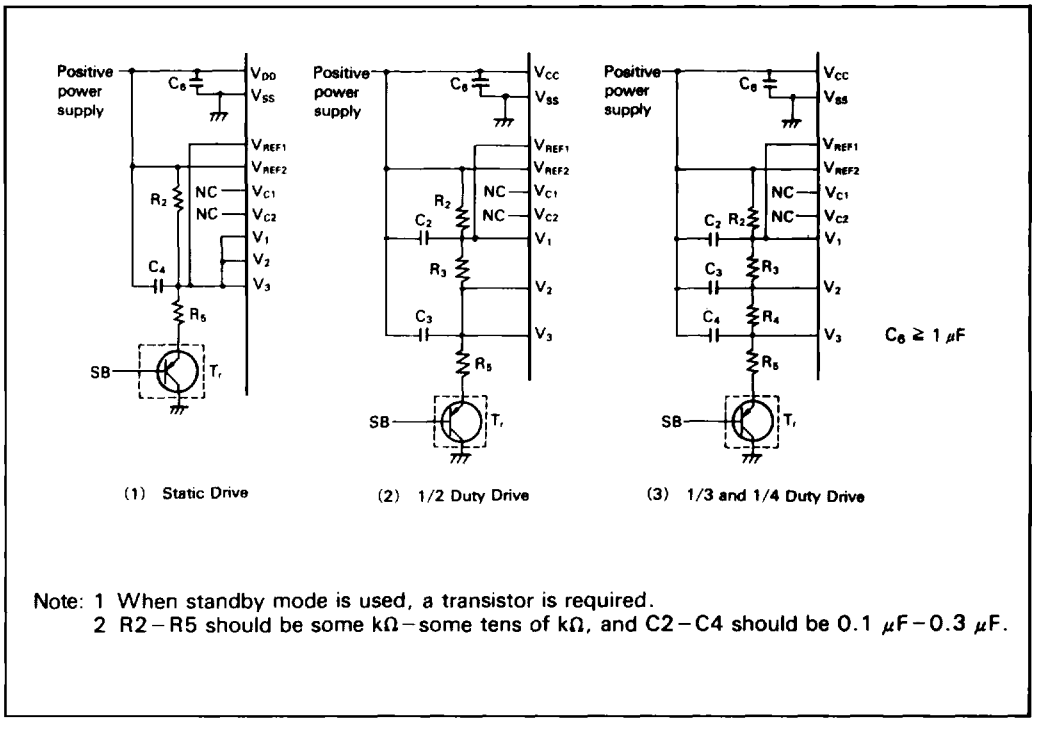


Figure 21. LCD Output Waveform and Output Levels (1/3 Duty, 1/3 Bias)



Note: 1 When standby mode is used, a transistor is required.
2 R2 – R5 should be some kΩ – some tens of kΩ, and C2 – C4 should be 0.1 μF – 0.3 μF.

Figure 22. Example when External Drive Voltage is Used

Liquid Crystal Display Drive Voltage (HD61605)

As shown in figure 23, apply LCD drive voltage from the external power supply.

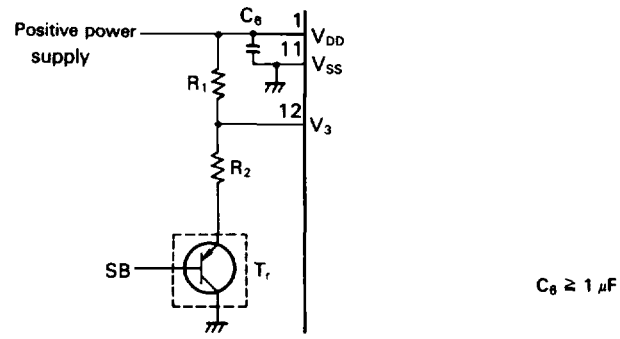
Oscillation Circuit

When Internal Oscillation Circuit is Used

When the internal oscillation circuit is used, attach an external resistor R_{OSC} as shown in figure 24. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC1 can be used for the input pin. In this case, open pin OSC2.



Note: When standby mode is used, a transistor is required.

Figure 23. Example of Drive Voltage Generator

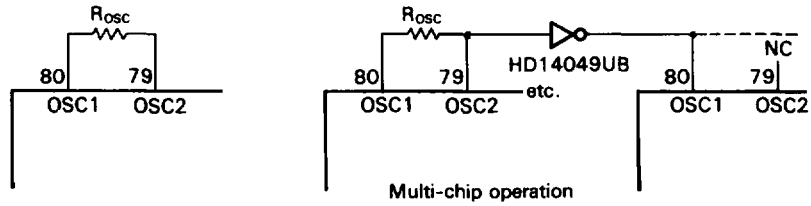


Figure 24. Example of Oscillation Circuit

Applications

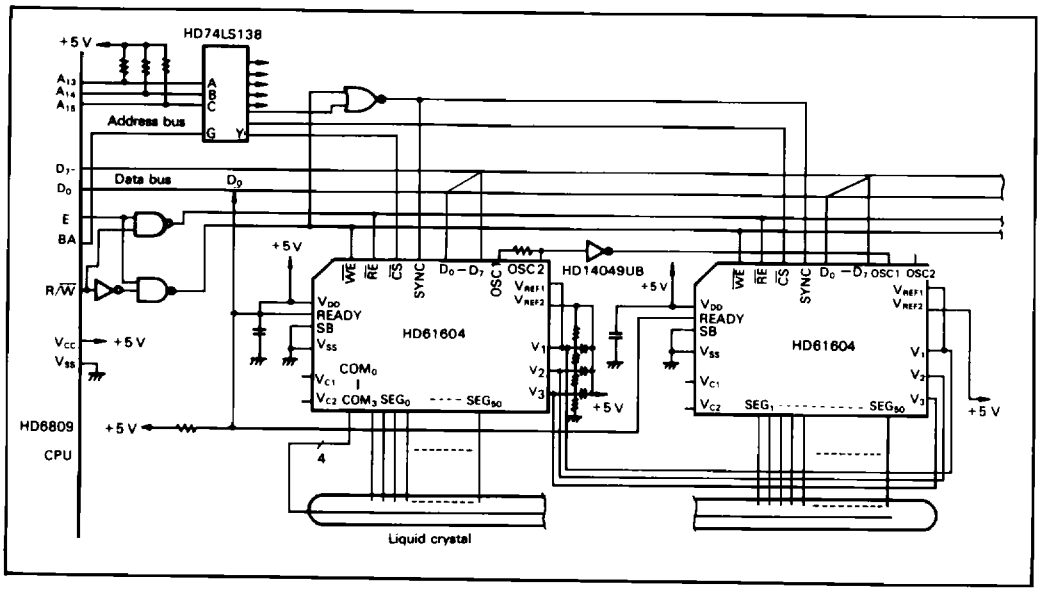


Figure 25. Example (1)

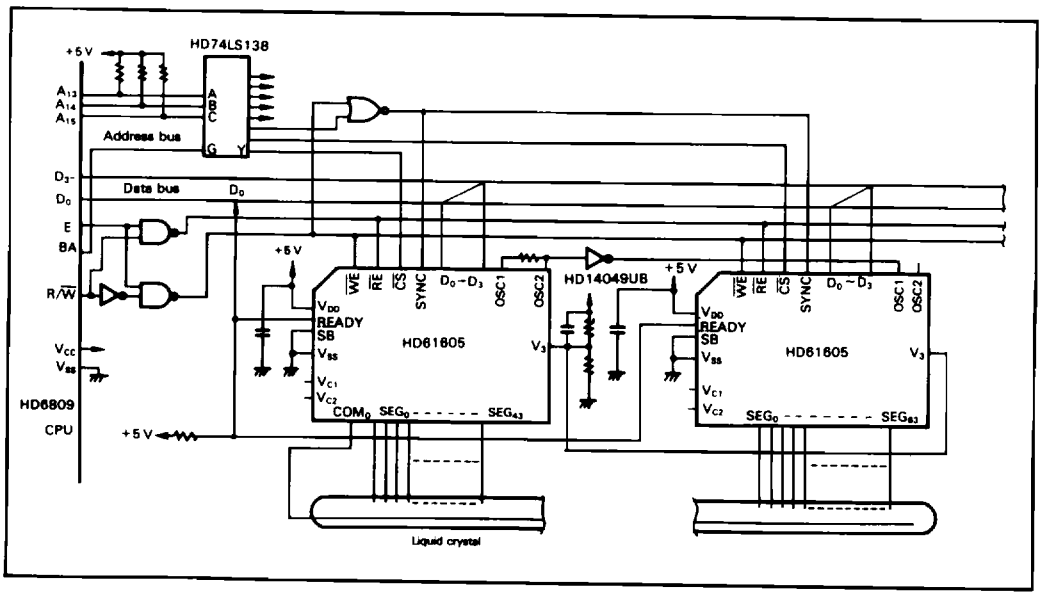


Figure 26. Example (2)

HITACHI
Hitachi America Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage*	V_{DD}, V_1, V_2, V_3	−0.3 to + 7.0	V
Pin voltage *	V_T	−0.3 to V_{DD} + 0.3	V
Operating temperature	Topr	−20 to +75	°C
Storage temperature	Tstg	−55 to +125	°C

*Value referred to V_{SS} = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

Item	Symbol	Limit			Unit
		Min	Typ	Max	
Power supply voltage*	V_{DD}	4.5	–	5.5	V
	V_1, V_2, V_3	0.3	–	V_{DD}	V
Pin voltage*	V_T	0	–	V_{DD}	V
Operating temperature	Topr	−20	–	+75	°C

*Value referred to V_{SS} = 0 V.

Electrical Characteristics

DC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta = −20 °C to +75 °C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Input high voltage	OSC1	V_{IH1}	0.8V_{DD}	–	V_{DD}	V	
	Others	V_{IH2}	2.0	–	V_{DD}	V	
Input low voltage	OSC1	V_{IL1}	0	–	0.2V_{DD}	V	
	Others	V_{IL2}	0	–	0.8	V	
Output leakage current	READY	I_{OH}	–	–	5	μA	Pull up the pin to V_{DD}
Output low voltage	READY	V_{OL}	–	–	0.4	V	I_{OL} = 0.4 mA
Input leakage current *1	Input pin	I_{IL1}	−1.0		1.0	μA	V_{IN} = 0 to V_{DD}
	V_1	I_{IL2}	−20	–	20	μA	V_{IN} = V_{DD} to V_3
	V_2, V_3	I_{IL3}	−5.0	–	5.0	μA	
LCD driver voltage drop	COM_0 – COM_3	V_{d1}	–	–	0.3	V	±Id = 3 μA for each COM, V_3 = V_{DD} to 3 V
	SEG_0 – SEG_{50}	V_{d2}	–	–	0.6	V	±Id = 3 μA for each SEG, V_3 = V_{DD} to 3 V
Current consumption *2		I_{DD}	–	–	100	μA	During display * R_{OSC} = 360 kΩ
		I_{DD}	–	–	5	μA	At standby

* Except the transfer operation of display data and bit data.
*1 V_1, V_2: applied only to HD61604.
*2 Do not connect any wire to the output pins and connect the input pins to V_{DD} or V_{SS}.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 V to 5.5 V, Ta = −20 °C to +75 °C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Oscillation frequency	OSC2	f_{OSC}	70	100	130	kHz	R_{OSC} = 360 kΩ
External clock frequency	OSC1	f_{OSC}	70	100	130	kHz	
External clock duty	OSC1	Duty	40	50	60	%	
I/O signal timing		t_S	400	–	–	ns	
		t_H	10	–	–	ns	
		t_{WH}	300	–	–	ns	
		t_{WL}	400	–	–	ns	
		t_{WR}	400	–	–	ns	
		t_{DL}	–	–	1.0	μs	Figure 31
		t_{EN}	400	–	–	ns	
		t_{OP1}	9.5	–	10.5	Clock	For display data transfer
		t_{OP2}	2.5	–	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	–	–	25	ns	

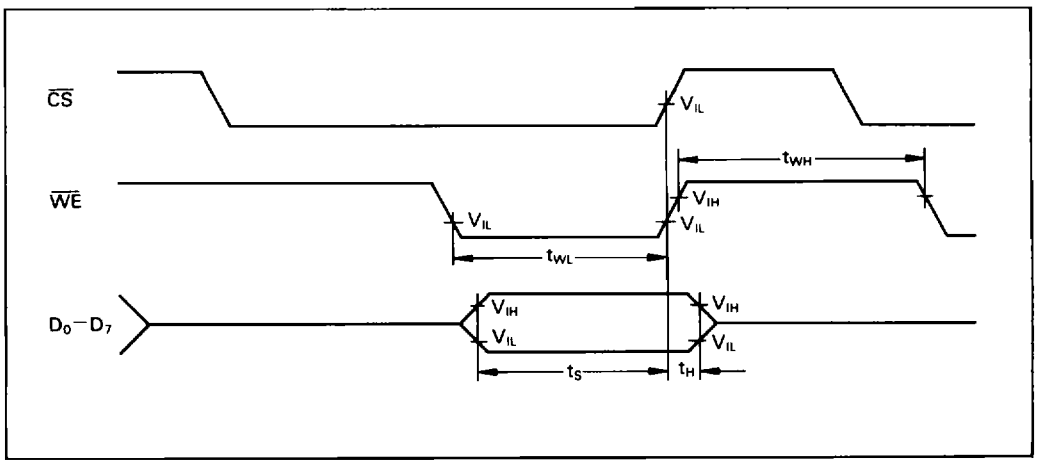


Figure 27. Write Timing ($\overline{RE}$ is fixed high and SYNC low)

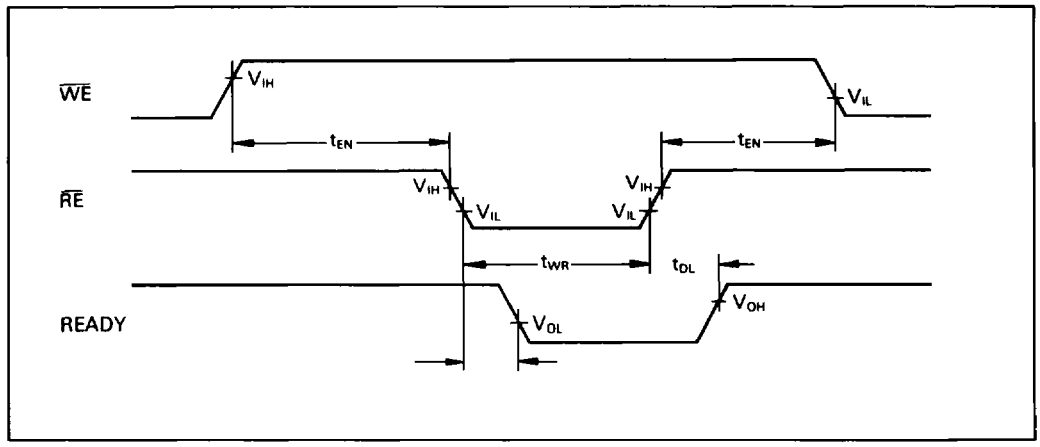


Figure 28. Reset/Read Timing ($\overline{CS}$ and SYNC are fixed low)

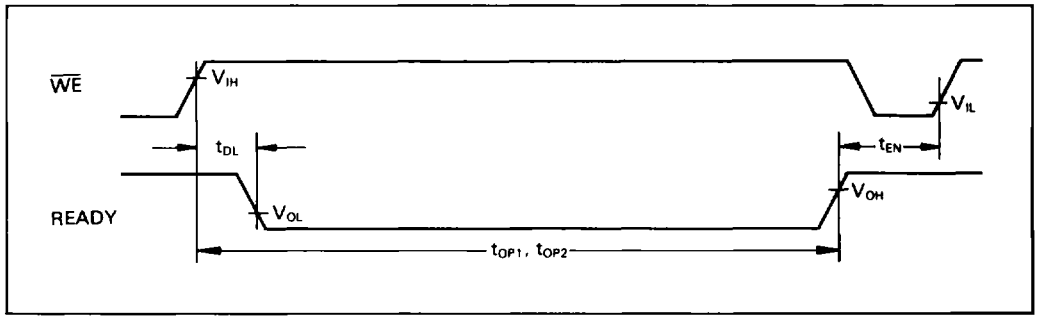


Figure 29. READY Timing (When the READY Output is Always Available)

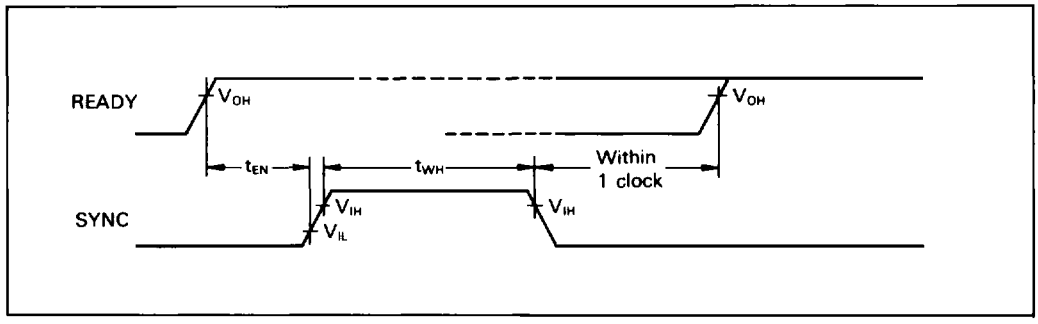


Figure 30. SYNC Timing

HITACHI
Hitachi America Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

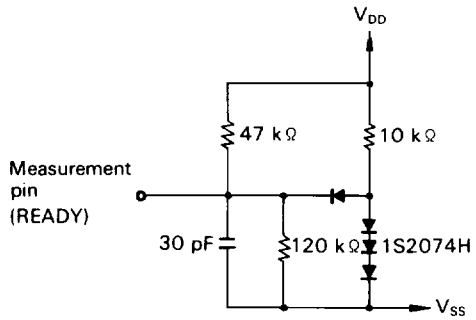


Figure 31. Bus Timing Load Circuit (LS-TTL Load)