PMI®

ADC-9012

CMOS MICROPROCESSOR-COMPATIBLE 12-BIT A/D CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- **Low Cost**
- **12-Bit Accurate**
  - **±1/2 LSB Nonlinearity Error Over Temperature**
  - **No Missing Codes at All Temperatures**
- **12 Microsecond Conversion Time**
- **Internal or External Clock**
- **Fast Bus Access and Disconnect Time**
  - **T_{ACC} = 90ns minimum**
  - **T_{DIS} = 75ns minimum**
- **8 or 16-Bit Data Bus Compatible**
- **Improved ESD Resistant Design**
- **Low 85mW Power Consumption**
- **Space Saving 24-Pin 0.3" DIP, or 24-Lead SOL**

APPLICATIONS

- **Data Acquisition Systems**
- **DSP System Front End**
- **Process Control Systems**
- **Portable Instrumentation**

ORDERING INFORMATION†

GAIN ERROR (LSB)	NON-LINEARITY (LSB)	MILITARY* TEMPERATURE −55°C to +125°C	INDUSTRIAL TEMPERATURE −40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1	±1/2	—	ADC9012EP	—
±4	±1/2	ADC9012BW	—	—
±4	±1/2	ADC9012BTC/883	—	—
±8	±1	—	ADC9012FW	—
±8	±1	—	ADC9012FP	ADC9012HP
±8	±1	—	ADC9012FS††	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

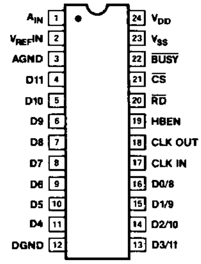
GENERAL DESCRIPTION

The ADC-9012 is a monolithic 12-bit accurate CMOS A/D converter. It contains a complete successive approximation A/D converter built with a high accuracy D/A converter, a precision bipolar transistor high-speed comparator, and successive approximation logic including three-state bus interface for logic compatibility. The accuracy of the ADC-9012 results from the addition of precision bipolar transistors in PMI's advanced-oxide isolated silicon-gate CMOS process. NPN transistors also provide excellent bus interface timing, 90ns access time, and 75ns bus disconnect time which results in faster data transfer without the need for wait states. An external 1MHz clock provides a 12μs conversion time.

In stand-alone applications an internal clock can be used with an external crystal.

An external negative five-volt reference sets the 0 to +10 volt input range. Plus five and minus 15 volt power supplies result in 85mW of total power consumption.

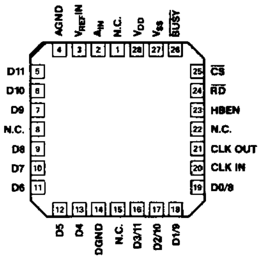
PIN CONNECTIONS



24-LEAD SOL (S-Suffix)

24-PIN 0.3" EPOXY DIP (P-Suffix)

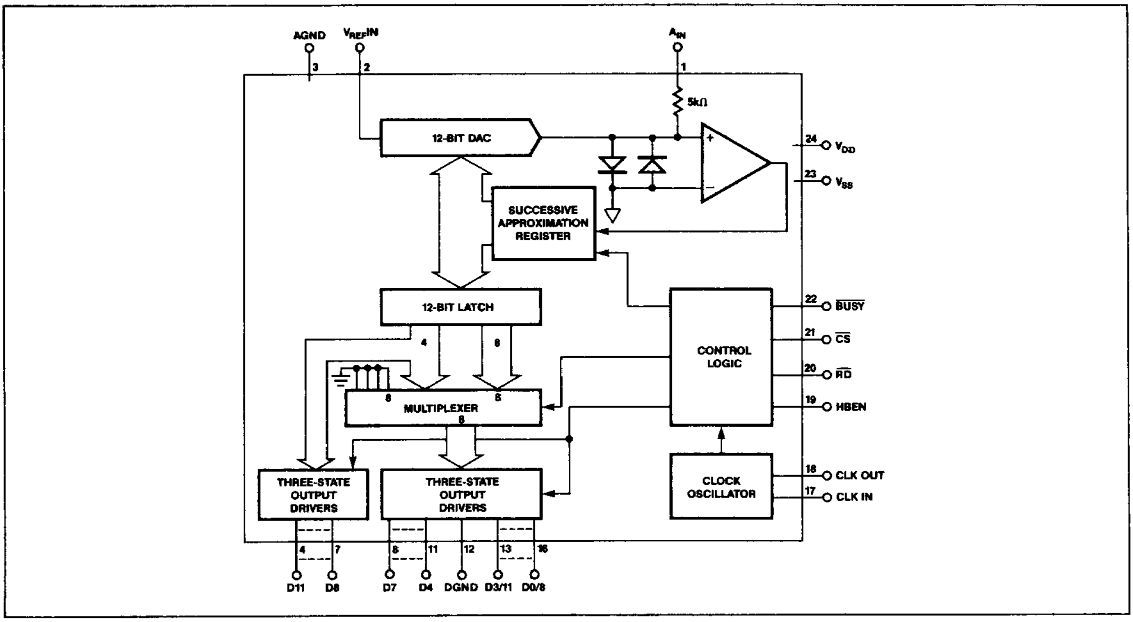
24-PIN 0.3" CERDIP (W-Suffix)



28-CONTACT LCC (T-Suffix)

This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = +25°C$ unless otherwise noted)

V_{DD} to DGND	−0.3V to +7V
V_{SS} to DGND	+0.3V to −17V
AGND to DGND	−0.3V, V_{DD} + 0.3V
A_{IN} to AGND	−15V to +15V
Digital Input Voltage to DGND	
Pins 17, 19–21	−0.3V, V_{DD} + 0.3V
Digital Output Voltage to DGND	
Pins 4–11, 13–16, 18, 22	−0.3V, V_{DD} + 0.3V
Operating Temperature Range	
HP	0 to +70°C
EP, FP, FW, FS	−40°C to +85°C
BW, BTC	−55°C to +125°C
Dice Junction Temperature	+150°C
Storage Temperature	−65°C to 150°C
Power Dissipation (Any Package) to +75°C	1,000mW
Derates above +75°C by	10mW/°C

CAUTION:

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{SS} = -12$ to $-15V$, $V_{REF} = -5V$, Analog Input 0 to +10V; $f_{CLK} = 1MHz$; $-40°C \leq T_A \leq +85°C$ for ADC-9012E/F, $0°C \leq T_A \leq +70°C$ for ADC-9012H, $-55°C \leq T_A \leq +125°C$ for ADC-9012B, unless otherwise noted. Specifications apply to Slow-Memory Mode.

PARAMETER	SYMBOL	CONDITIONS	ADC-9012 MIN	TYP	MAX	UNITS
Integral Nonlinearity	INL	B/E Grades F/H Grades	−1/2 −1	— —	+1/2 +1	LSB
Differential Nonlinearity	DNL		−1	—	+1	LSB
Offset Error	V_{ZSE}	E Grade B/F/H Grades	−1 −4	— —	+1 +4	LSB
Gain Error	G_{FSE}	E Grade B Grade F/H Grades	−1 −4 −8	— — —	+1 +4 +8	LSB

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{SS} = -12$ to $-15V$, $V_{REF} = -5V$, Analog Input 0 to +10V; $f_{CLK} = 1MHz$; $-40°C \leq T_A \leq +85°C$ for ADC-9012E/F, $0°C \leq T_A \leq +70°C$ for ADC-9012H, $-55°C \leq T_A \leq +125°C$ for ADC-9012B, unless otherwise noted. Specifications apply to Slow-Memory Mode. (Continued)

				ADC-9012		
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Full-Scale Tempco (Note 1)	TCG_{FS}	E Grade B/F/H Grades	— —	— —	+5 +10	ppm/°C
Input Voltage Range	V_{IN}		0	—	+10	V
Input Current Range	I_{IN}		0	—	+3	mA
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD} = \pm10\%$, $\Delta V_{SS} = \pm10\%$	—	1/2	1	LSB
Logic Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, HBEN	2.4	—	—	V
Logic Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, HBEN	—	—	0.8	V
Logic Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN	—	—	±1	μA
Digital Input Capacitance	C_{IN}	Digital Input, CS, RD, HBEN, CLK IN (Note 1)	—	—	10	pF
Logic Output High Voltage	V_{OH}	$I_{SOURCE} = 0.4mA$	3.5	—	—	V
Logic Output Low Voltage	V_{OL}	$I_{SINK} = 1.6mA$	—	—	0.4	V
Three-State Output Leakage	I_{OZ}	D11-D0/8	—	—	10	μA
Digital Output Capacitance	C_{OUT}	D11-D0/8 (Note 1)	—	—	15	pF
Positive Supply Current	I_{DD}	$V_{DD} = +5V$ (Note 2)	—	—	5	mA
Negative Supply Current	I_{SS}	$V_{SS} = -12V$ (Note 2)	—	—	5	mA
Power Consumption	P_{diss}	$V_{DD} = +5V$, $V_{SS} = -12V$ (Note 2)	—	—	85	mW
Conversion Time	T_c	$f_{CLK} = 1MHz$ (Note 6) Synchronous Clock Asynchronous Clock	 — 12	 — —	 12.5 13.5	μs
TIMING CHARACTERISTICS (Notes 1, 3)						
CS to RD Set-up Time	t_1		0	—	—	ns
RD to BUSY Propagation Delay	t_2	$T_A = +25°C$ T_A = Full Temperature Range E/F/H Grades B Grade	— — —	— — —	190 230 270	ns
Data Access Time After RD	t_3	(Note 4) $C_L = 20pF$ $C_L = 100pF$	— —	— —	90 125	ns
Read Pulse Width	t_4	$C_L = 20pF$ $C_L = 100pF$	— —	— —	90 125	ns
CS to RD Hold Time	t_5		0	—	—	ns
Data Set-up Time After BUSY	t_6	(Note 4)	—	—	70	ns
Bus Disconnect Time	t_7	(Note 5)	20	—	75	ns
HBEN to RD Set-up Time	t_8		0	—	—	ns
HBEN to RD Hold Time	t_9		0	—	—	ns
Delay Between Successive Read Operations	t_{10}		500	—	—	ns

NOTES:

1. Guaranteed by design.
2. Converter inactive; $\overline{CS}$, $\overline{RD}$ = HIGH, $A_{IN} = +10V$.
3. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of 1.6V.
4. t_3 and t_6 are measured with the load circuits of Figure 1 and timed for an output to cross 0.8V or 2.4V.
5. t_7 is the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
6. See Synchronizing Start Conversion information in Converter Operation Details.

FIGURE 1: Load Circuits for Access Time

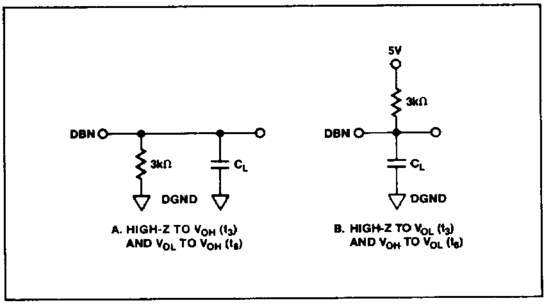


FIGURE 2: Load Circuits for Output Float Delay

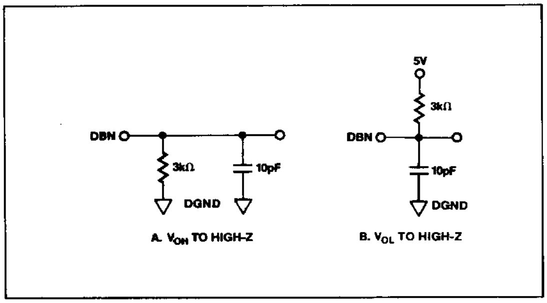


TABLE 1: Pin Function Description

PIN	MNEMONIC	DESCRIPTION
1	A_{IN}	Analog Input. 0 to +10 volts.
2	V_{REF}IN	Voltage Reference Input. Requires external −5 volt reference.
3	AGND	Analog Ground
4...11	D11...D4	Three State data outputs become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
13...16	D3/11...D0/8	Individual pin function is dependent upon High Byte Enable (HBEN) input.

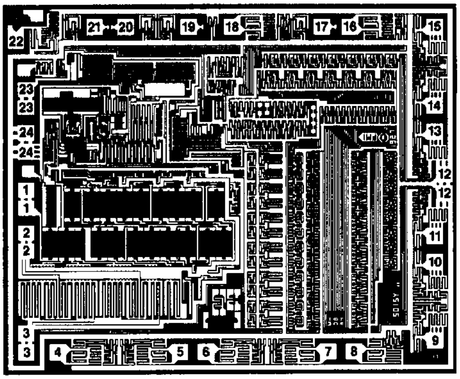
DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

NOTES:
*D11...D0/8 are the ADC data output pins.
DB11...DB0 are the 12-bit conversion results, DB11 is the MSB.

PIN	MNEMONIC	DESCRIPTION
12	DGND	Digital Ground
17	CLK IN	Clock Input pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description for crystal (resonator).
19	HBEN	High Byte Enable input. Its primary function is to multiplex the 12 bits of conversion data onto the lower D7...D0/8 outputs (4 MSBs or 8 LSBs). See Pin description 4...11 and 13...16. Also disables conversion start when HBEN is high.
20	$\overline{RD}$	READ input. This active LOW signal, in conjunction with $\overline{CS}$ is used to enable the output data three-state drivers and initiates a conversion if $\overline{CS}$ and HBEN are low.
21	$\overline{CS}$	CHIP SELECT input. This active LOW signal, in conjunction with $\overline{RD}$ is used to enable the output data three-state drivers and initiates a conversion if $\overline{RD}$ and HBEN are low.
22	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
23	V_{SS}	Negative Supply, −15V.
24	V_{DD}	Positive Supply, +5V.

DICE CHARACTERISTICS



DIE SIZE 0.122 × 0.148 inch, 18,056 sq. mils
(3.098 × 3.759 mm, 11.65 sq. mm)

1. A_{IN}
2. V_{REF} IN
3. AGND
4. D11
5. D10
6. D9
7. D8
8. D7
9. D6
10. D5
11. D4
12. DGND
13. D3/11
14. D2/10
15. D1/9
16. D0/8
17. CLK IN
18. CLK OUT
19. $\overline{HBEN}$
20. $\overline{RD}$
21. $\overline{CS}$
22. $\overline{BUSY}$
23. V_{SS}
24. V_{DD} (Substrate)

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +5V$, $V_{SS} = -12V$ to $-15V$, $V_{REF} = -5V$, $A_{IN} = 0V$ to $+10V$, and $T_A = +25°C$, unless otherwise noted.

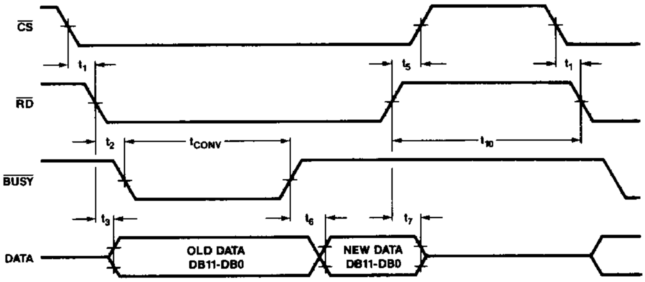
PARAMETER	SYMBOL	CONDITIONS	ADC-9012G LIMIT	UNITS
Integral Nonlinearity	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Offset Error	V_{ZSE}		±8	LSB MAX
Gain Error	G_{FSE}		±8	LSB MAX
Analog Input Resistance	R_{AIN}		4/6	KΩ MIN/MAX
Logic Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, HBEN	2.4	V MIN
Logic Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, HBEN	0.8	V MAX
Logic Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN	±1	μA MAX
Logic Output High Voltage	V_{OH}	$I_{SOURCE} = 0.4mA$	3.5	V MIN
Logic Output Low Voltage	V_{OL}	$I_{SINK} = 1.6mA$	0.4	V MAX
Positive Supply Current	I_{DD}	$V_{DD} = +5V$ (Note 1)	5	mA MAX
Negative Supply Current	I_{SS}	$V_{SS} = -12V$ (Note 1)	5	mA MAX

NOTES:

1. Converter inactive $\overline{CS} = \overline{RD} = HBEN =$ Logic HIGH, $A_{IN} = +10V$.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

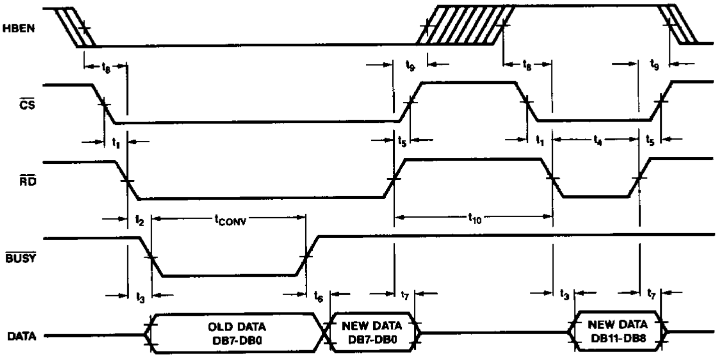
FIGURE 3: Parallel Read Timing Diagram, Slow-Memory Mode (HBEN = LOW)



SLOW-MEMORY MODE, PARALLEL READ DATA BUS STATUS

ADC-9012 DATA OUTPUTS	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
READ	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

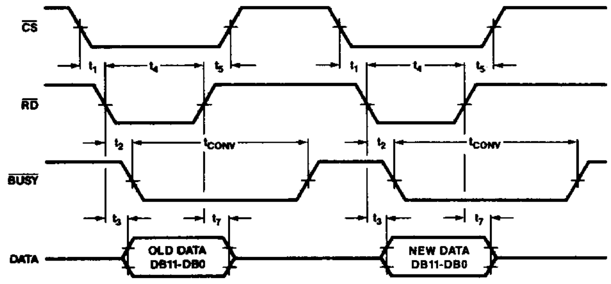
FIGURE 4: Two-Byte Read Timing Diagram, Slow-Memory Mode



SLOW-MEMORY MODE, TWO-BYTE READ DATA BUS STATUS

ADC-9012 DATA OUTPUTS	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
FIRST READ	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SECOND READ	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

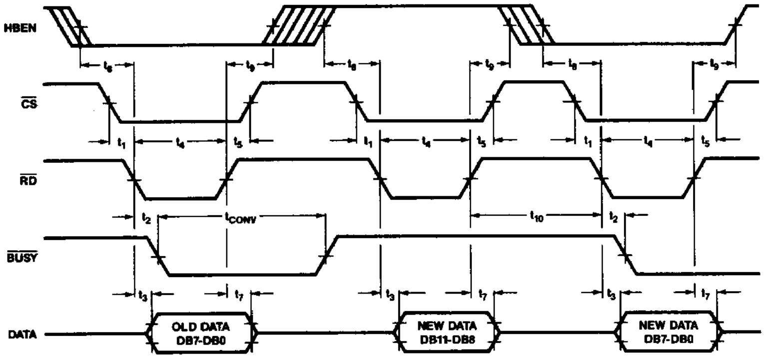
FIGURE 5: Parallel Read Timing Diagram, ROM Mode (HBEN = LOW)



ROM MODE, PARALLEL READ DATA BUS STATUS

ADC-9012 DATA OUTPUTS	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
FIRST READ (OLD DATA)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SECOND READ	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

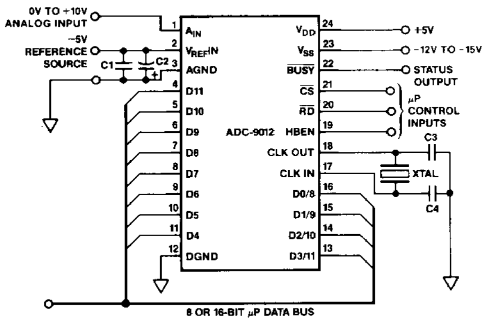
FIGURE 6: Two-Byte Read Timing Diagram, ROM Mode



ROM MODE, TWO-BYTE READ DATA BUS STATUS

ADC-9012 DATA OUTPUTS	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
FIRST READ (OLD DATA)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SECOND READ	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
THIRD READ	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

FIGURE 7: Basic Connection Diagram



XTAL = 1MHz C1 = 0.1µF C2 = 47µF
C3, C4 = 30 TO 100pF DEPENDING ON XTAL CHOSEN

CONVERTER OPERATION DETAILS

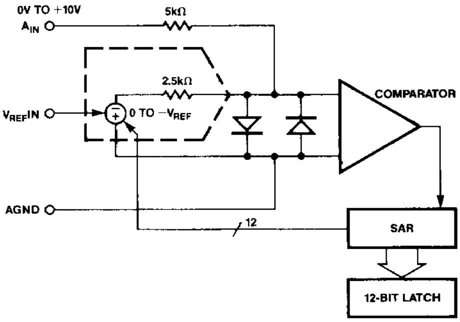
The CS, RD and HBEN digital inputs control the start of conversion. A high-to-low transition on both CS and RD initiate a conversion sequence. The HBEN high-byte-enable input must be low or coincident with the read RD input edge. The start of conversion resets the internal successive approximation register (SAR) and enables the three-state outputs. See Figure 8. The busy line is active low during the conversion process.

During conversion, the SAR sequences the voltage output DAC from the most-significant-bit (MSB) to the least-significant-bit (LSB). The analog input connects to the comparator via a 5kΩ resistor. The DAC which has a 2.5kΩ output resistance connects to the same comparator input. The comparator, performing a zero crossing detection, tests the addition of successively weighted bits from the DAC output versus the analog input signal. The MSB decision occurs after the second negative edge of the CLK IN following conversion initiation. The remaining 11-bit trials occur on the next 11 negative CLK IN edges. Once a conversion cycle is started it cannot be stopped or restarted, without upsetting the remaining bit decisions. Every conversion cycle must have 13 negative CLK IN edges. At the end of conversion the comparator input voltage is zero. The SAR contains the 12-bit data word representing the analog input voltage. The BUSY line returns to logic high, signalling end of conversion. The SAR transfers the new data to the 12-bit latch.

SYNCHRONIZING START CONVERSION

Aligning the negative edge of the RD with the rising edge of CLK IN provides synchronization of the start convert signal to the conversion process for sampling system applications. Without synchronization the conversion time will vary from 12 to 13 clock cycles. See Figure 9.

FIGURE 8: Simplified Analog Input Circuitry of ADC-9012



POWER ON INITIALIZATION

During system power-up the ADC-9012 comes up in a random state. One complete conversion of 13 clock cycles must be performed to reset the A/D conversion process. The results of the first conversion should be disregarded. The second 13 clock cycles will provide a valid A/D conversion. This is important in battery operated systems where power supplies are shut down between measurement times.

DRIVING THE ANALOG INPUT

During conversion, the DAC output current modulates the analog input current at the CLK IN frequency of 1MHz. The analog input to the ADC-9012 must not change during the conversion process. This requires an external buffer with low output impedance at 1MHz. Suitable devices meeting this requirement include the OP-27, OP-42, and the SMP-11.

INTERNAL CLOCK OSCILLATOR

Figure 10 shows the ADC-9012 internal clock circuit. The clock oscillates at the external crystal or ceramic resonator frequency. The 1MHz crystal or ceramic resonator connects between the CLK IN (pin 17) and the CLK OUT (pin 18). Capacitance values (C1, C2) depend on the crystal or ceramic resonator manufacturer. Typical values range from 30pF to 100pF.

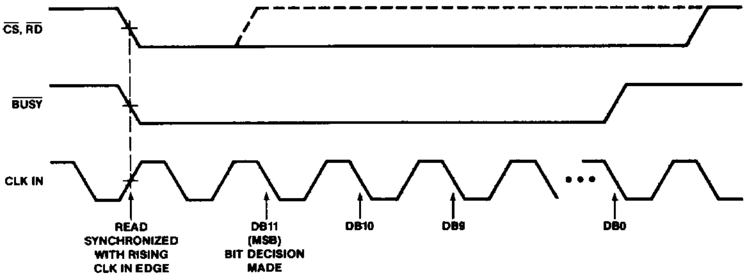
EXTERNAL CLOCK INPUT

A TTL compatible signal connected to CLK IN provides proper converter clock operation. No connection is necessary to the CLK OUT pin. The CLK IN duty cycle is not critical, since all internal circuit timing occurs on the negative CLK IN edge. The duty cycle of the external clock input can range from 20% to 80%. Figure 9 shows the important waveforms.

EXTERNAL REFERENCE

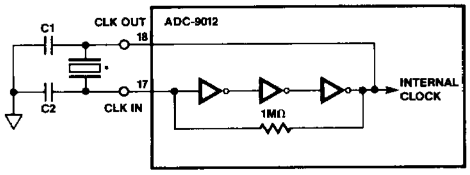
A low-output resistance negative-five volt reference is necessary. The external reference should be able to supply 3mA of reference current. A bypass capacitor is necessary on the

FIGURE 9: External Clock Input Synchronization



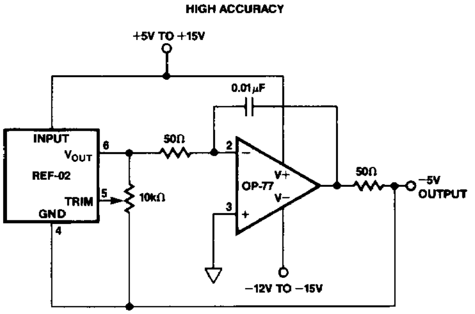
reference input lead to minimize system noise. The reference input to the internal DAC is code dependent requiring anywhere from zero to 3mA. The reference voltage tolerance has a direct influence on A/D converter full-scale voltage. The maximum input full-scale voltage equals 2 × $-V_{REF}$. The ADC-9012 is not designed for ratiometric operation; the range for reference input voltages should be limited to ±5%. Figure 11 provides a good negative-five volt reference.

FIGURE 10: ADC-9012 Simplified Internal Clock Circuit



* CRYSTAL OR CERAMIC RESONATOR

FIGURE 11: Negative-Five Volt Reference

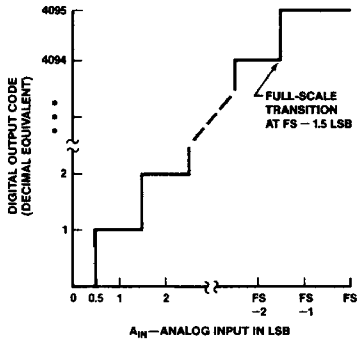


TRIM IS OPTIONAL, ONLY NECESSARY FOR ABSOLUTE ACCURACY CIRCUITS.

UNIPOLAR ANALOG INPUT OPERATION

Figure 12 shows the ideal input/output characteristic for the 0 to 10 volt input range of the ADC-9012. The designed output code transitions occur midway between successive integer LSB values (i.e., 0.5 LSB, 1.5 LSBs, 2.5 LSBs, ..., FS − 1.5 LSBs). The output code is natural binary with 1 LSB = FS/4096 = (10/4096)V = 2.44mV. The maximum full-scale input voltage is (10 × 4095/4096)V = 9.9976V, which is 0.5 LSB higher than the last code transition.

FIGURE 12: Ideal ADC-9012 Input/Output Transfer Characteristic

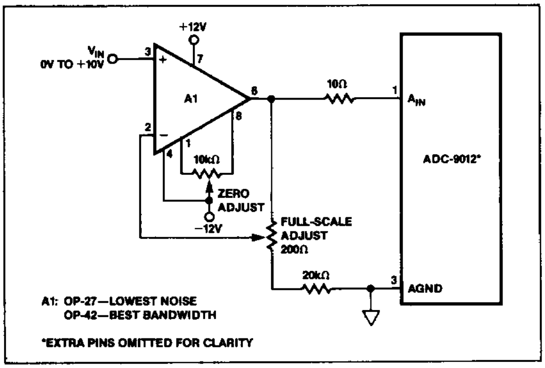


OFFSET AND FULL-SCALE ERROR ADJUSTMENT, UNIPOLAR OPERATION

In applications where absolute accuracy is important then offset and full-scale error can be adjusted to zero. Figure 13 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the null offset of the op amp driving A_{IN}.

Adjust the zero-scale first by applying 1.22mV (equivalent to 0.5 LSB input) to V_{IN}. Adjust the op amp offset control until the digital output toggles between 0000 0000 0000 and 0000 0000 0001. The next step is adjustment of full scale. Apply 9.9964V (equivalent to FS − 1.5 LSB) to V_{IN} and adjust R1 until the digital output toggles between 1111 1111 1110 and 1111 1111 1111.

FIGURE 13: Unipolar 0V to +10V Operation



MICROPROCESSOR INTERFACING

The ADC-9012 has self-contained logic for both 8-bit and 16-bit data bus interfacing. The output data can be formatted into either a 12-bit parallel word for a 16-bit data bus or an 8-bit data word pair for an 8-bit data bus. Data is always right justified, i.e., LSB is the most right-hand bit in a 16-bit word. For a two-byte read, only data outputs D7 . . . D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7 . . . D0/8 outputs (4 MSBs or 8 LSBs) where it can be read in two read cycles. The 4 MSBs always appear on D11 . . . D8 whenever the three-state output drivers are turned on. See Figure 14.

Two A/D conversion modes of operation are available for both data bus sizes: the ROM mode and the Slow-Memory mode.

In the ROM mode each READ instruction obtains new, valid data assuming the minimum timing requirements are satisfied. However, since the data output from a current READ instruction was generated from a conversion initiated by a previous READ operation, the current data may be out-of-date. To be sure of obtaining up-to-date data, READ instructions may be coded in pairs (with some NOPs between them); use only the data from the second READ in each pair. The first READ starts the conversion, the second READ gets the results.

The Slow-Memory mode is the simplest mode. It is the method of choice where compact coding is essential, or where software bugs are a hazard. In this mode, a single READ instruction will initiate a data conversion, interrupt the microprocessor until completion (WAIT states are introduced), then read the results. If the system throughput tolerates WAIT states, and the hardware is correct, then the Slow-Memory mode is virtually immune to subsequent software modifications. Placing the microprocessor in the WAIT state has an additional advantage of quieting the digital system to reduce noise pickup in the analog conversion circuitry. The 12-bit parallel Slow-Memory mode provides the fastest analog sampling rate combined with digital data transfer rate for sampled-data systems.

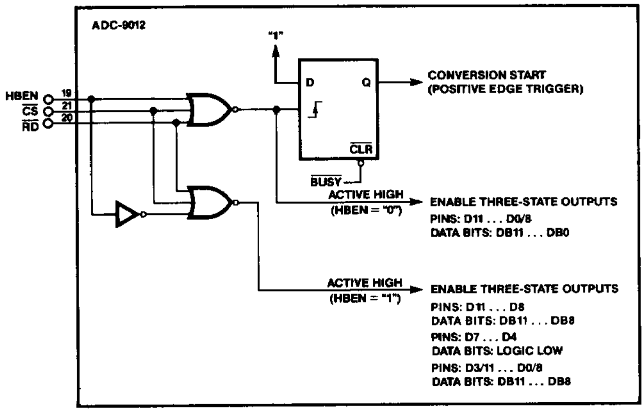
PARALLEL READ, SLOW-MEMORY MODE (HBEN = LOW)

Figure 3 shows the timing diagram and data bus status for Parallel Read, Slow-Memory Mode. CS and RD going low triggers a conversion and the ADC-9012 acknowledges by taking BUSY low. Data from the previous conversion appears on the three-state data outputs. BUSY returns high at the end of conversion, when the output latches have been updated, and the conversion result is placed on data outputs D11 . . . D0/8.

TWO-BYTE READ, SLOW-MEMORY MODE

For a two-byte read only 8 data outputs D7 . . . D0/8 are used. Conversion start procedure and data output status for the first read operation is identical to Parallel Read, Slow-Memory Mode.

FIGURE 14: Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$, and HBEN



See Figure 4, Timing Diagram and Data Bus Status. At the end of conversion, the low data byte (DB7 . . . DB0) is read from the A/D converter. A second READ operation with HBEN high, places the high byte on data outputs D3/11 . . . D0/8 and disables conversion start. Note the 4 MSBs appear on data outputs D11 . . . D8 during these two READ operations.

PARALLEL READ, ROM MODE (HBEN = LOW)

A conversion is started with a READ operation. The 12 bits of data from the previous conversion are available on data outputs D11 . . . D0/8 (see Figure 5). This data may be disregarded if not required. A second READ operation reads the new data (DB11 . . . DB0) and starts another conversion. A delay at least as long as the ADC-9012 conversion time must be allowed between READ operations. If a READ takes place prior to the end of 13 CLKS of the ADC conversion, the remaining bits not yet tested will be invalid.

TWO-BYTE READ, ROM MODE

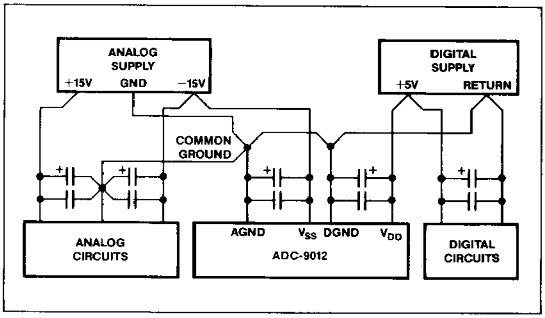
For a two-byte read-only data outputs D7 . . . D0/8 are used. Conversion is started in the same way with a READ operation and the data output status is the same as the Parallel Read, ROM Mode. See Figure 6, Two-Byte Read Timing Diagram. Two more READ operations are required to obtain the new conversion result. A delay equal to the ADC-9012 conversion time must be allowed between conversion start and the second data READ operation. The second READ operation, with HBEN high, disables conversion start and places the high byte (4 MSBs) on data outputs D3/11 . . . D0/8. A third READ operation accesses the low data byte (DB7 . . . DB0) and starts another conversion. The 4 MSBs appear on data outputs D11 . . . D8 during all three read operations above.

CIRCUIT LAYOUT GUIDELINES

As with any high speed A/D converters good circuit layout practice is essential. Wire-wrap boards are not recommended due to stray pickup of the high frequency digital noise. A PC board offers the best results. Digital and analog grounds should be separated even if they are ground planes instead of ground traces. Don't lay digital traces adjacent to high impedance analog traces. Avoid digital layouts that radiate high frequency clock signals, i.e., don't lay out digital signal lines and ground returns in the shape of a loop antenna. Shield the analog input if it comes from a different PC board source. Set up a single point ground at AGND (pin 3) of the ADC-9012. Tie all other analog grounds to this point. Also tie the logic power supply ground, but no other digital grounds to this point (see Figure 15). Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC. Their trace widths should be as wide as possible. Good power supply bypass capacitors located near the ADC package insure quiet operation. Place a 10μF capacitor in parallel with a 0.01μF ceramic capacitor across V_{DD} to ground and V_{SS} to ground (near pin 3).

In applications where the ADC-9012 data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get LSB level errors in conversion results. These errors are due to a feedthrough from the microprocessor to the internal comparator. The problem can be minimized by forcing the microporcessor into a WAIT state during conversion (see Slow-Memory Mode microprocessor interfacing). An alternate method is isolation of the data bus with three-state buffers.

FIGURE 15: Power Supply Grounding



INTERFACING TO THE TMS32010 DSP PROCESSOR

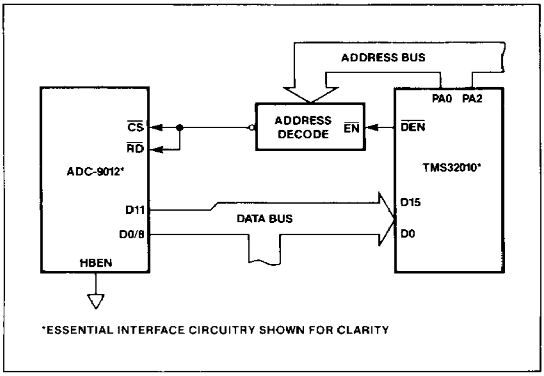
Figure 16 shows an ADC-9012 to TMS32010 interface. The ADC-9012 is operating in the ROM Mode. The interface is designed for a maximum TMS32010 clock frequency of 18.6MHz but will typically work over the full 20MHz TMS32010 clock frequency range.

The ADC-9012 is mapped at a user-selected port address (PA). The following I/O instruction starts a conversion and reads the previous conversion into the data memory.

IN DATA, PA PA = Port Address
DATA = Data Memory Location

When conversion is complete, a second I/O instruction reads the new data into the data memory and starts another conversion. Sufficient A/D conversion time must be allowed between I/O instructions. The very first data read after system power-up should be discarded.

FIGURE 16: ADC-9012 to TMS32010 DSP Processor Interface



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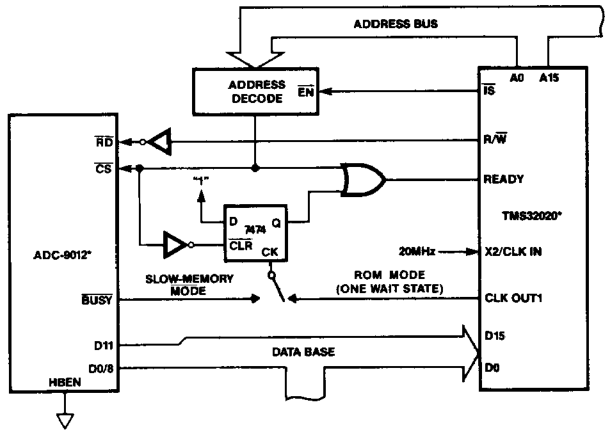
USING WAIT STATES

The TMS32020 DSP processor has the added capability of WAIT states. This feature simplifies the hardware required for slow memory devices by extending the microprocessor bus access time. Figure 15 shows an ADC-9012 to TMS32020 interface using one WAIT state to guarantee data interface at the full 20MHz clock frequency. This WAIT state extends the bus access time by 200ns. In this circuit the ADC-9012 operates in the ROM mode where each input instruction (IN DATA, PA) takes the previous conversion result and stores it in memory. The next input instruction must be delayed as long as the A/D conversion time to read a new conversion result.

SLOW-MEMORY MODE OPERATION USING WAIT STATES

The WAIT state feature of the TMS32020 can be used to operate the ADC-9012 in the Slow-Memory mode. This is accomplished by driving the clock input of the 7474 flip-flop in Figure 17, from the BUSY output of the ADC-9012, instead of the CLK OUT1 of the TMS32020. Once a conversion has started the READY input of the TMS32020 is not released until the ADC-9012 completes its 12-bit A/D conversion. This stops the TMS32020 during the conversion process reducing microprocessor system noise generation. Another advantage for the system software is the single instruction IN MEM, PA used to start, process, and read the results of the A/D conversion. This makes the software code more transportable between systems operating at different clock speeds. The disadvantage is wasted processing time.

FIGURE 17: ADC-9012 to TMS32020 Interface Using WAIT States



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