Product Preview

1:2 Fanout Differential PECL to TTL Translator

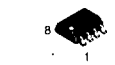
MC10ELT26
MC100ELT26

The MC10ELT/100ELT26 is a 1:2 fanout differential PECL to TTL translator. Because PECL (Positive ECL) levels are used only +5V and ground are required. The small outline 8-lead SOIC package and the 1:2 fanout design of the ELT23 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The V_{BB} output allows the ELT26 to also be used in a single-ended input mode. In this mode the V_{BB} output is tied to the $\overline{IN}$ input for a non-inverting buffer or the IN input for an inverting buffer. If used the V_{BB} pin should be bypassed to ground via a 0.01μF capacitor.

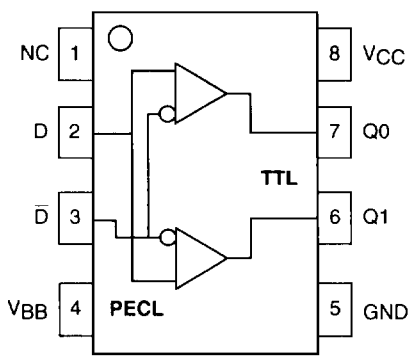
The ELT26 is available in both ECL standards: the 10ELT is compatible with positive MECL 10H logic levels while the 100ELT is compatible with positive ECL 100K logic levels.

- 3.5ns Typical Propagation Delay
- <500ps Typical Output to Output Skew
- Differential PECL Inputs
- Small Outline SOIC Package
- 24mA TTL Outputs
- Flow Through Pinouts



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Qn	TTL Outputs
D	Diff PECL Input
V_{CC}	+5.0V Supply
V_{BB}	Reference Output
GND	Ground

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