32-bit Barrel Shifter with Registers LSH33

FEATURES

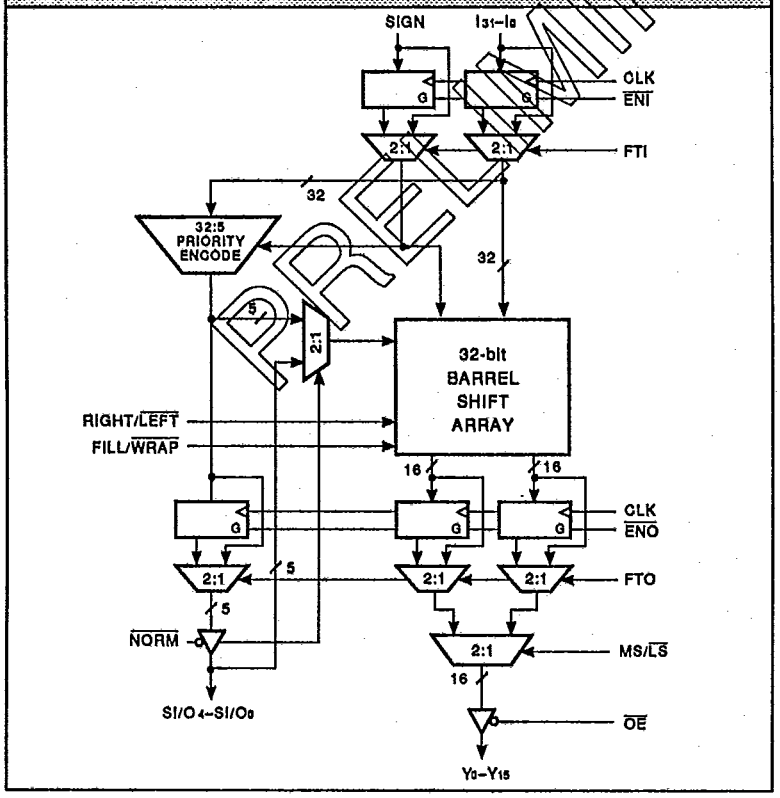
- 32-bit Input, 32-bit Output Multiplexed to 16 Lines
- Full 0–31 Position Barrel Shift Capability
- Integral Priority Encoder for 32-bit Floating Point Normalization
- Sign-Magnitude or Two's Complement Mantissa Representation
- 32-bit Linear Shifts with Sign or Zero Fill
- Fully Registered Input/Output with Independent Bypass Paths
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC (Type C)
  - 68-pin Pin Grid Array

DESCRIPTION

The LSH33 is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shift with sign extend are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

Input/Output registers provide complete pipelined operation. Both have independent bypass paths for complete flexibility.

LSH33 Block Diagram



Shift Array

The 32 registered inputs to the LSH33 are applied to a 32-bit shift array. The 32 outputs of this array can be registered, then are multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH33 is configured as a left shift device. That is, a shift code of 00000$_2$ results in no shift of the input field. A code of 00001$_2$ provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 11111$_2$ (–1$_{10}$) results in a right shift of one position, etc.

When not in the wrap mode, the LSH33 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the Right/$\overline{\text{Left}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

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Table 1. Wrap Mode Shift Code Definitions.

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	I_{31}	I_{30}	•	•	I_{16}	I_{15}	•	•	I_1	I_0
00001	I_{30}	I_{29}	•	•	I_{15}	I_{14}	•	•	I_0	I_{31}
00010	I_{29}	I_{28}	•	•	I_{14}	I_{13}	•	•	I_{29}	I_{30}
00011	I_{28}	I_{27}	•	•	I_{13}	I_{12}	•	•	I_{30}	I_{29}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	I_{16}	I_{15}	I_{14}	•	I_1	I_0	•	•	I_{18}	I_{17}
10000	I_{15}	I_{14}	I_{13}	•	I_0	I_{31}	•	•	I_{17}	I_{16}
10001	I_{14}	I_{13}	I_{12}	•	I_{31}	I_{30}	•	•	I_{16}	I_{15}
10010	I_{13}	I_{12}	I_{11}	•	I_{30}	I_{29}	•	•	I_{15}	I_{14}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	I_{13}	I_{12}	I_1	•	I_{20}	I_{19}	•	•	I_5	I_4
11101	I_2	I_1	I_0	•	I_{19}	I_{18}	•	•	I_4	I_3
11110	I_1	I_0	I_{31}	•	I_{18}	I_{17}	•	•	I_3	I_2
11111	I_0	I_{31}	I_{30}	•	I_{17}	I_{16}	•	•	I_2	I_1

Table 2. Fill Mode Shift Code Definitions (Left Shift).

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	I_{31}	I_{30}	•	•	I_{16}	I_{15}	•	•	I_1	I_0
00001	I_{30}	I_{29}	•	•	I_{15}	I_{14}	•	•	I_0	0
00010	I_{29}	I_{28}	•	•	I_{14}	I_{13}	•	•	0	0
00011	I_{28}	I_{27}	•	•	I_{13}	I_{12}	•	•	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	I_{16}	I_{15}	I_{14}	•	I_1	I_0	•	•	0	0
10000	I_{15}	I_{14}	I_{13}	•	I_0	0	•	•	0	0
10001	I_{14}	I_{13}	I_{12}	•	0	0	•	•	0	0
10010	I_{13}	I_{12}	I_{11}	•	0	0	•	•	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	I_3	I_2	I_1	•	0	0	•	•	0	0
11101	I_2	I_1	I_0	•	0	0	•	•	0	0
11110	I_1	I_0	0	•	0	0	•	•	0	0
11111	I_0	0	0	•	0	0	•	•	0	0

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{L}$ input can be viewed as the most significant bit of a 6-bit two's complement shift code, comprised of R/$\overline{L}$ concatenated with the SI_4–SI_0 lines. Thus a positive shift code (R/$\overline{L}$ = 0) results in a left shift of 0–31 positions, and a negative code (R/$\overline{L}$ = 1) a right shift of up to 32 positions. The LSH33 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

Output Multiplexer

The shift array outputs can be registered and then applied to a 2:1 multiplexer controlled by the MS/$\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

Priority Encoder

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result the leading significant digit will always be "1." This affects only the encoder inputs;

Table 3. Fill Mode Shift Code Definitions (Right Shift).

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	S	S	•	•	S	S	•	•	S	S
00001	S	S	•	•	S	S	•	•	S	I_{31}
00010	S	S	•	•	S	S	•	•	I_{31}	I_{30}
00011	S	S	•	•	S	S	•	•	I_{30}	I_{29}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	S	S	S	•	S	S	•	•	I_{18}	I_{17}
10000	S	S	S	•	S	I_{31}	•	•	I_{17}	I_{16}
10001	S	S	S	•	I_{31}	I_{30}	•	•	I_{16}	I_{15}
10010	S	S	S	•	I_{30}	I_{29}	•	•	I_{15}	I_{14}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	S	S	S	•	I_{20}	I_{19}	•	•	I_5	I_4
11101	S	S	S	•	I_{19}	I_{18}	•	•	I_4	I_3
11110	S	S	I_{31}	•	I_{18}	I_{17}	•	•	I_3	I_2
11111	S	I_{31}	I_{30}	•	I_{17}	I_{16}	•	•	I_2	I_1

Table 4. Priority Encoder Function Table.

I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}	•••	I_0	Shift Code
1	X	X	•••	X	X	X	•••	X	00000
0	1	X	•••	X	X	X	•••	X	00001
0	0	1	•••	X	X	X	•••	X	00010
•	•	•	•••	•	•	•	•••	•	•
•	•	•	•••	•	•	•	•••	•	•
0	0	0	•••	1	X	X	•••	X	01111
0	0	0	•••	0	1	X	•••	X	10000
0	0	0	•••	0	0	1	•••	X	10001
•	•	•	•••	•	•	•	•••	•	•
•	•	•	•••	•	•	•	•••	•	•
0	0	0	•••	0	0	0	•••	1	11111
0	0	0	•••	0	0	0	•••	0	11111

the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

Normalize Multiplexer

The $\overline{NORM}$ input, when asserted, results in the priority encoder output driving the internal shift code inputs directly. When using the $\overline{NORM}$ function, the LSH33 should be placed in fill mode, with the R/$\overline{L}$ input low.

When $\overline{NORM}$ is high (not asserted), the SI/O_4–SI/O_0 port acts as the shift code input to the shifter.

Applications Examples

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH33. The $\overline{NORM}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{LS}$.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH33 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{LS}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

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Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
Vcc supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ Vcc ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ Vcc ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		Vcc	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ Vcc			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ Vcc			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, Vcc = Max (Notes 4, 8)			–250	mA
I_{CC1}	Vcc Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	Vcc Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10*

GUARANTEED MAXIMUM COMBINATIONAL DELAYS (ns)

From Input \ To Output	LSH33-40 Y_{15}–Y_0	LSH33-40 SO_4–SO_0	LSH33-30 Y_{15}–Y_0	LSH33-30 SO_4–SO_0	
FTI = 0, FTO = 0					
CLK					
MS/$\overline{LS}$		—		—	
FTI = 0, FTO = 1					
CLK					
SI_4–SI_0		—		—	
R/$\overline{L}$, F/$\overline{W}$		—		—	
MS/$\overline{LS}$		—		—	
FTI = 1, FTO = 0					
CLK					
MS/LS		—			
FTI = 1, FTO = 1					
I_{31}–I_0, SIGN					
SI_4–SI_0		—		—	
R/$\overline{L}$, F/$\overline{W}$		—		—	
MS/$\overline{LS}$		—		—	

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE (ns)

Input	LSH33-40 FTI = 0 Setup	LSH33-40 FTI = 0 Hold	LSH33-40 FTI = 1 Setup	LSH33-40 FTI = 1 Hold	LSH33-30 FTI = 0 Setup	LSH33-30 FTI = 0 Hold	LSH33-30 FTI = 1 Setup	LSH33-30 FTI = 1 Hold		
I_{31}–I_0, SIGN										
SI_4–SI_0										
R/$\overline{L}$, F/$\overline{W}$										
$\overline{ENI}$, $\overline{ENO}$										

THREE STATE ENABLE/DISABLE TIMES (ns) Note 11

	LSH33-40	LSH33-30	
t_{EN}			
t_{DIS}			

CLOCK CYCLE TIME AND PULSE WIDTH (ns)

	LSH33-40	LSH33-30	
Minimum Cycle Time			
Highgoing Pulse			
Lowgoing Pulse			

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SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +120°C) *Notes 9, 10*

GUARANTEED MAXIMUM COMBINATIONAL DELAYS (ns)

From Input \ To Output	LSH33-50 Y_{15}–Y_0	LSH33-50 SO_4–SO_0	LSH33-40 Y_{15}–Y_0	LSH33-40 SO_4–SO_0	
FTI = 0, FTO = 0					
CLK					
MS/$\overline{LS}$		—		—	
FTI = 0, FTO = 1					
CLK					
SI_4–SI_0		—		—	
R/$\overline{L}$, F/$\overline{W}$		—		—	
MS/$\overline{LS}$		—		—	
FTI = 1, FTO = 0					
CLK					
MS/LS		—			
FTI = 1, FTO = 1					
I_{31}–I_0, SIGN					
SI_4–SI_0		—		—	
R/$\overline{L}$, F/$\overline{W}$		—		—	
MS/$\overline{LS}$		—		—	

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE (ns)

Input	LSH33-50 FTI = 0 Setup	LSH33-50 FTI = 0 Hold	LSH33-50 FTI = 1 Setup	LSH33-50 FTI = 1 Hold	LSH33-40 FTI = 0 Setup	LSH33-40 FTI = 0 Hold	LSH33-40 FTI = 1 Setup	LSH33-40 FTI = 1 Hold		
I_{31}–I_0, SIGN										
SI_4–SI_0										
R/$\overline{L}$, F/$\overline{W}$										
$\overline{ENI}$, $\overline{ENO}$										

THREE STATE ENABLE/DISABLE TIMES (ns) Note 11

	LSH33-50	LSH33-40	
t_{EN}			
t_{DIS}			

CLOCK CYCLE TIME AND PULSE WIDTH (ns)

	LSH33-50	LSH33-40	
Minimum Cycle Time			
Highgoing Pulse			
Lowgoing Pulse			

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at –0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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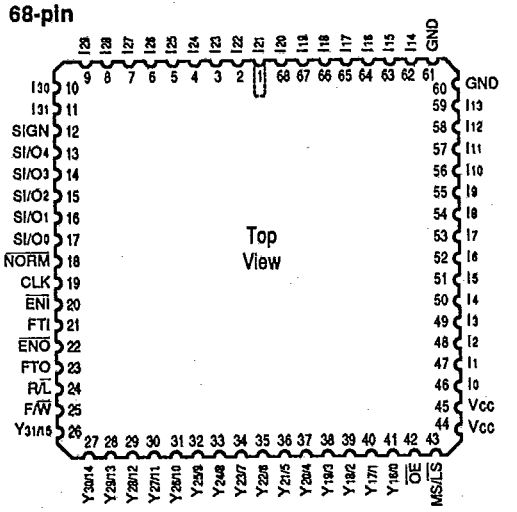
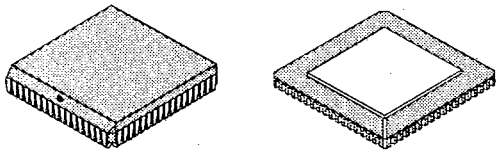
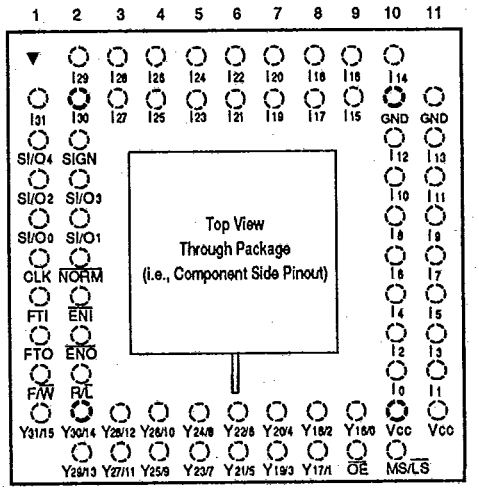
ORDERING INFORMATION

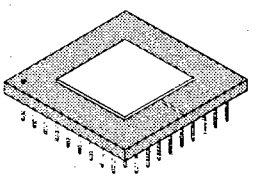
68-pin





68-pin





Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening		
40 ns 30 ns	LSH33JC40 ▪ ▪ 30	LSH33KC40 ▪ ▪ 30	LSH33GC40 ▪ ▪ 30
	–55°C to +125°C — Commercial Screening		
50 ns 40 ns		LSH33KM50 ▪ ▪ 40	LSH33GM50 ▪ ▪ 40
	–55°C to +125°C — Extended Screening		
50 ns 40 ns		LSH33KME50 ▪ ▪ 40	LSH33GME50 ▪ ▪ 40
	–55°C to +125°C — MIL-STD-883 Compliant		
50 ns 40 ns		LSH33KMB50 ▪ ▪ 40	LSH33GMB50 ▪ ▪ 40