SERIAL E^2PROM

TC89121P, TC89122P
TC89121M, TC89122M

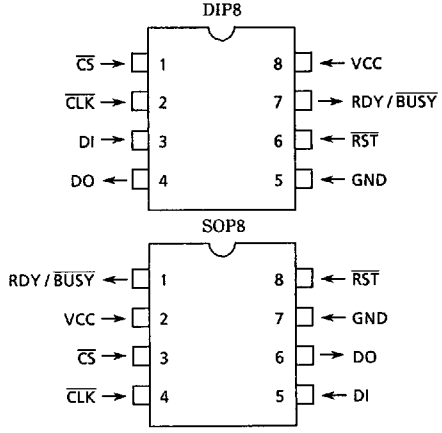
The TC89121P is a 1024 bit serial E²PROM. The TC89122P is a 2048 bit serial E²PROM. These are fabricated with floating gate CMOS technology.

PART No.	CAPACITY	ORGANIZATION	PACKAGE
TC89121P	1024-bit	128 x 8-bit	DIP8
TC89121M			SOP8
TC89122P	2048-bit	256 x 8-bit	DIP8
TC89122M			SOP8

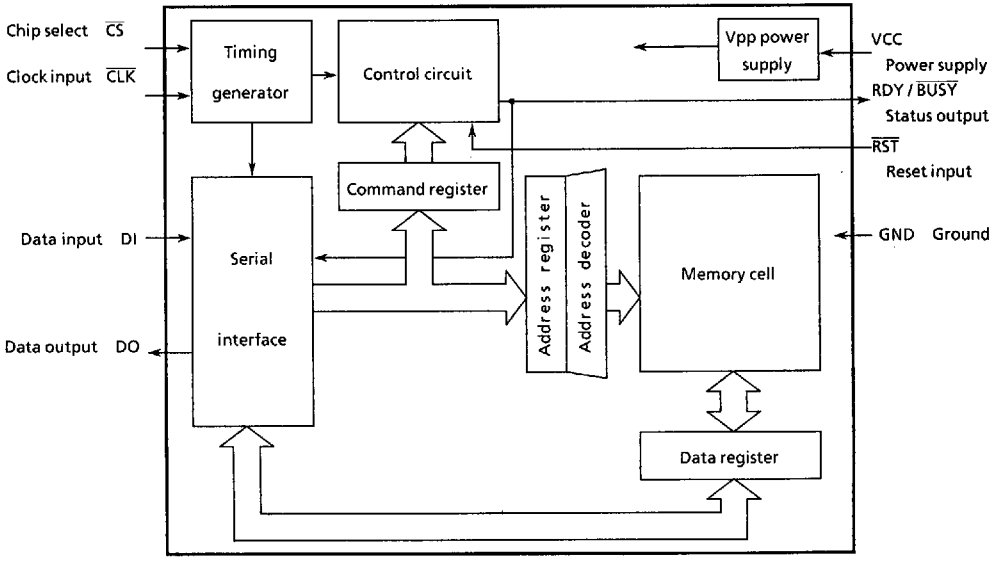
FEATURES

- ◆Serial I/O
- ◆Self timed Program cycle (Built in Timer)
- ◆Program Time ; 10ms Max (Vcc 2.7 to 5.5V)
- ◆Ready/Busy status signal
- ◆Erase/Write Enable and Disable by software
- ◆Program and Chip Erase
- ◆Single 5V supply
- ◆Low power dissipations (CMOS)
- ◆Wide voltage supply (2.7 to 5.5V)
- ◆Wide operating temperature

PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS
$\overline{CS}$	Input	Chip select Chip is enabled when $\overline{CS}$ is at "L" level. Set $\overline{CS}$ to "H" level before executing instructions.
$\overline{CLK}$	Input	Clock Input The DI data is latched at the rising edge of $\overline{CLK}$. The data is output from DO at the falling edge of $\overline{CLK}$. $\overline{CLK}$ is enabled when $\overline{CS}$ is at "L" level.
DI	Input	Serial data input The address, command and Data input pin.
DO	Output	Serial data output The data output pin.
$\overline{RST}$	Input	Reset input Reset signal input pin.
RDY/$\overline{BUSY}$	Output	Status output "L" level is output during Program or Chip Erase operation. "H" level is output when Program or Chip Erase operation is completed.
VCC	Power supply	+ 5V
GND		0V (GND)

OPERATIONAL DESCRIPTION

1. INSTRUCTION SET

(1) TC89121

Instruction	Address	Command	Data
		C0 C1 C2 C3	
Read	A0 ~ A6, 0	1 0 0 0 0 0 0 0	
Program	A0 ~ A6, 0	0 1 1 0 0 0 0 0	D0 ~ D7
Chip Erase	* * * * * * * *	0 0 1 1 0 0 0 0	
Busy Monitor	* * * * * * * *	1 0 1 1 0 0 0 0	
E/W Enable	* * * * * * * *	1 0 0 1 0 0 0 0	
E/W Disable	* * * * * * * *	1 1 0 1 0 0 0 0	

** ; don't care*

(2) TC89122

Instruction	Address	Command								Data
		C0	C1	C2	C3					
Read	A0 ~ A7	1	0	0	0	0	0	0	0	
Program	A0 ~ A7	0	1	1	0	0	0	0	0	D0 ~ D7
Chip Erase	********	0	0	1	1	0	0	0	0	
Busy Monitor	********	1	0	1	1	0	0	0	0	
E/W Enable	********	1	0	0	1	0	0	0	0	
E/W Disable	********	1	1	0	1	0	0	0	0	

*; *don't care*

2. OPERATION METHOD

Set $\overline{CS}$ and $\overline{CLK}$ to "H" level before executing instruction. $\overline{CS}$ changes to "L" level, then $\overline{CLK}$ is enabled and operates as the sync signal for serial I/O. The DI data is latched at the rising edge of $\overline{CLK}$. The data is output from DO at the falling edge of $\overline{CLK}$.

Execute instruction only when RDY/$\overline{BUSY}$ status signal is "H" level. However Busy Monitor instruction can be executed whenever.

Uses only commands which are included in the Instruction Set listed above.

(1) Read

Executing Read instruction reads out the memory data at the specified address and outputs it serially from DO.

(2) Program

Executing Program instruction automatically starts internal rewriting of the memory data at the specified address with the input data.

After Program instruction is input, $\overline{CS}$ can be set to "H" level ever while the internal rewriting process is operating.

(3) Chip Erase

Executing Chip Erase instruction automatically Starts internal erasing of the memory data at all address.

After Chip Erase instruction is input, $\overline{CS}$ can be set to "H" level even while the internal erasing process is operating.

(4) Busy Monitor

Executing Busy Monitor instruction outputs the RDY/$\overline{BUSY}$ status signal from DO.

"L" level is output during Program or Chip Erase operation. "H" level is output when Program or Chip Erase operation is completed.

The RDY/$\overline{BUSY}$ status signal is output until $\overline{CS}$ is switched to "H" level.

(5) E/W Enable

Executing E/W Enable instruction sets E/W enable mode and enables Program and Chip Erase instructions.

(6) E/W Disable

Executing E/W Disable instruction sets the E/W disable mode and disables both the Program and Chip Erase instructions. Once E/W disable mode is set, E/W disable mode is held until E/W Enable instruction is executed.

E/W disable mode is set by reset signal input.

3. CAUTIONS WHEN TURNING THE POWER ON AND OFF

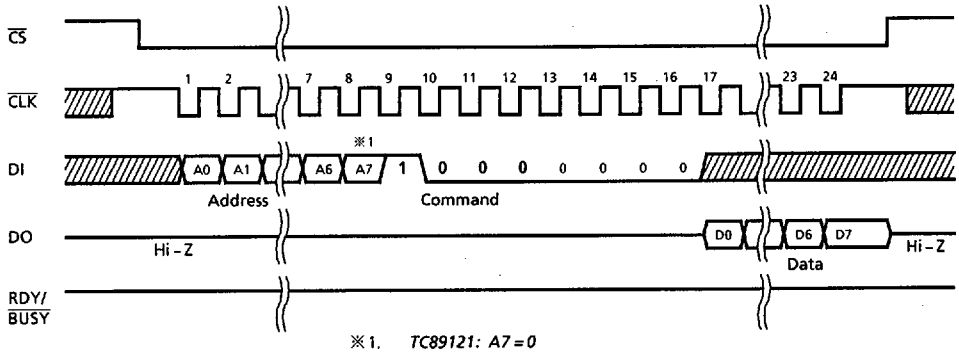
(1) After turning the power on, wait 1ms for warm-up before executing instruction.

(2) Set $\overline{RST}$ to "L" level when turning the power on and off.

(3) E/W disable mode is set by reset signal input.

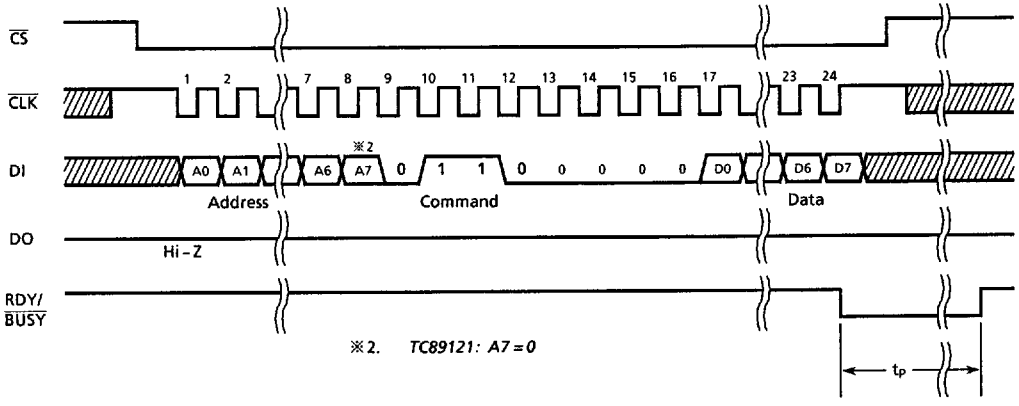
4. TIMING DIAGRAMS

(1) Read



※1. *TC89121: A7 = 0*

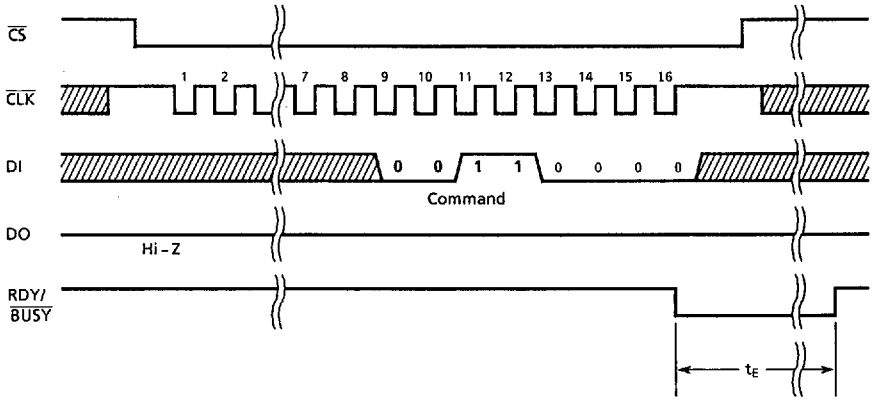
(2) Program



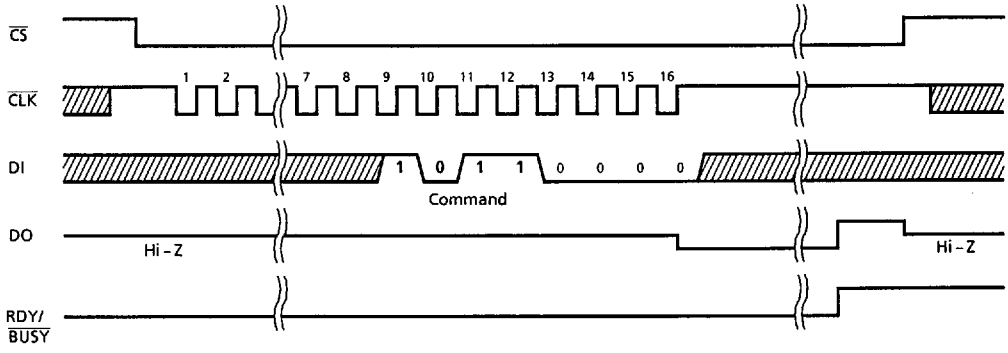
※2. *TC89121: A7 = 0*

Note. ▨ *don't care*

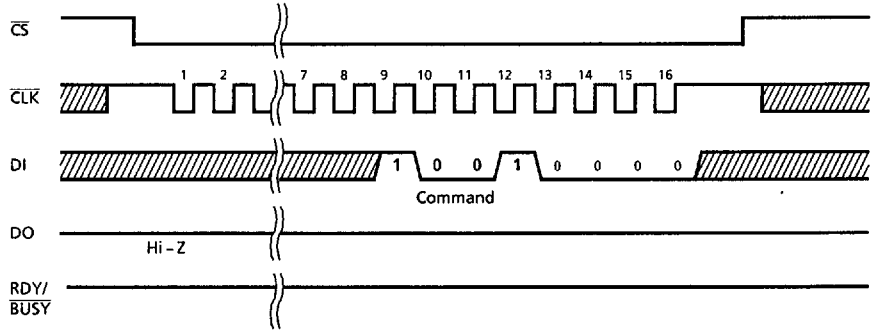
(3) Chip Erase



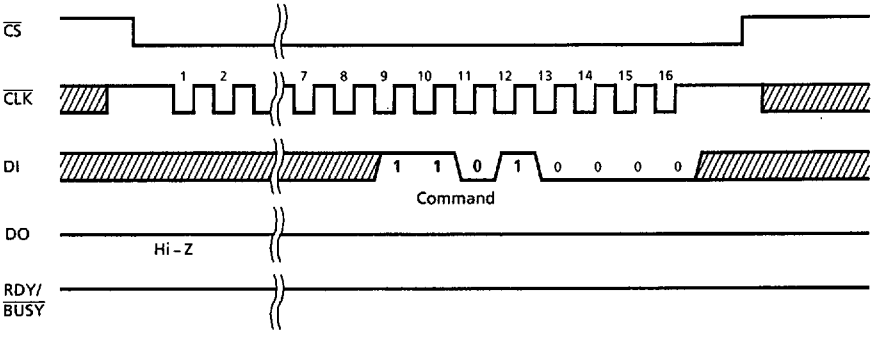
(4) Busy Monitor



(5) E/W Enable



(6) E/W Disable



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (GND = 0V)

PARAMETER	SYMBOL	RATINGS	UNITS
Supply Voltage	V_{CC}	−0.3~7	V
Input Voltage	V_{IN}	−0.3~V_{CC} + 0.3	V
Output Voltage	V_{OUT}	−0.3~V_{CC} + 0.3	V
Power Dissipation	PD	600	mW
Soldering Temperature (time)	Tsld	260 (10sec)	°C
Storage Temperature	Tstg	−55~125	°C
Operating Temperature	Topr	−30~70	°C

RECOMMENDED OPERATING CONDITION (GND = 0V, Topr = −30~70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Max.	UNITS
Supply Voltage	V_{CC}		2.7	5.5	V

RECOMMENDED OPERATING CONDITION

($GND = 0V$, $V_{CC} = 4.5 \sim 5.5V$, $Topr = -30 \sim 70°C$)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNITS
Input Low Voltage	V_{IL}		$V_{CC} = 4.5V$	0	0.8	V
Input High Voltage	V_{IH1}	$\overline{CS}$, DI, $\overline{RST}$	$V_{CC} = 5.5V$	2.0	V_{CC}	V
	V_{IH2}	$\overline{CLK}$	$V_{CC} = 5.5V$	3.0	V_{CC}	V
Clock Frequency	f_{CLK}			0	1	MHz

D.C. CHARACTERISTICS

($GND = 0V$, $V_{CC} = 4.5 \sim 5.5V$, $Topr = -30 \sim 70°C$)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNITS
Input Current	I_{LI}		–	–	± 10	μA
Output Leakage Current	I_{LO}		–	–	± 10	μA
Output High Voltage	V_{OH1}	$V_{CC} = 4.5V$, $I_{OH} = -400\mu A$	2.4	–	–	V
Output Low Voltage	V_{OL1}	$V_{CC} = 4.5V$, $I_{OL} = 2.1mA$	–	–	0.4	V
Output High Voltage	V_{OH2}	$I_{OH} = -20\mu A$ (CMOS Interface)	$V_{CC}-0.4$	–	–	V
Output Low Voltage	V_{OL2}	$I_{OL} = 20\mu A$ (CMOS Interface)	–	–	0.4	V
Supply Current	I_{CCO}		–	–	500	μA
	I_{CCP}	During Program or Chip Erase	–	–	10	mA
	I_{CCS}	$\overline{CS} = 1$ (Except Program or Chip Erase operation)	–	–	10	μA

A.C. CHARACTERISTICS

($GND = 0V$, $V_{CC} = 4.5 \sim 5.5V$, $Topr = -30 \sim 70°C$)

PARAMETER	SYMBOL	Min.	Max.	UNITS
$\overline{CLK}$ Frequency	f_{CLK}	0	1	MHz
$\overline{CLK}$ Low Time	t_{CKL}	400	–	ns
$\overline{CLK}$ High Time	t_{CKH}	400	–	ns
$\overline{RST}$ Low Time	t_{RSW}	1	–	μs
$\overline{RST}$ Input Setup Time	t_{RSS}	1	–	μs
$\overline{CLK}$ Input Setup Time	t_{CKS}	250	–	ns
$\overline{CS}$ Input Setup Time	t_{CSS}	250	–	ns
DO Output Delay Time ※1	t_{ODD1}	–	250	ns
	t_{ODD2}	–	500	ns
RDY/$\overline{BUSY}$ Output Delay Time	t_{RBD}	–	250	ns
DI Input Setup Time	t_{IDS}	250	–	ns
DI Input Hold Time	t_{IDH}	250	–	ns

※1 $C_L = 100pF$, $V_{OH} / V_{OL} = 2.0V / 0.8V$

RECOMMENDED OPERATING CONDITION

(GND = 0V, V_{CC} = 2.7~3.3V, Topr = −30~70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNITS
Input Low Voltage	V_{IL}		V_{CC} = 2.7V	0	0.45	V
Input High Voltage	V_{IH1}	$\overline{CS}$, DI, $\overline{RST}$	V_{CC} = 3.3V	1.6	V_{CC}	V
	V_{IH2}	$\overline{CLK}$	V_{CC} = 3.3V	2.0	V_{CC}	V
Clock Frequency	f_{CLK}			0	250	KHz

D.C. CHARACTERISTICS

(GND = 0V, V_{CC} = 2.7~3.3V, Topr = −30~70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNITS
Input Current	I_{LI}		−	−	±5	μA
Output Leakage Current	I_{LO}		−	−	±5	μA
Output High Voltage	V_{OH}	I_{OH} = −20μA (CMOS Interface)	V_{CC} − 0.4	−	−	V
Output Low Voltage	V_{OL}	I_{OL} = 20μA (CMOS Interface)	−	−	0.4	V
Supply Current	I_{CCO}		−	−	100	μA
	I_{CCP}	During Program or Chip Erase	−	−	6	mA
	I_{CCS}	$\overline{CS}$ = 1 (Except Program or Chip Erase operation)	−	−	5	μA

A.C. CHARACTERISTICS

(GND = 0V, V_{CC} = 2.7~3.3V, Topr = −30~70°C)

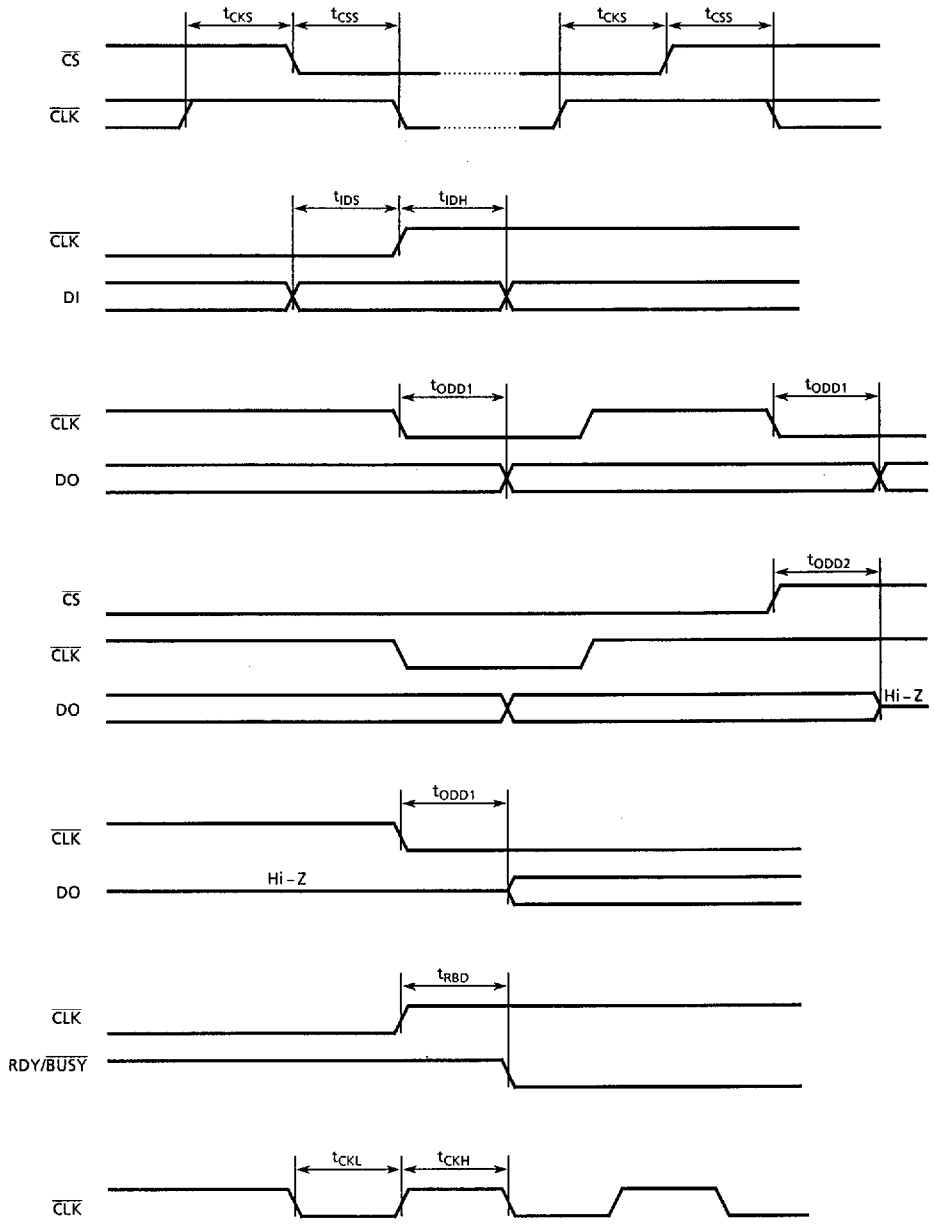
PARAMETER	SYMBOL	Min.	Max.	UNITS
$\overline{CLK}$ Frequency	f_{CLK}	0	250	KHz
$\overline{CLK}$ Low Time	t_{CKL}	2	−	μs
$\overline{CLK}$ High Time	t_{CKH}	2	−	μs
$\overline{RST}$ Low Time	t_{RSW}	4	−	μs
$\overline{RST}$ Input Setup Time	t_{RSS}	4	−	μs
$\overline{CLK}$ Input Setup Time	t_{CKS}	1	−	μs
$\overline{CS}$ Input Setup Time	t_{CSS}	1	−	μs
DO Output Delay Time ※1	t_{ODD1}	−	1	μs
	t_{ODD2}	−	2	μs
RDY/$\overline{BUSY}$ Output Delay Time	t_{RBD}	−	1	μs
DI Input Setup Time	t_{IDS}	1	−	μs
DI Input Hold Time	t_{IDH}	1	−	μs

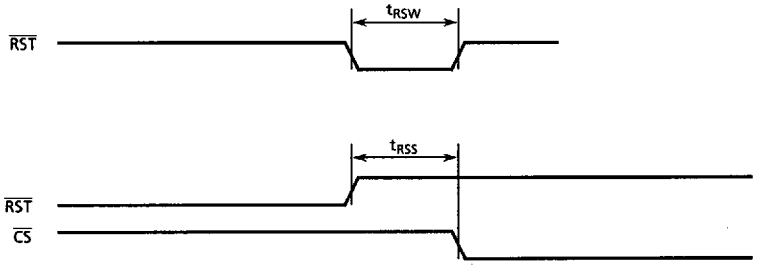
※1 C_L = 100pF, V_{OH} / V_{OL} = 1.6V / 0.45V

E²PROM CHARACTERISTICS (GND = 0V, V_{CC} = 2.7~5.5V, Topr = −30~70°C)

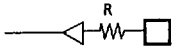
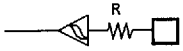
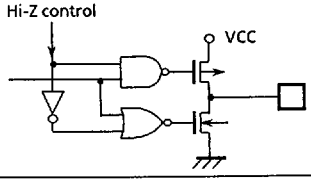
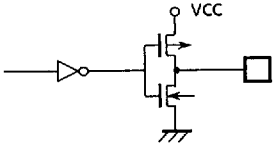
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNITS
Chip Erase Time	t_E		–	4	10	ms
Program Time	t_P		–	4	10	ms
Erase/Write Cycle	N_{EW}		5×10^4	3×10^5	–	cycles
Data Retention Time	t_{RET}		10	–	–	years

A.C. CHARACTERISTICS TIMING DIAGRAMS





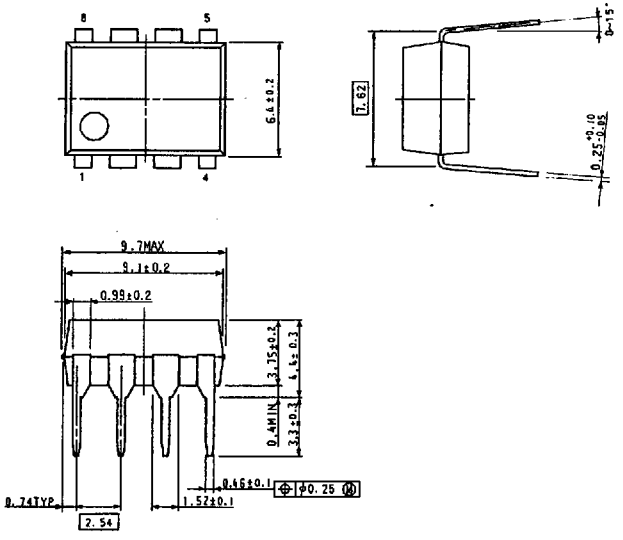
INPUT/OUTPUT CIRCUITRIES

PIN NAME	I/O	INPUT/OUTPUT CIRCUTRY	REMARKS
$\overline{CS}$ DI $\overline{RST}$	Input		
$\overline{CLK}$	Input		Hysteresis input
DO	Output		Initial "Hi-Z"
RDY/$\overline{BUSY}$	Output		Initial "High"

PACKAGE

UNIT:mm

DIP8-P-300B



SOP8-P-225