DATA SHEET

DFE9952R
DFE Read Signal Processor

Objective Specification
Mass Storage Product Group

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Philips
Semiconductors

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DFE Read Signal Processor DFE9952R

GENERAL DESCRIPTION

The DFE9952R is a 200 Mbit/s Decision Feedback Equalization (DFE) read channel integrated circuit designed for hard disk drives. With enhanced decision feedback equalization implemented with advanced BiCMOS technology, the DFE9952R is able to provide high performance with low power consumption.

The following read channel functions are included: variable gain amplification with programmable AGC control, adaptive forward filtering, hybrid RAM/linear feedback filtering, timing recovery, synchronization, write/idle clock synthesis, servo demodulation, a complete 8/9 (0,4) ENDEC, and programmable write precompensation.

The DFE9952R is fully programmable to support a wide range of hard disk drive design points. This includes operating frequencies from 64 to 200 Mbit/s, fully programmable, adaptive equalizers, write precompensation, write current reference, etc. The programmed parameters are easily accessed through a serial port.

The DFE9952R dissipates 800 mW in read mode at 200 Mbit/s. Full power management features have been designed to power down idle circuits. Sleep mode power consumption is less than 100 mW.

Features

- Fully integrated BiCMOS single chip read channel
- 64-200 Mbit/s data rate, programmable in 1% steps
- Hybrid RAM/linear decision feedback equalization
- Real-time adaptive equalization
- Single 5V (±10%) supply
- PD <800 mW at 200 Mbit/s
- Sleep mode power <100 mW
- Sleep to Wakeup time <5 µs
- Bidirectional NRZ data interface, Byte or nibble (8 or 4 bits) wide
- Local data generator for equalizer training and channel quality measurement
- 8/9 rate (0,4/4) Industry standard ENDEC
- Data randomizer
- Adjustable threshold slicer in DFE core for stressed error generation.
- Standard 3-wire serial port interface
- Sync detector logic
- Programmable Write precompensation
- Write current reference DAC
- MR stripe bias DAC
- Differential Analog test ports (forward filter, equalizer out, etc.)
- 64-pin LQFP package

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

Maximum Ratings

Parameter	Rating	Units
Storage Temperature	- 65 to 150	°C
Maximum Junction Operating Temperature	125	°C
Positive Supply Voltage	-0.5 to 6.5	V
Voltage Applied to Any Pin	-0.5 to V_{CC} + 0.5	V

SIMPLIFIED BLOCK DIAGRAM

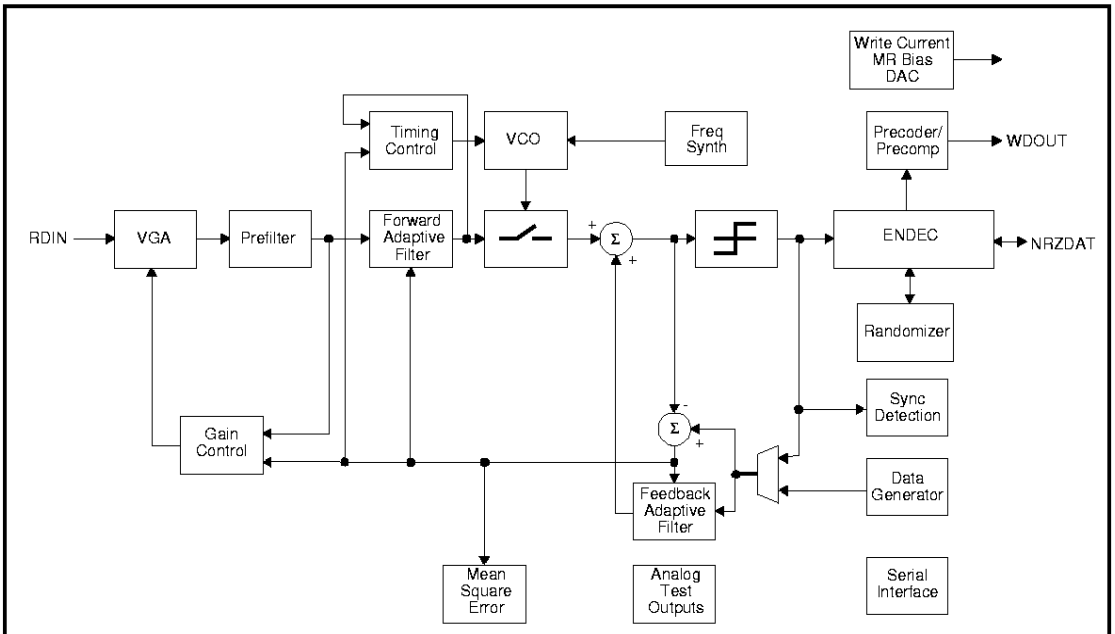


FIGURE 1. High Level Block Diagram

MATHEMATICAL MODEL TERMS

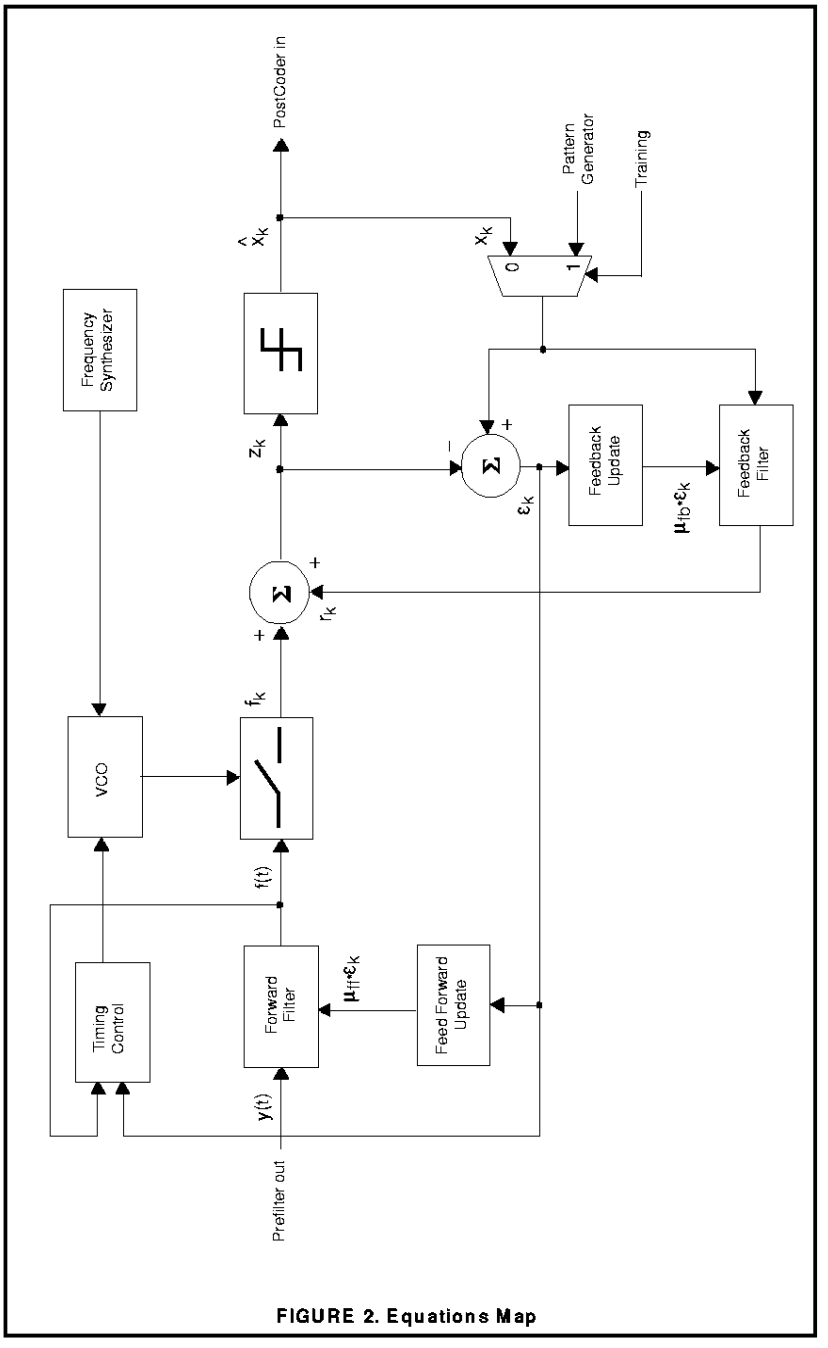


FIGURE 2. Equations Map

PIN DIAGRAM

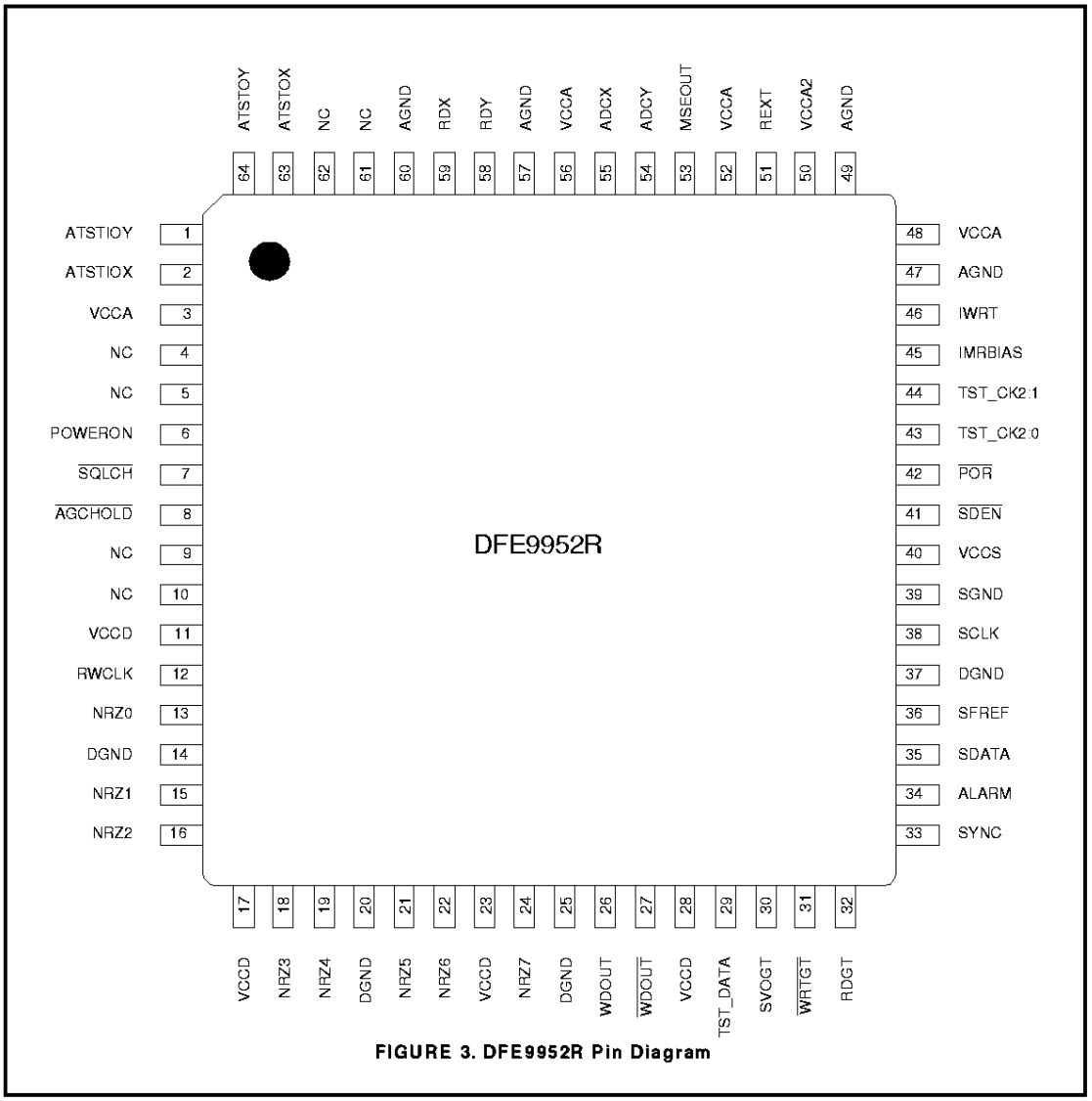


FIGURE 3. DFE9952R Pin Diagram

PIN DESCRIPTIONS

Digital Pins

Symbol	Pin	Type	Description
$\overline{\text{SDEN}}$	41	I	**$\overline{\text{Shift Enable}}$** - Allows data transfer to/from the serial interface. Active LOW.
SCLK	38	I	**Serial Clock** - Positive edge clocks data bits into and out of the serial interface.
SDATA	35	I/O	**Serial Data** - Bidirectional data interface to/from the serial interface. Data must be/is valid at the rising edge of SCLK.
$\overline{\text{POR}}$	42	I	**$\overline{\text{Power-On Reset}}$** - Sets internal logic to reset state. Connect to microcontroller Power on Reset pin. Active LOW. (TTL compatible)
POWERON	6	I	**Poweron** - Must be turned on 5 µsec before RDGT and SVOGT, but not $\overline{\text{WRTGT}}$.
RDGT	32	I	**Read Gate** - From disk controller to initiate read operation. (TTL compatible)
$\overline{\text{WRTGT}}$	31	I	**$\overline{\text{Write Gate}}$** - From disk controller to initiate write operation. Active LOW. (TTL compatible)
SVOGT	30	I	**Servo Gate** - Periodic signal required for offset cancellation - there is no active Servo circuitry in this device. (TTL compatible)
NRZ7 NRZ6 NRZ5 NRZ4 NRZ3 NRZ2 NRZ1 NRZ0	24 22 21 19 18 16 15 13	I/O	**NRZ Data** - 8-bit bi-directional interface. Asserting RDGT makes the DFE9952R drive read data onto this bus. When $\overline{\text{WRTGT}}$ is asserted, the DFE9952R receives write data from this bus. Data is strobed on the rising edge of RWCLK. In the 4-bit NRZ mode, the data is transferred using the four LSBs of this bus. (TTL compatible. Input buffers have internal pulldowns.)
RWCLK	12	O	**R/W Clock** - From DFE9952R to disk controller to strobe data on NRZ7:0. CLOCK IS ALWAYS PRESENT unless the DisRWCLK bit is set.
WDOUT $\overline{\text{WDOUT}}$	26 27	O	**Differential Write Data Output** - Encoded and precompensated NRZI write data to preamp. (Pseudo-ECL levels)
SYNC	33	O	**Sync Mark Detected** - Asserted when the sync mark is detected in the read mode and remains asserted until the end of the current read operation.
ALARM	34	O	**Alarm** - Assertion indicates the IC has determined an internal error has occurred. Assertation of two controls at once will set this signal - controls SVOGT, RDGT, and $\overline{\text{WRTGT}}$.
SFREF	36	I	**Synthesizer Reference Clock** -Reference frequency for the frequency synthesizer. The input frequency must be from 20 to 40 MHz. Also used as the reference for tuning the Prefilter.
$\overline{\text{AGCHOLD}}$	8	I	**$\overline{\text{AGC Hold}}$** - Disables the AGC charge pump and holds the variable gain amplifier gain at its last value. Active LOW. (TTL compatible)
$\overline{\text{SQLCH}}$	7	I	**$\overline{\text{VGA Squelch}}$** - Places low impedance across signal inputs to VGA. Active LOW. (CMOS compatible)

Digital Pins (Continued)

Symbol	Pin	Type	Description
TST_DATA	29	I	**Test Read Data Input** - NRZI read data input port when EnRdTest bit in Control2 Register is enabled. Allows test access into the Decision block and Feedback filter.
TST_CK2:1 TST_CK2:0	44 43	I/O	**Test Clock I/O pins** - When used as inputs, external clocks can be used to replace free running oscillators for testing purposes. When used as outputs, they can be used to monitor the VCOs of the Frequency Synthesizer or Timing Recovery.

Analog Pins

Symbol	Pin	Type	Description
RDX RDY	59 58	I	**Differential Read Data** - Analog head read signal from preamp input into Variable Gain Amplifier.
IWRT (TST_CK1:1)	46	O (I)	**Write Current** - This is a scaled current used to establish the write head current in the R/W preamp. In test mode, this is the TST_CK1:1 input pin.
IMRBIAS (TST_CK1:0)	45	O (I)	**MR Head Bias Current** - This scaled current is used by the R/W preamp to set the MR element bias level. In test mode, this is the TST_CK1:0 input pin.
MSEOUT	53	O	**Equalizer Error Analog** - Output of Mean Square Error. Averaged equalizer error signal for channel quality assessment.
REXT	51	I	**Master Resistor** - A 20 kΩ, 1% external resistor is connected from this pin to VCCA2.
ATSTIOY ATSTIOX	1 2	I/O	**Analog High-Speed I/O Test Bus** - state and internal connections controlled through the serial interface.
ATSTOX ATSTOY	63 64	O	**Analog High-Speed Output Test Bus** - state and internal connections controlled through the serial interface. Bandwidth is 150 MHz.
ADCX ADCY	55 54	I/O	**Analog Low-Frequency I/O Test Bus** - DC bias and low frequency (< 5 MHz) test points. Pins can be internally buffered when used as output.

Power Pins

Symbol	Pin Name	Pin Function
VCCD	11	**Digital + 5 VDC**
VCCD	17	
VCCD	23	
VCCD	28	
VCCS	40	**VCO + 5 VDC**
VCCA	3	**Analog + 5 VDC**
VCCA	48	
VCCA	52	
VCCA	56	
VCCA2	50	**Master Resistor + 5 VDC** - To be connected to the 20 kΩ external resistor, which is connected to REXT on the other end.
DGND	14	Digital Ground
DGND	20	
DGND	25	
DGND	37	
AGND	47	Analog Ground
AGND	49	
AGND	57	
AGND	60	
SGND	39	VCO Ground

FUNCTIONAL DESCRIPTION

System Operation

The DFE9952R is a Decision Feedback Equalization Signal Processor. There are three major operational modes supported by the device: Fixed Normal Operation, Adaptive Normal Operation and Supervised Training mode. This section will be a general overview of the DFE processor usage in all three of these modes.

The details about individual blocks are covered in the following section Circuit Description. This includes the required programming of the many registers.

Normal Operation

The DFE9952R DFE Signal Processor is used to write data to, and read data from a Head Disk assembly equipped with a read/write Preamplifier IC. The write data inputs of the Preamplifier must be differential PECL and directly control the direction of the write current. The read data outputs of the Preamplifier should be differential amplified head waveforms between 35 and 600 mVpp.

Normal operation is controlled by 3 asynchronous inputs: RDGT, $\overline{\text{WRTGT}}$, and SVOGT. The signal SVOGT overrides the other mode controls, RDGT and $\overline{\text{WRTGT}}$. RDGT in turn overrides $\overline{\text{WRTGT}}$. Data Read mode is defined by RDGT assertion. Data Write mode is defined by $\overline{\text{WRTGT}}$ assertion. SVOGT is asserted only to perform internal cancellations. There are no outputs of controls for use by the Preamplifier.

For Normal Data Read operation, the bypass ENDEC bit is reset and the ENSuprvsry bit is reset. Both of these are in Control register 1. For Training, the ENSuprvsry bit in Control register 1 is set.

Normal operation has 2 submodes: Fixed Tap, and Adaptive. Since the modes only differ in the Data Read portion, the differences will be covered in detail at that point.

DATA READ

Normal Data Read Operation has both a Fixed Tap submode and an Adaptive submode. The difference between the two is that the Fixed Tap submode has all data directed Adaptation (correction) to the Forward and Feedback filters turned off. These two filters have tap weights which can be adjusted during the Adaptation process to minimize the error in their output. It is recommended that the Adaptive submode be used.

The head readback waveforms from the Preamplifier are input to a Variable Gain amplifier. This regulates the output of the Prefilter to be constant. The AGC action begins at the start of the Preamble at maximum gain. The AGC control then decays the gain quickly to the set level.

The amplified waveforms are then input to a low pass continuous-time filter to reduce noise and bandlimit the signal. This specific filter is referred to as the Prefilter.

The Data Read mode uses the Decision Feedback core as its circuit of data detection. The Normal outputs of the Prefilter are applied to a squelching circuit (considered part of the Prefilter), and the output of this squelching circuit is connected internally to the DFE core.

The first part of the DFE core is the Forward filter. It is a continuous time transversal filter which shapes the input signal for sampling by the decision block. There are 5 taps (coefficients) and they must be programmed for optimal performance to starting values determined in the Supervised Training mode. They can be either adaptive during Normal Operation, or they can be fixed. It is recommended that at least 1 coefficient always be in Fixed mode. The function of the Forward filter is to transform precursor InterSymbol Interference (ISI) into postcursor ISI.

The next portion of the DFE is the sampler which is a Sample and Hold circuit controlled by the Timing Recovery clock running at the symbol rate. The sampled output enters one input of the Decision block at a summing junction. The other input to the summing junction is from the Feedback Filter. The previous 8 decisions (logic level outputs) are stored for feedback. The most recent 3 decisions select a value from an 8 level adaptive RAM lookup storage. The least recent 5 decisions are multiplied by adaptive linear coefficients. These selected values, the lookup and the linear, are combined. Their sum is the Feedback Filter output.

The output of the summing junction is applied to the Slicer block and the output of the slicer is the data decisions. When the summing junction input signal to the slicer is greater than a programmable threshold, the high logic level is generated. This serial stream of Slicer outputs is a reproduction of the write current waveform that recorded the pattern read from the disk.

In Data Read mode, the Timing recovery PLL, the VGA amplitude control and the Forward and Feedback coefficient adaptation all use Decision directed tracking. This term means the correction factor for all the closed loop functions is derived from the equalizer error. The input to the slicer and the output decision are subtracted, and this residual analog voltage, the equalizer error ε_k, is fed back for Decision directed control. The error ε_k is in control from just after the Preamble portion of the data until RDGT is deasserted.

The serial decision stream and the Timing Recovery clock are input to a postcoder, then to a 9 to 8 decoder function, and optionally through a de-Randomizer block. The user data then decoded is output, either in a nibble wide or byte wide interface, to the disk data path controller.

The Data Read mode is started by asserting the control signal RDGT. When this is done, the immediate minimum 100 symbol periods will be used for the Data frequency acquisition phase of the Data read. This field of Preamble should be from 100 to 244 symbol periods long. Prior to the assertion of RDGT, the Frequency Synthesizer should be programmed to the zone data rate. The Timing Recovery VCO should acquire the Frequency Synthesizer's output frequency before starting acquisition of the data frequency (initiating a Data read).

The disk data frequency is acquired by the Timing Recovery portion of the IC. The disk preamble readback frequency is 1/4 the sampling (symbol) frequency. The Timing recovery matches by taking samples at $(2n+1)\pi/4$ intervals. These are then internally compared and the VCO frequency adjusted.

Following 100 symbol periods (25 cycles of the amplified head waveform), the Sync Mark detection search starts. The Sync Mark can be out to 144 symbol periods later. Its length is 36 symbol periods. The operations of a Normal and a Training read separate after the Sync Mark detection. In Training, the user data is not output, but is used internally to

Train the equalizers (see Training below). The Normal Data Read will postcode the serial decision stream, deserialize it, 9 to 8 decode it, and, if enabled, de-Randomize. This recovered data will be output on pins NRZ7-NRZ0 if the byte wide mode is enabled, or on NRZ3-NRZ0 if in nibble mode. The user data portion of both types of Data Read mode continues until deassertion of RDGT. The signal SYNC remains high until the deassertion of RDGT.

DATA WRITE

The Data Write mode requires that RDGT be deasserted, SVOGT be deasserted, POWERON be deasserted, and then $\overline{\text{WRTGT}}$ to be asserted Low. Any change in controls terminates the write.

Data Write has the opposite direction of data flow. When the controller asserts $\overline{\text{WRTGT}}$, the inputs NRZ7-NRZ0 (byte mode) or NRZ3-NRZ0 (nibble mode) should be 0. They should be held at 0 until 1 byte of 0xFF is input to indicate the Sync Mark should be written. Following the Sync Mark, RWCLK clocks in write data on its rising edge. The data is optionally Randomized, 8 to 9 encoded, optionally precoded and optionally precompensated. The output of the precompensation block is the differential write current drive signal. The outputs WDOUT and $\overline{\text{WDOUT}}$ are Pseudo ECL level outputs to the Read/Write Preamplifier, which are direct representations of the write current to the head. This data path continues to write until $\overline{\text{WRTGT}}$ is deasserted, or one of the other two controls is asserted.

There is an ENDEC bypass mode which requires the datapath controller to write the Preamble, the Sync Mark and all data directly. The data presented on the NRZ bus is serialized directly and is written immediately at the very assertion of $\overline{\text{WRTGT}}$. No Preamble or Sync Mark are generated by the DFE9952R. The user must supply both of these patterns in his data. This ENDEC bypass mode is intended for test. In the ENDEC bypass mode, the Randomizer is not available, but the precoder and precompensation remain optional. The RWCLK will be set to the symbol VCO rate divided by 8 or by 4.

OTHER MODES

There is a ready reserve state where the signal POWERON is turned on prior to a data read or servo compensation. The Idle mode is the state where all controls are deasserted.

Supervised Training

The Supervised Training mode determines a set of coefficients for the Forward Filter and the Feedback Filter to be used during normal disk operations, both Adaptive and Fixed. Starting values for the Training mode can be obtained from Philips.

The Supervised Training mode is to take those starting values and then converge the coefficients of the filters to optimum values for a particular data rate and a particular head and disk surface combination. The digitized coefficient (tap weight) values read back after Training should be stored outside, and loaded into the Forward and Feedback filters when a zone change or head switch is done during Normal Operations in the drive.

The training is done with a pseudo-random data pattern written on the disk, then read back. During readback, the pattern known to be written on the disk is automatically substituted as the output of the decision block, and therefore as the input to the equalizer error calculation block. The normal adaptation, correcting coefficients for error, converges as it would in a user data disk read. After the read (or reads) complete, the coefficients are frozen, digitized and then read back through the serial port, and stored for future use. The registers should be set to autodigitize the coefficients. Approximately 20 µsec after the completion of the Training read, the digitization will be complete, and the microcontroller can read the coefficient registers. If the read of coefficients is done before the completion of digitization, the results are not guaranteed.

The first step in the Supervised Training is to load the registers for a write. The Frequency Synthesizer M and N values, Center Frequency value, VCO offset tuned value, (see VCO Tuning under Circuit Description), Delay Cell Calibration Values, and control registers are loaded. The Frequency Synthesizer should be allowed sufficient time to lock. The MR Bias current DAC and the Write Current DAC registers should be loaded with values appropriate for the particular head undergoing Training. The Data Generator Seed should be loaded (12 bits). The Bypass SM and Bypass ENDEC bits in Control register 1 (0x02) must be specifically reset for Training.

For Training, the ENSuprvsry bit in the Control register 1 is set.

The Prefilter frequency cutoff register, the AGC Bandwidth register, and the AGC Loop Gain register should be loaded for data read values.

The datapath controller should be set up to write the Preamble pattern (0x00 on NRZ data bus). Also, program 1 byte of 0xFF on the NRZ data bus for the Sync Mark. An arbitrary byte must be input as RWCLK clocks in data from the NRZ interface during the Write. This data is internally discarded and the Data Generator output is substituted. At this point, a disk write is done under normal datapath control.

A disk read should be setup by the drive. This includes loading the Starting values into the taps of the Forward and Feedback filters, and additionally a large value for both the RAM and linear Feedback filter and the Forward filter update multipliers.

Then initiate a disk read with the datapath controller. When the Sync Mark is detected, the Data Generator is started at the seed, and substitutes its known-correct values for the output of the Decision block. Since the Timing Recovery is driving this process, the values are matched to the samples being processed by the DFE core. The calculation of Mean Square error is done as normally, and the adaptive portions of both filters are updated. This adaptation continues until the end of the disk read. At that time, the values adapted to are frozen, digitized and read into the register where the Starting values had originally been placed.

The coefficients can be read out and stored, or additional cycles of Training done until values have converged further. In addition, more cycles of Training can be done with different patterns by changing the Data Generator seed value, writing to disk, and then reading back without writing new Starting values. There will be a Users Manual published which will cover the Supervised Training process, and the Starting values calculations, in detail.

Circuit Description

VARIABLE GAIN AMPLIFIER (VGA)

The VGA provides amplitude normalization and impedance transformation for differential read signals from the pre-amplifier. This low noise amplifier increases the signal amplitude from the pre-amplifier level to the level required by the Forward filter and decision blocks. The VGA will also maintain this signal level by adjusting its gain based on control voltage from the AGC circuit. Prior to the Sync Mark detection portion of a Data Read, the AGC control uses a peak detection, high Decay current mode. After the Preamble, the DFE equalizer error controls the gain. The AGC goes into HOLD mode after 100 symbol periods and then goes into Decision directed tracking mode after Sync Mark detection.

The VGA is fully-differential to maximize immunity to common-mode and power supply noise. The inputs to the VGA are AC-coupled from the pre-amplifier. In order to minimize write-to-read recovery time, the VGA inputs are placed into a low-impedance clamping configuration to allow for quick recovery of the AC coupling capacitors. The VGA inputs are clamped for a programmable period of time following deassertion of $\overline{\text{WRTGT}}$. They are also clamped when $\overline{\text{POR}}$ or $\overline{\text{SQLCH}}$ is asserted.

AUTOMATIC GAIN CONTROL (AGC) CIRCUIT

The AGC circuit adjusts the VGA gain to regulate the signal amplitude at the output of the Prefilter. Two separate feedback methods are employed to regulate the amplitude of the read data waveform. First, a continuous-time peak-detecting control loop is used to acquire the desired signal level during the Preamble portion of data fields. In the second method, when reading data, a decision-directed discrete-time algorithm regulates signal amplitude using equalizer error as the controlling signal.

The AGC starts each data acquisition with maximum VGA gain to ensure that low level signals can be acquired quickly. The acquisition is triggered by the rising edge of RDGT. The reference voltage is programmed in the AGCDataRef register (0x10). The amplitude out of the Prefilter will be 4 times the setting of this register differential peak to peak. Full scale reference output is .4V and the recommended setting is .25V. The VGA/AGC control feature is stabilized by a temperature compensated circuit design incorporating an exponential control characteristic.

The AGC loop is designed to settle within 7 peaks (or 3 1/2 cycles) for any 4 dB change of input signal amplitude. The VGA gain is directly controlled by the voltage on a 20 pF holding capacitor. The attack current charges the capacitor and

will increase the gain of the amplifier whereas the decay current, which equals 10 times of the attack current, discharges this capacitor and reduces the VGA gain.

The AGCDataBW register (0x12) sets the current during preamble acquisition for a data read. The attack current is programmable from 1 µA to 100 µA through a 6 bit DAC. During read mode, once the DFE9952R control state machine determines that timing and amplitude acquisition has been established, the AGC system feedback is taken from a discrete-time amplitude regulation loop controlled by equalizer error. The full scale charge current in decision directed mode is:

$$I_{AGC} = \frac{\varepsilon_k}{2k\Omega}$$

The current I_{AGC} is then multiplied by the μ_{gt} factor in the AGCTrack register (0x1E) will the following weights:

AGCTrack

AGCTrack<3:0> μ_{gt}	Current Multiplier
0000	0
0001	0.012
0010	0.037
0011	0.050
0100	0.110
0101	0.122
0110	0.147
0111	0.159
1000	0.330
1001	0.342
1010	0.367
1011	0.379
1100	0.440
1101	0.452
1110	0.477
1111	0.489

This allows the AGC system to compensate for media and track following induced amplitude variations.

When $\overline{\text{SQLCH}}$ is asserted, or following the rising edge of $\overline{\text{WRTGT}}$, the VGA input is clamped to a low-impedance state for a duration that is programmed from 0.2 µs to 3.2 µs by the VGASQ register (0x14).

The gain control voltage is frozen when it is not being updated in read mode. It can also be frozen by asserting $\overline{\text{AGCHOLD}}$. This allows the AGC to coast through areas where it is known that less than optimum amplitude regulation will be realized. The gain control value is maintained with minimal leakage when the control loop is frozen.

PREFILTER

The Prefilter removes high-frequency components of the read signal before it is supplied to the DFE Forward equalizer. This filter is a digitally controlled 5-pole, 0.05° equiripple linear phase filter. The Prefilter output can be monitored at the ATSTOX/ATSTOY pins with appropriate setting in the prefilter control register.

The Prefilter is designed using a fully-differential continuous-time circuit to maximize immunity to common-mode and power supply noise. The functional blocks are the filter core, the bandwidth control block, and the tuning block.

The filter core has a pair of outputs - the normal lowpass output. The Prefilter output is sent to the DFE block through offset cancellation circuit, which must be zero'd by periodic assertion of SVOGT.

The bandwidth control converts the register settings to analog controls to set the bandwidth of the filter. The tuning block normalizes the filter response characteristics. It is used to lock the filter's frequency response against the variations of process, temperature, and power supply voltage. The frequency synthesizer reference clock, SFREF, is used as the reference for tuning.

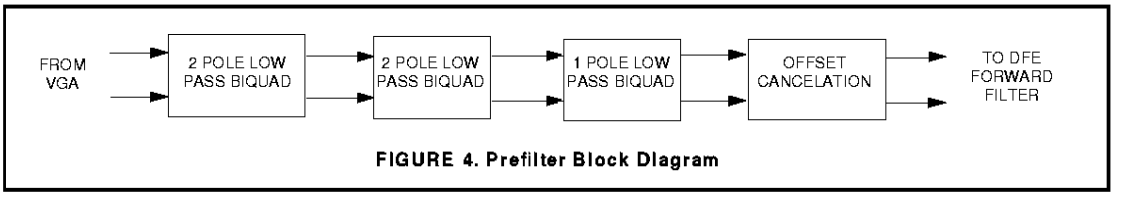


FIGURE 4. Prefilter Block Diagram

BANDWIDTH CONTROL

The PFBW register (0x17) controls the Prefilter Bandwidth. The low nibble sets the Data Cutoff frequency. The filter cutoff is the -3 dB frequency.

DatBW<3:0> of the PFBW register is used to set the prefilter cutoff frequency from 30 to 86.25 MHz at 3.75 MHz per step. Refer to Table below for detailed settings.

Prefilter Data Cutoff Frequency

DatBW<3:0>	BW (MHz)
0000	30.00
0001	33.75
0010	37.50
0011	41.25
0100	45.00
0101	48.25
0110	52.50
0111	56.25
1000	60.00
1001	63.75
1010	67.50
1011	71.25
1100	75.00
1101	78.25
1110	82.50
1111	86.25

TUNING CONTROL

A 5 bit register is used to adjust the on chip automatic tuning circuit to the input reference frequency SFREF, which could vary from 10 to 38.75 MHz. Note that the Frequency Synthesizer stipulates SFREF to be from 20 to 40 MHz. If the SFREF frequency is exactly equal to two table values, set PFRF<4:0> to the lower setting.

Prefilter Tuning

	Input	Freq (MHz)
PFRF<4:0>	Min Freq (MHz)	Max Freq (MHz)
00000	10.00	11.25
00001	11.25	12.50
00010	12.50	13.75
00011	13.75	15.00
00100	15.00	16.25
00101	16.25	17.50
00110	17.50	18.75
00111	18.75	20.00
01000	20.00	21.25
01001	21.25	22.50
01010	22.50	23.75
01011	23.75	25.00
01100	25.00	26.25
01101	26.25	27.50
01110	27.50	28.75
01111	28.75	30.00
10000	30.00	31.25
10001	31.25	32.50
10010	32.50	33.75
10011	33.75	35.00
10100	35.00	36.25
10101	36.25	37.50
10110	37.50	38.75

FORWARD FILTER

The forward adaptive filter is implemented using a continuous-time five-tap finite-impulse response (FIR) filter. The tap weights (coefficients) can either be fixed in value, set once during initialization, or they can be adaptive and will change during Read operations to minimize the calculated error.

The forward filter consists of a tapped delay line, tap weight multipliers, and circuitry to set and adapt the weights. The delay line has four delay cells and five taps. Each delay cell is an all-pass structure which has frequency independent time delay over the necessary range of input signal frequencies. The signal at each tap is multiplied by a coefficient and summed to form the output of the forward filter.

When in Adaptive mode, the FIR filter is adapted according to the equalizer error, ε_k, that is generated as a result of data decisions (in decision-directed mode) or the data generator output (in supervised training mode), each with an update multiplier that is user programmable. The transfer function of the forward filter is determined by:

$$f(t) = \sum_{i=0}^{4} y\left(t - iT_d\right) \times w_i$$

where *y(t)* is the continuous read data output from the Prefilter, T_d is the delay time of the delay cells and w_i is the coefficient (or tap weight) of the forward filter. The subscript *i* refers to the tap number of the five taps.

Offset Cancellation

The Forward filter offsets are cancelled every time SVOGT is active. During this mode, the Prefilter squelches its output stage so the Forward filter will see a zero input. The offset cancellation block inside the decision block then uses the 1MHz clock to compensate for any offset through the Forward filter. Every SVOGT must be at least 2 µsec. long. At least 150 SVOGTs should occur after Delay Cell Calibration, or reload of the DCCalVal register (0x62), and before doing a Data Read.

Delay Cell Calibration

The calibration circuitry sets the value of the delay time used in the Forward filter. The range of the delay time is between 4 to 14 ns. The DCCalVal register (0x62) is used to store the value, and after the calibration, it should be read and stored elsewhere.

The Frequency Synthesizer has an output at 1/16 the symbol frequency. This is input to a quadrature phase detector so that phase match is obtained at 90°. The derived tuning voltage then sets each of the four delay elements to one symbol period in delay length. The tuning needs to be done during final test of the manufacturing of the disk drive for each data rate (zone), and before any Supervised Training for any head or zone. This is because Supervised Training assumes a successful Read can be accomplished.

The DCCalVal register must be loaded at least 150 SVOGT assertions before the Forward filter offsets can be guaranteed to be zero'd.

Tap Weight Initialization and Update

The tap weights are coefficients of the linear filter. They are optimized during the adaptation process using the least mean square (LMS) algorithm:

$$w_{i,\,k+1} = w_{i,\,k} + \mu_{ff} \times \varepsilon_k \times \mathrm{sgn}[y(t - iTd)]$$

where w_k is the tap weight vector, *y(t-iTd)* is the local delayed value at the *ith* tap of the delay line, ε_k is the error signal derived from the decision feedback block and μ_{ff} is the tap weight update multiplier that is programmable by the FFGain register (0x65). This parameter is chosen on an empirical basis. This is covered in detail in the Users Manual on Starting Values for Training.

The FFGain register (0x65) has the following values:

Forward Filter update

FFGain<2:0>	Update Multiplier
111	0.1
110	0.05
101	0.025
100	0.0125
011	0.01
010	0.005
001	0.0025
000	0.00125

In Fixed Normal Operation, these taps are only initialized. The value loaded into the Forward Filter tap weight registers will not change. In Adaptive Normal Operation, the updates to the tap weights may occur continuously when data is read, either during Supervised Training or Normal Adaptive Operation.

The coefficients can be frozen by resetting the bits<4:0> in the AdaptFFTap register (0x63). When an individual bit is reset, all adaptation for that tap is disabled.

At least one tap should always be operated in fixed mode by resettting its bit.

The FFWn tap weight registers (0x5D-0x61) have the following value range:

Forward Filter taps

FFWn<7:0>	Nominal Tap Weight
00000000	+1.000
10000000	0
11111111	-1.000

The three operating modes of the coefficient updating circuitry are adaptation, digitization, and initialization. Initialization is done when the tap weights are loaded via register. The lowest FFWn register, FFW0 or (0x5D) corresponds to the undelayed input of the Forward Filter. The highest FFWn register, FFW4 or (0x61) is the tap for the output of the last delay cell. Initialization time is around 4 µs.

The adaptation process runs during read mode, if enabled. In the adaptive mode, the initialization of the filter tap weights is done in the same manner as the fixed tap mode. The taps will be adapted during data reads. The Adaptation will not start until after the Sync Mark has been detected. The autodigitize function is used to capture the tap weights after adaptation during RDGT. The AutoADC bit of the ADCntl register (0x30) should be set. At the deassertion of RDGT, the autodigitize function will start. It will complete digitizing the new, adapted values about 20 µsec. after a Read is complete. If a serial port read of tap weight or RAM register values is attempted in either the Forward or Feedback filters before they are completely digitized, the autodigitization operation is stopped and the values not held. The adapted to values are held during Idle, Write, and Servo modes. Initialization does not have to be redone after Sleep mode.

Values read should be used to load the register after power up or zone changes.

In Fixed Normal Operation, the values will be held continuously, and not Adapt during all modes.

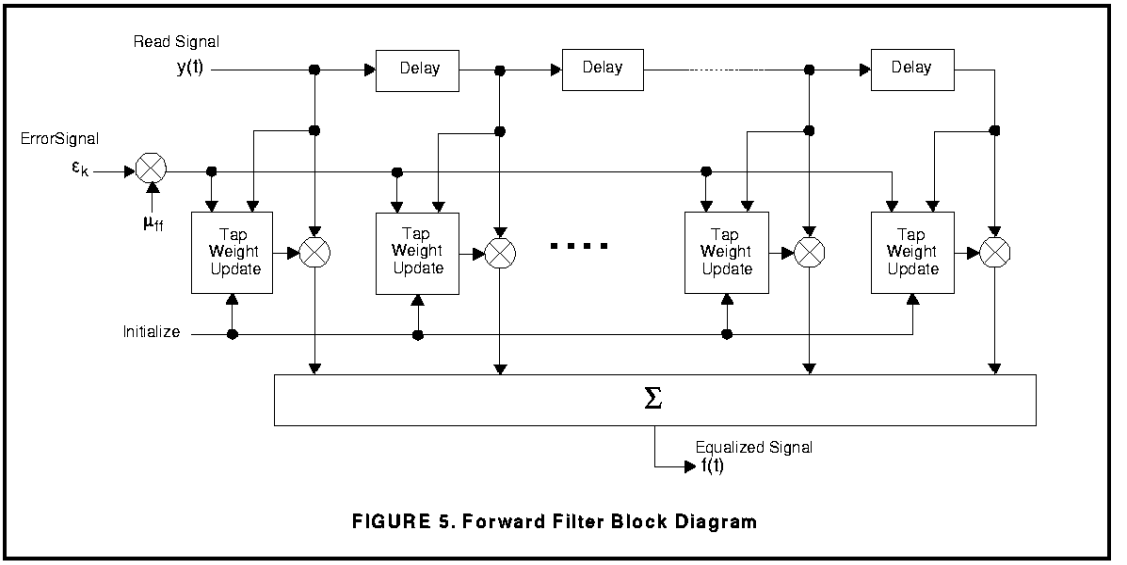


FIGURE 5. Forward Filter Block Diagram

SAMPLER

The sampler converts the continuous-time output of the forward adaptive filter into a discrete-time signal.

This is done for two reasons:

1. The timing recovery needs a sampled output of the equalizer error ε_k to calculate VCO clock phase error.
2. With a discrete-time signal, the subtraction of the feedback filter output is independent of timing, within the same clock cycle.

The sampling frequency is extracted from the input data waveform and is equal to the code frequency. The sampled output is one of the inputs to the Decision block summing junction.

FEEDBACK EQUALIZER

The feedback adaptive filter is used to remove both the linear and non-linear trailing ISI. The Feedback Equalizer is a hybrid architecture consisting of a linear feedback filter and a RAM-based equalizer.

The most recent decisions go through an 8-bit shift register. The most recent three decisions are used to address the RAM look up table. The five least recent decisions are the taps for the FIR filter. These five decisions are multiplied by the coefficients and the sum of the products are the output of the linear feedback equalizer. The lookup table output and the linear filter output are summed. This sum is the Feedback Equalizer output and is one of the inputs to the summing junction ahead of the Decision Block. The total Feedback output is:

$$r_k = RAM\ [X_{k-1},\ X_{k-2},\ X_{k-3}] + \sum_{j=0}^{4} b_{j,k} \times X_{k-(j+4)}$$

Both the linear feedback block and the analog RAM block use the error signal ε_k generated by the decision circuitry for adaptation purpose.

RAM FEEDBACK FILTER

Analog RAM cells are included in the feedback equalizer to cancel out the non-linear ISI effect. Each cell consists of three functional blocks: the current DAC used during fixed tap operation; the integrator used during adaptive operation and switching circuitry for output selection and mode control.

During adaptation, the update of the presently addressed cell location is:

$$ram_{k+1} = ram_k + \mu_{ram} \times \varepsilon_k$$

where ram_k is the value of the currently addressed location in the RAM and μ_{ram} is the update multiplier ranging from 0.00125 to 0.1 and is programmable by RGain<2:0> of the FBFGain register (0x41).

RAM Feedback update

RGain<2:0>	Update Multiplier
111	0.1
110	0.05
101	0.025
100	0.0125
011	0.01
010	0.005
001	0.0025
000	0.00125

LINEAR FEEDBACK FILTER

There are 5 cells in the linear feedback filter. The 5 least recent decisions of the previous 8 (from the shift register) are connected to each of these cells. The outputs of all 5 cells are summed to form the linear feedback output. Similar to the RAM feedback filter, the linear feedback filter consists of three functional blocks: the current DAC, the integrator and the switching circuitry. The difference is that decisions are used directly to modify the signs of the tap weights and input error signal. The update of the each cell is determined by:

$$b_{i,\,k+1} = b_{i,\,k} + \mu_{fb} \times \varepsilon_k \times x_{k-(i+4)}$$

where b_k is the tap weight value, μ_{fb} is the linear feedback filter tap weight update multiplier that is programmed by LGain<2:0> of the FBFGain register (0x41) and x_{k-i} is the bit in the shift register that corresponds to the tap weight b_{i-k}.

The values of the taps are below:

Feedback Filter taps

FFWn<7:0>	Nominal Tap Weight
00000000	-1.000
10000000	0
11111111	+1.000

Linear Feedback update

LGain<2:0>	Update Multiplier
111	0.1
110	0.05
101	0.025
100	0.0125
011	0.01
010	0.005
001	0.0025
000	0.00125

FEEDBACK FILTER OPERATION

The feedback filter operates in two different modes: fixed tap mode and adaptive mode.

In fixed tap mode, the tap weight of the linear feedback cells and the values of the lookup RAM are loaded through serial interface. This is done by loading the RFBn registers (0x50 - 0x57) for the RAM feedback filter and LFBn registers (0x58 - 0x5C) for the linear feedback filter. All tap weights stay constant during operation, i.e. there is no adaptation done during Read mode. The lowest number RFBn register corresponds to a decision of {-1, -1, -1}. The lowest number LFBn register corresponds to the fourth most recent decision and the highest LFBn register to the least recent (8).

In the adaptive mode, the initialization of the filter tap weights is done in the same manner as the fixed tap mode. The taps will be adapted during data Reads, and the adapted to value held during Idle, Write, and Servo modes.

The autodigitize function will allow the new, adapted values to be read about 20 µsec. after a Read is complete. If a read of values is attempted in either the Forward or Feedback filters before they are completely digitized, the autodigitization operation is stopped and the values not held.

Initialization does not need to be done after Sleep mode.

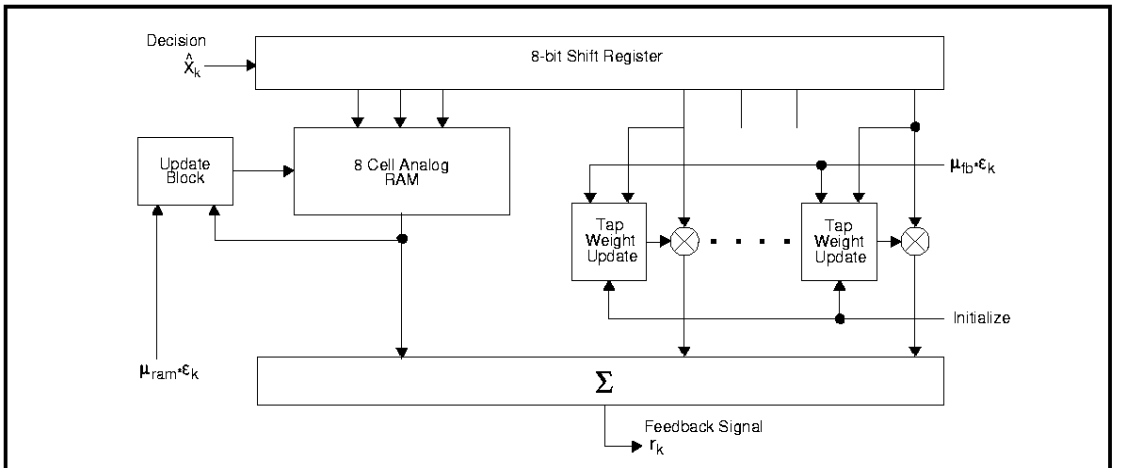


FIGURE 6. Feedback Filter Block Diagram

DECISION GENERATOR

The decision block combines the sampled forward filter output f_k and the feedback filter output r_k to generate z_k. The signal z_k is the fully (forward and feedback) compensated signal. The decision block utilizes a slicer to make the decision x_k. The slicer is an analog comparator which compares the summer output with a single, dc threshold. The threshold value is programmable by the SlicerThresh register (0x1D). If the summer output is above the dc level, the decision is made that the write current flowed in one direction. If the summer output is below the threshold, then the write current was in the opposite direction. The output serial stream from the Decision block reproduces the direction of the write current which recorded the head readback waveform. The Decision block also contains the equalizer error generation as well. The error ε_k is generated from z_k and x_k, the decision. The error is used to adapt the forward and feedback filters, adjust the AGC gain, and to synchronize the timing recovery clock.

There is also a register for d_k, which should be programmed to a factory set value.

Equalized Signal:

$$z_k = r_k + f_k$$

$$\hat{x}_k = \text{sign}\left(z_k\right) \quad \text{if threshold} = 0$$

$$\varepsilon_k = x_k \times \left(\left(d_k\right) - z_k\right)$$

FREQUENCY SYNTHESIZER

The DFE9952R contains a programmable frequency synthesizer that generates a low-jitter write clock (WrtClk). The write clock frequency is programmed through the serial interface. It is specified as the frequency of a reference clock (SFREF) multiplied by a ratio of two integers.

$$F_{WrtClk} = \frac{8(M+1)}{(N+1)} \times F_{SFREF}$$

The frequency synthesizer is a phase-locked loop (PLL) with a divide by 8 pre-scaler, and a programmable 6 bit divider (M counter) in the feedback path. Another programmable 6 bit frequency divider (N counter) is used to divide down the SFREF frequency. By phase comparing the frequency-divided clocks, the synthesizer VCO output (WrtClk) will achieve the desired frequency once the PLL is locked.

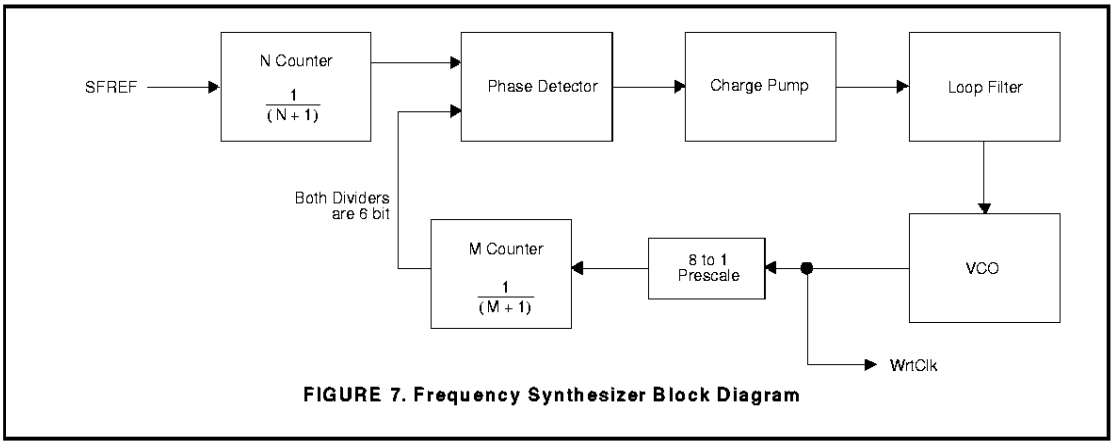


FIGURE 7. Frequency Synthesizer Block Diagram

The synthesizer PLL includes a digital phase detector, fully differential charge pump with selection of four charge pump currents, programmable on-chip loop compensator with four choices of pole/zero frequencies and a narrow-range, fully differential VCO with 16 overlapping frequency bands.

Charge pump current is varied as follows:

Synthesizer Current

i_pmp<1:0>	Charge Pump current
00	16.67µA
01	22.22µA
10	27.78µA
11	33.33µA

SYNTHESIZER LOOP FILTER

The synthesizer PLL loop filter is of the integrator-pole-zero type and is internal to the DFE9952R. Its zero and pole frequencies are programmed by lpf 1:0> of the SynthN register (0x22). Bits <7:6>.

The nominal zero/pole frequencies are as follows:

Pole/Zero Frequency

ipf<1:0>	Zero ------ Pole
00	11.9 kHz / 572.9kHz
01	13.7 kHz / 661.0 kHz
10	16.2 kHz / 781.2 kHz
11	19.8 kHz / 954.8 kHz

VCO

The fully differential VCO is identical to the Timing recovery VCO in design. Both of the VCOs require loading registers to adjust their center frequency. The table below lists nominal values to be used for both the SynthCF register (0x23) and TRCintl2 register (0x26).

VCO Center Frequency

Band Number	Nominal fcenter (MHz)	register 0x23, 0x26 contents
0	78.26	0x10
1	88.04	0x21
2	97.83	0x22
3	107.61	0x23
4	117.40	0x24
5	127.17	0x25
6	136.96	0x26
7	146.74	0x37
8	156.52	0x38
9	166.30	0x39
10	176.09	0x3A
11	185.87	0x3B
12	195.65	0x3C
13	205.43	0x4D
14	215.22	0x4E
15	225.00	0x4F

VCO CENTER-FREQUENCY CALIBRATION

In order to guarantee the relationship between the VCO center frequency and the frequency programming, it is necessary to calibrate the synthesizer VCO center frequency. This calibration must be done prior to attempting to lock the synthesizer.

The calibration process utilizes the existing M and N dividers of the synthesizer. By carefully selecting the M and N values, the divided reference frequency and the desired divided center frequency are made as close to each other as possible. The VCO control voltage is set to zero and a 4-bit offset DAC is initially set to 0x0 to bring the VCO frequency below the target center frequency. The two divided frequencies are compared to each other. If the divided VCO frequency is below that of the reference, the offset DAC is incremented by one step to increase the VCO frequency. This process is repeated until the divided VCO frequency is just above that of the reference. At this point, the offset DAC is held and the VCO center frequency is established. Since the data VCO is the same as the synthesizer VCO, the data VCO is calibrated at the same time. The offset DAC value should then be read back and stored for future use.

To calibrate the VCO center frequency, the M and N values must first be selected and loaded into the SynthM and SynthN registers (0x21 & 0x22). Next, load the SynthCF register (0x23) with the appropriate frequency band setting. The VCO center-frequency calibration process is started when the start_cf_calib bit in the TRCalib register (0x24) is reset, then set. While the calibration is in progress, the cf_calibrating bit will be set. If the VCO center frequency is above the range of the offset DAC, then the cf_overflow bit will be set. The logic is not designed to detect if the VCO center frequency is below the range of the offset DAC. If only one frequency can be calibrated, the highest zone frequency used in the application should be the one used.

When the VCO center frequency is not being calibrated, i.e. the cf_calibrating bit is not set, the offset DAC can be loaded through the serial interface.

TIMING RECOVERY

In the read mode, the VCO frequency and phase are adjusted to lock to the incoming read signal. The system first acquires the correct frequency and phase using an acquisition preamble - 4T pattern (1/4 of the symbol rate).

ZERO-PHASE RESTART

The VCO is started synchronously with the preamble to reduce the acquisition time. (This is commonly known as zero-phase restart, (ZPR)). At the assertion of RDGT, the ZPR circuit counts two analog cycles. A fixed comparator is armed, and when the input waveform next crosses the threshold, the VCO is started synchronously.

TIMING ERROR

Immediately after a zero-phase restart, the timing control attempts to acquire phase lock to the incoming signal. In both the acquisition mode and tracking modes, the timing error is calculated as follows:

$$\tau = \varepsilon_k \, \mathrm{sgn}[f(k-1)] - \varepsilon_{k-1} \, \mathrm{sgn}[f(k)]$$

In all non-read modes, the data VCO is locked to the frequency synthesizer output frequency.

SYNC MARK DETECTION

After the data VCO enters data tracking the DFE9952R searches for the sync mark written between the preamble and data. Locating the sync mark identifies the start of customer data and frames the read data bits into the correct byte boundaries for decoding.

This operation is important for three reasons:

1) the read data cannot be properly decoded unless the byte boundary is established,

2) the data randomizer must be initialized to its seed value for the first byte of data.

3) the data generator must be initialized to the programmable seed value to match the incoming read data under supervisory training mode.

The read acquisition mode time is a minimum of 100 symbol periods, and can be up to 16 bytes (144 symbol periods) longer. After the minimum 100 symbol periods, the DFE9952R enters read tracking mode and Sync Mark detection is started.

The Sync Mark must be found before the number of user bytes programmed for the Sync Timeout. The time-out period is programmed as SMTO<3:0> in the SyncTol register (0x04). The number of errors allowed in Sync Mark detection is programmed in the SMTol<2:0> bits in the same register.

If the Sync Mark is detected, the Read mode continues until RDGT is deasserted. If the Sync Mark is not found within the time-out period, the Read mode is aborted.

The sync mark is a (1,3) RLL encoded pattern:

$0100\ 0100\ 1000\ 1010\ 0101\ 0010\ 1001\ 0001\ 0010_2$

The Sync Mark is exactly 4 user bytes long. The pattern is fixed.

It is possible to force the DFE9952R to complete the Read mode by setting the BypassSM bit in the Control1 register (0x02). In this case, the Read mode continues until RDGT is deasserted. This is a special test hook that is used only when the ENDEC is also bypassed. Otherwise, the read data cannot be properly decoded when the Sync Mark is not detected.

NRZ INTERFACE

The NRZ interface is a bi-directional data interface that communicates with the disk controller to transfer read/write data. In the Write mode, the data to be written onto the disk is transferred from the disk controller to the DFE9952R. In the Read mode, the data read from the disk is transferred from the DFE9952R to the disk controller. The DFE9952R supports both 8-bit and 4-bit data transfer across the NRZ interface. The width of the NRZ interface can be selected by programming the NRZWidth8 bit in the Control1 register (0x02). When NRZWidth8 is set, the NRZ interface is eight bits wide, and data is transferred via the NRZ7:0 pins. When NRZWidth8 is reset, the NRZ interface is four bits wide, and data is transferred via the NRZ3:0 pins.

In the Write mode, the disk controller must start by transferring a minimum of 14 bytes of 0x00 across the NRZ interface. These bytes of 0x00 indicate to the DFE9952R to write the preamble. The disk controller must then transmit exactly one byte of 0xFF to initiate the writing of the Sync Mark. After one byte of 0xFF, the customer data must follow. Since the actual Sync Mark is four bytes in length, the customer data has three bytes buffered in the DFE9952R. This buffering and other delays in the write data path result in a 7 byte latency delay. The disk controller must account for this by writing arbitrary pad bytes at the end of the customer data.

In the DFE9952R design, there are actually three phases to Write mode. At $\overline{\text{WRTGT}}$ assertion, preamble is written until a byte of 0xFF is transferred across the NRZ interface. The Sync Mark is then generated and written. After 4 user byte times the user data transferred across the NRZ interface is written.

In the Read mode, the DFE9952R will transfer 0x00 across the NRZ interface until the Sync Mark is detected. One byte of 0xFF will be transferred to indicate Sync Mark detection. The user read data is then transferred.

In Supervised Training mode data is transferred after the Sync Mark, both in Write and Read modes. However, the Write data is not written to the Preamplifier and the Read data is not the recovered data from the disk.

In the 4-bit NRZ mode, one byte of data is transferred as two 4-bit nibbles. There is no specific indication of which nibble is MSB or LSB. It is up to the disk controller and the DFE9952R to frame these nibbles into bytes based on the detection of the Sync Mark across the NRZ interface.

Data across the NRZ interface is strobed by the clock at the RWCLK pin. In both Read and Write modes, the data must be/is valid at the rising edge of RWCLK. The RWCLK is active and available to the disk controller in read, write, servo, and standby modes. However, if the DisRWCLK bit in Control1 register (0x02) is set, the RWCLK is active only in read and write modes. The RWCLK is generated from the frequency synthesizer WrtClk during non-read mode. During the read mode, RWCLK is generated from the Timing recovery VCO. During the clock source switching, RWCLK will exceed its nominal clock period. However, it will not glitch or produce a clock period that is smaller than nominal.

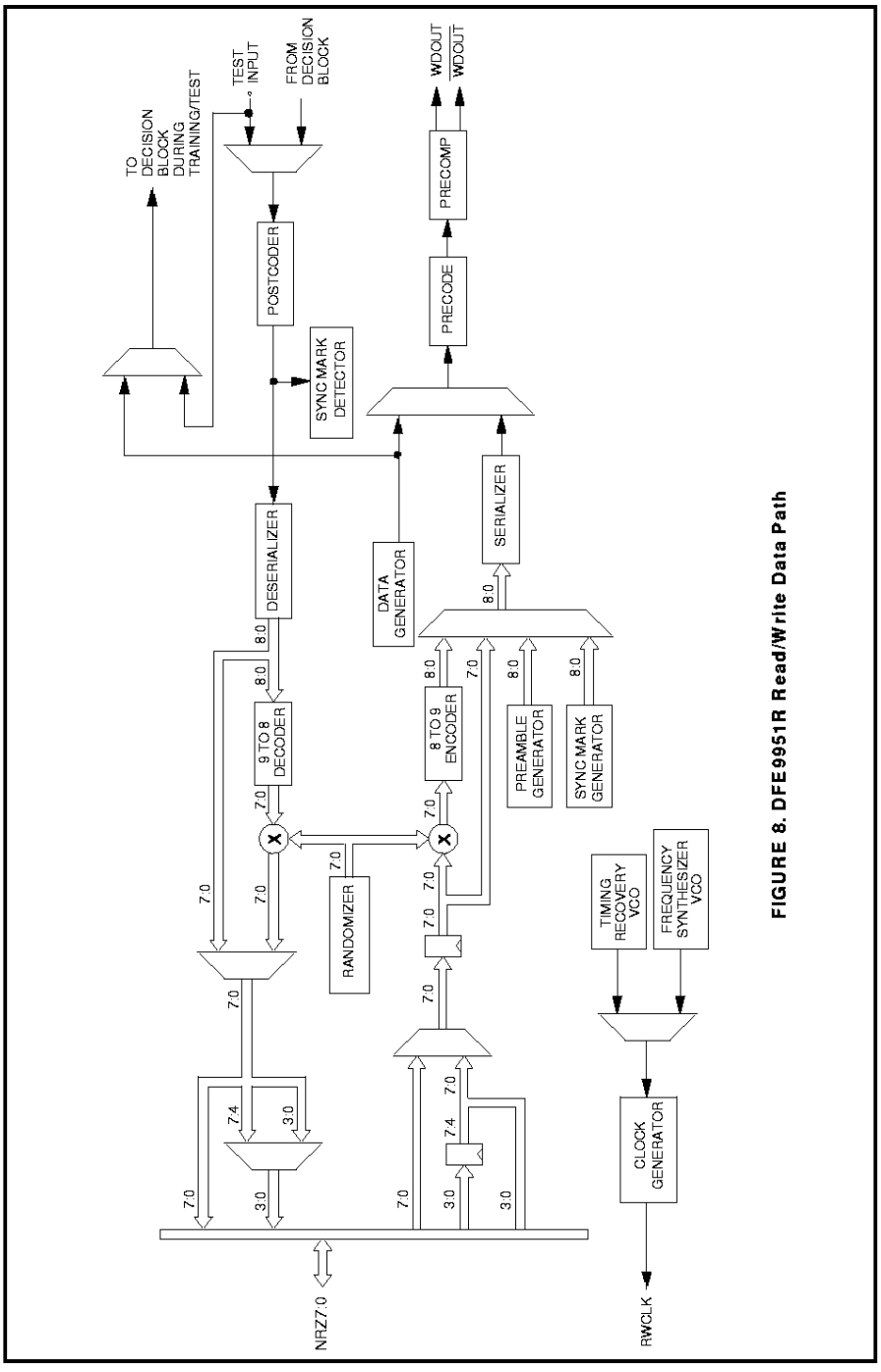


FIGURE 8. DFE9951R Read/Write Data Path

ENDEC

The DFE9952R uses an industry standard 8/9 (0,4/4) ENDEC for converting user data into codewords written to disk. This is done to ensure sufficient transitions are written to maintain phase lock of the Timing Recovery in readback.

During Write, the ENDEC outputs 9 symbols for every 8 input user data bits. During Read, the ENDEC translates 9 symbols into 8 output user data bits.

The internal ENDEC can be bypassed by setting the Bypass ENDEC bit in Control1 register (0x02). When bypassing the ENDEC, the codewords, written to disk, or read from disk, are directly transferred directly on the NRZ interface. On readback, the codewords are not byte-aligned on output.

When bypassing the ENDEC, the protocol for transferring preamble and Sync Mark are no longer valid. The pre-encoded preamble (1/4T) and Sync Mark must also be generated by the disk controller and transmitted across the NRZ interface. In the Bypass mode, the DFE9952R does not generate any preamble or Sync Mark internally. Additionally, the RWCLK will have a shorter period, 8/9ths of nominal. This is because only 8 bits of codeword are written/read for every RWCLK rather than 9 symbols when the ENDEC is not bypassed.

When the ENDEC is enabled, the Randomizer can either be on or off. When the ENDEC is bypassed, the Randomizer is always off.

DATA RANDOMIZER

In the DFE9952R, the randomizer can be selectively enabled or disabled by setting the EnRandom bit in the Control1 Register (0x02) to set or reset. Data written with the data randomizer enabled cannot be recovered with the data randomizer disabled, and vice versa. When the ENDEC is bypassed, the data is not randomized regardless of the state of the EnRandom bit.

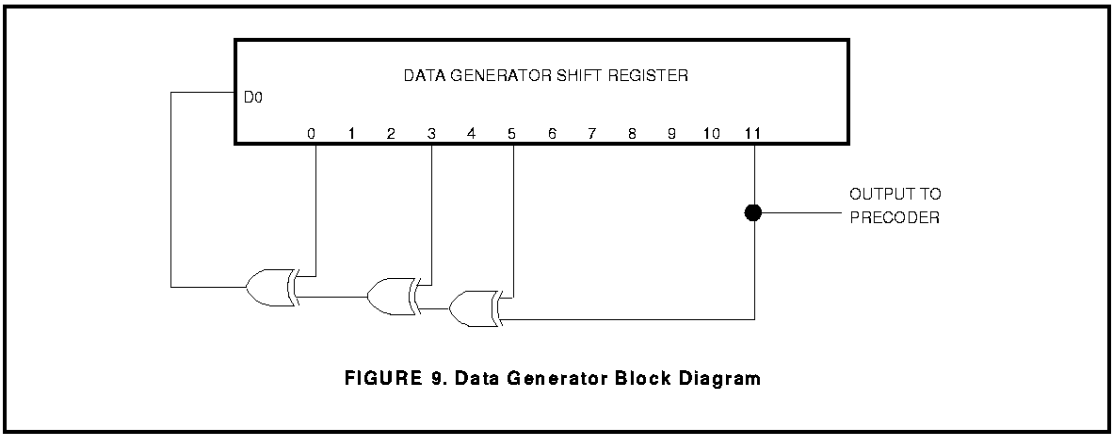


FIGURE 9. Data Generator Block Diagram

DATA GENERATOR

The DFE9952R contains a data generator that generates a pseudo-random data pattern used for various testing and functional purposes. The data generator is basically a linear-feedback shift register (LFSR) with corresponding control logic to reset, hold, and enable the data generator. The feedback initial seed value is programmable up to 12 bits. The high order bit must be zero (0). The pseudo-random data pattern generated is used to write the data for Training. When a read is done during Training, the LFSR pattern is substituted for the output of the decision block. This forces the equalizer error to be the value it should be, even if the decision was incorrect, and adapts the equalizers.

The block diagram of the data generator is shown in the figure above. The feedback polynomial is fixed and is of degree 12:

$$x^{12} + x^6 + x^4 + x + 1$$

WRITE PRECOMPENSATION CIRCUIT

The DFE9952R includes a write precompensation circuit to shift the write data edges in order to reduce the amount of inter-symbol interference (ISI) effects. The precomp algorithm delays a magnetic transition whenever it is preceeded by a transition in the previous clock cycle. Since ISI compensation requires adjusting the relative distance between adjacent magnetic transitions, the time delay is therefore specified as a percentage of the symbol-clock period to accommodate zone recording. The amount of delay is programmable in 5% steps up to 30% and is controlled by Precomp register (0x0D).

Write precompensation can be done even if the data is not precoded. The precoder can be bypassed by setting the BypassPrecoder bit in Control 1 register (0x02).

Bypassing the Precoder is only for test modes. The Postcoder is in-circuit at all times. Therefore user data should be Precoded if the data must be recovered.

The following table shows the value of the Precompensation that can be programmed.

Delay set

Precomp<2:0>	Delay (%T)
000	5
001	10
010	15
011	20
100	25
101	30

WRITE CURRENT DAC

The DFE9952R includes a 6 bit DAC to control head write current. WriteDAC<5:0> of WriteDAC register (0x0B) controls an output sink current from 0.5 mA to 2.5 mA. The write current DAC is enabled only when $\overline{\text{WRTGT}}$ is asserted (Low). In all other modes, the write current DAC is shut off to reduce power consumption.

MR BIAS CURRENT DAC

The DFE9952R has a programmable head bias current DAC for MR preamp applications. The current available is from 0.1 mA to 1.6 mA. The current is programmed through bits MRDAC<5:0> of the MRDAC register (0x0C). The MR Bias DAC is turned off only when $\overline{\text{WRTGT}}$ is asserted (Low).

SERIAL INTERFACE

The DFE9952R contains a serial interface that allows the microprocessor to program the internal registers. It consists of three signals: $\overline{\text{SDEN}}$, SCLK, and SDATA. Both the $\overline{\text{SDEN}}$ and SCLK lines are driven by the microprocessor to the DFE9952R. The SDATA line is bi-directional to allow data transfer to/from the DFE9952R. The $\overline{\text{SDEN}}$ line is asserted low only during address/data transfer. It must be deasserted to the high state after each address/data transfer to terminate the transfer cycle before the next transfer cycle can begin. During the time that the $\overline{\text{SDEN}}$ line is asserted, the SCLK line must switch exactly 16 cycles to clock 16 bits of address/data transfer. Each data bit is clocked on the rising edge of SCLK. In addition, there must be exactly 1 SCLK after the deassertion of $\overline{\text{SDEN}}$. After that one clock, SCLK is ignored when $\overline{\text{SDEN}}$ is not asserted. (However, it would be best not to switch SCLK when it is not necessary in order to reduce noise and power.)

A transfer cycle consists of transfer of the register address, a $\overline{R}$/W mode bit, a don't care bit, and the register data. The $\overline{R}$/W mode bit and the register address is always transferred from the microprocessor to the DFE9952R. The register data can be written to or read from the DFE9952R. The first six bits transferred is the register address with the MSB transferred first. The next bit transferred is the $\overline{R}$/W mode. It indicates the direction of register data transfer. The register data is written to the DFE9952R if the $\overline{R}$/W mode bit is set. Otherwise, the register data is read from the DFE9952R. The next don't care bit allows SDATA to turn around in case of a read operation. Finally, the last eight bits transferred are the register data with the MSB transferred first.

POWER MANAGEMENT

The DFE9952R operates in four power-management modes: read mode, write mode, standby mode, and sleep mode. Power management features are designed into the DFE9952R with the intention of reducing the maximum power dissipation during not only read mode but also in all other operating modes in order to minimize average power consumption in the disk drive.

The Read, Write, and Servo modes are the active modes. Transition from any active mode to another active mode must pass through the standby mode. The important timing parameters of power management are the wakeup times allowed for each circuit when transitioning from standby mode to each of the active modes.

A manual override is provided via the serial interface to keep individual blocks powered-on in all operating modes except the sleep mode.

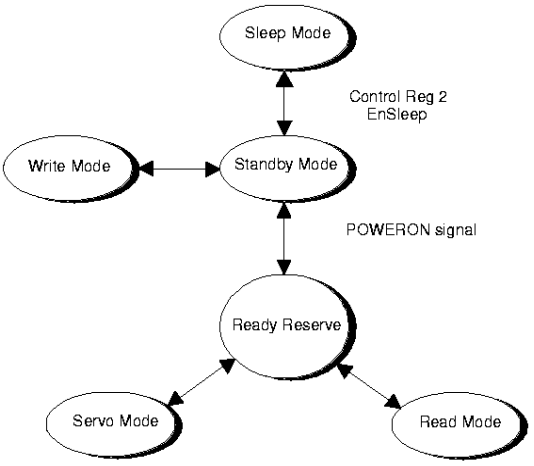


FIGURE 10. Operating Mode Transition Diagram for Power Management

READ MODE

The DFE9952R is in the read mode when RDGT is asserted. At least 5 µsec before RDGT, the signal POWERON must be asserted. In the read mode, all write data path logic is powered-down. This includes the write current DAC, the precompensation logic, and the serializer. The Sync Mark detection circuit is active only from the beginning of the read mode until the end of the sync mark search operation, i.e., sync mark found or time-out.

SERVO MODE

The DFE9952R is in the servo mode when SVOGT is asserted. In the servo mode, the offset cancellation of the Forward filter is done. SVOGT duration must be a minimum of 2 µs for offset cancellation to be done. The SVOGT period is a maximum of 100 µs.

To enter Servo Mode, first assert the signal POWERON, then at least 5 µsecs later, assert SVOGT.

WRITE MODE

The DFE9952R is in the write mode when $\overline{\text{WRTGT}}$ is asserted. In the write mode, most of the DFE9952R chip is powered-down. The powered down blocks include the VGA, AGC, Prefilter, forward adaptive filter, feedback adaptive filter, sampler, slicer, and sync mark detector.

STANDBY MODE

The DFE9952R is in the standby mode when the signals POWERON and $\overline{\text{WRTGT}}$ are deasserted. The only two mode switches are to Write and to Ready Reserve when $\overline{\text{WRTGT}}$ or POWERON are asserted, respectively.

SLEEP MODE

The DFE9952R is placed in and out of the sleep mode only by programming through the serial interface. Individual power management override controls are ignored in sleep mode. While in the sleep mode, all registers shall maintain their contents.

REGISTER DESCRIPTION

Addr	Name	Description							
0x00	SerIntf	Serial interface register - (serial I/O section)							
		Reg Bank	Chip Reset						
0x01	Status	Status register - (ENDEC section)							
		Alarm	OpMode <1>	OpMode <0>	Mode Error		SMNot Found		
0x02	Control1	Control1 register - (ENDEC section)							
		NRZ Width8	Enab Random	Bypass SM	En Supvsry	Bypass Endec	Dis RWCLK	Bypass Precomp	Bypass Precoder
0x03	Control2	Control2 register - (ENDEC section)							
		En Sleep	Dis EndPdn	EnRd Test					
0x04	SyncTol	Sync mark detection error tolerance and time-out count (ENDEC section)							
			SMTol <2>	SMTol <1>	SMTol <0>	SMTO <3>	SMTO <2>	SMTO <1>	SMTO <0>
0x05	DGSeed LSB	Data generator seed value (ENDEC section) (LSB)							
		DGSeed <7>	DGSeed <6>	DGSeed <5>	DGSeed <4>	DGSeed <3>	DGSeed <2>	DGSeed <1>	DGSeed <0>
0x06	DGSeed MSB	Data generator seed value (ENDEC section) (MSB)							
						DGSeed <11>	DGSeed <10>	DGSeed <9>	DGSeed <8>
0x07	RefClkDiv	Reference clock divider. (ENDEC section)							
			DC50K	RefDiv <1>	RefDiv <0>	ClkDiv <3>	ClkDiv <2>	ClkDiv <1>	ClkDiv <0>
0x08 - 0x0A	Reserved								
0x0B	WriteDAC	Programmable write current DAC value. (write data section)							
		WriteDAC Off		Iwrite<5>	Iwrite<4>	Iwrite<3>	Iwrite<2>	Iwrite<1>	Iwrite<0>
0x0C	MRDAC	Programmable MR bias DAC value (write data section)							
		MRDAC Off		IMR<5>	IMR<4>	IMR<3>	IMR<2>	IMR<1>	IMR<0>
0x0D	Precomp	Programmable precomp delay selection. (write data section)							
		Dis WD PDn				Precomp Test	Precomp <2>	Precomp <1>	Precomp <0>
0x0E	Reserved								
0x0F	Reserved								
0x10	AGC DataRef	AGC data mode reference level (VGA/AGC section)							
			AGC DataRef <6>	AGC DataRef <5>	AGC DataRef <4>	AGC DataRef <3>	AGC DataRef <2>	AGC DataRef <1>	AGC DataRef <0>
0x11	Reserved								

Addr	Name	Description							
0x12	AGC DataBW	AGC DatBW mode bandwidth (VGA/AGC section)							
		Dis VGAPDn		AGC DatBW <5>	AGC DatBW <4>	AGC DatBW <3>	AGC DatBW <2>	AGC DatBW <1>	AGC DatBW <0>
0x13	Reserved								
0x14	VGASQ	VGA squelch time (VGA/AGC section)							
		AGC Test<0>	AGC Test<1>	AGC Test<2>	DisSvo SQ	VGASQ <3>	VGASQ <2>	VGASQ <1>	VGASQ <0>
0x15	Reserved								
0x16	Reserved								
0x17	PFBW	Prefilter data cutoff frequency (Prefilter section)							
						DatBW <3>	DatBW <2>	DatBW <1>	DatBW <0>
0x18	Reserved								
0x18	PFCntl	Prefilter control register (Prefilter section)							
				DisPFPDn	PFRF <4>	PFRF <3>	PFRF <2>	PFRF <1>	PFRF <0>
0x1A	PFTest	Prefilter test register (Prefilter section)							
		<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
0x1B	Reserved								
0x1C	d_kGain	Target amplitude - scaling factor for equalizer error, d_k. (decision section)							
		d_kGain <7>	d_kGain <6>	d_kGain <5>	d_kGain <4>	d_kGain <3>	d_kGain <2>	d_kGain <1>	d_kGain <0>
0x1D	SlicerThresh	Slicer threshold - (decision section)							
		Slicer Thresh <7>	Slicer Thresh <6>	Slicer Thresh <5>	Slicer Thresh <4>	Slicer Thresh <3>	Slicer Thresh <2>	Slicer Thresh <1>	Slicer Thresh <0>
0x1E	AGCTrack	AGC tracking gain, μ_{gt}, (decision section)							
		Dis Dec PDn	DecTst <10>	DecTst <9>	DecTst <8>	AGC Trk<3>	AGC Trk<2>	AGC Trk<1>	AGC Trk<0>
0x1F	Reserved								
0x20	SynthCntl	Synthesizer control register (timing recovery section)							
						forc_ vctl	mon_ vctl	forc_ clk	pd_clr
0x21	SynthM	Synthesizer M feedback counter (timing recovery section)							
		i_pmp <1>	i_pmp <0>	M<5>	M<4>	M<3>	M<2>	M<1>	M<0>
0x22	SynthN	Synthesizer N reference counter (timing recovery section)							
		lpf<1>	lpf<0>	N<5>	N<4>	N<3>	N<2>	N<1>	N<0>
0x23	SynthCF	Synthesizer control - VCO center frequency and loop gain (timing recovery section)							
			svco_ld_ en<2>	svco_ld_ en<1>	svco_ld_ en<0>	svco_ ctl<3>	svco_ ctl<2>	svco_ ctl<1>	svco_ ctl<0>

Addr	Name	Description							
0x24	TRCalib	Data and synthesizer VCO center-frequency offset calibration. (timing recovery section)							
		zero_ cmp	start_cf_ calib	cf_calibrat ing	vco_over _flow	vco_offset <3>	vco_offset <2>	vco_offset <1>	vco_offset <0>
0x25	TRCntl1	Read mode acquisition time-out and zero-phase start threshold (timing recovery section)							
		dvco_ up	dvco_ dn	pdinsel_ nrd	Ichg<1>	Ichg<0>	ZP<2>	ZP<1>	ZP<0>
0x26	TRCntl2	Timing recovery control, charge pump and VCO current adjustment (timing recovery section)							
		Ichg Adj	dvco_ld_ en<2>	dvco_ld_ en<1>	dvco_ld_ en<0>	dvco_ ctl<3>	dvco_ ctl<2>	dvco_ ctl<1>	dvco_ ctl<0>
0x27	TRTest1	Timing recovery test control1 (timing recovery section)							
		VCOin Test	EnTestClk	RefDiv4	TRAcq On	VCOout Test	TRTest <2>	TRTest <1>	TRTest <0>
0x28	TRTest2	Timing recovery test control2 (timing recovery section)							
						Ck2Sel	Ck2Drv	Ck2En	Ck1En
0x29 - 0x2F	Reserved								
0x30	ADCntl	Analog diagnostic control register (analog diagnostic section)							
			ErrLevon		Single Trigger	Auto Trigger	Auto ADC	ErrLev toADC	ADC Done
0x3F	ADData	Analog diagnostic data register (analog diagnostic section)							
		ADData <7>	ADData <6>	ADData <5>	ADData <4>	ADData <3>	ADData <2>	ADData <1>	ADData <0>
0x32	ADTest	Analog diagnostic test control register (analog diagnostic section)							
		ErrLev Reset	ErrLev BWLo	HSO on	HSIO on	HSIO in	DCIOCtl <2>	DCIOCtl <1>	DCIOCtl <0>
0x33 - 0x3E	Reserved								
0x3F	ChipID	Chip ID Number							
		0	0	0	0	0	0	0	0
0x41	FBFGain	Feedback filter update gain, μ_{ram} and μ_{fb}							
				LGain <2>	LGain <1>	LGain <0>	RGain <2>	RGain <1>	RGain <0>
0x42	FBFCntl	Feedback filter control register							
				FBF Adapt	Test Mode	TstAddr <3>	TstAddr <2>	TstAddr <1>	TstAddr <0>
0x43 - 0x4F	Reserved								
0x50	RFB0	RAM feedback filter cell0 content - RFB0<7:0>							
0x51	RFB1	RAM feedback filter cell1 content - RFB1<7:0>							
0x52	RFB2	RAM feedback filter cell2 content - RFB2<7:0>							

Addr	Name	Description							
0x53	RFB3	RAM feedback filter cell3 content - RFB3<7:0>							
0x54	RFB4	RAM feedback filter cell4 content - RFB4<7:0>							
0x55	RFB5	RAM feedback filter cell5 content - RFB5<7:0>							
0x56	RFB6	RAM feedback filter cell6 content - RFB6<7:0>							
0x57	RFB7	RAM feedback filter cell7 content - RFB7<7:0>							
0x58	LFB0	Linear feedback filter tap0 weight - LFB0<7:0>							
0x59	LFB1	Linear feedback filter tap1 weight - LFB1<7:0>							
0x5A	LFB2	Linear feedback filter tap2 weight - LFB2<7:0>							
0x5B	LFB3	Linear feedback filter tap3 weight - LFB3<7:0>							
0x5C	LFB4	Linear feedback filter tap4 weight - LFB4<7:0>							
0x5D	FFW0	Forward filter tap0 weight - FFW0<7:0>							
0x5E	FFW1	Forward filter tap1 weight - FFW1<7:0>							
0x5F	FFW2	Forward filter tap2 weight - FFW2<7:0>							
0x60	FFW3	Forward filter tap3 weight - FFW3<7:0>							
0x61	FFW4	Forward filter tap4 weight - FFW4<7:0>							
0x62	DCCalVal	Delay cell calibration value							
			DCCalVal <6>	DCCalVal <5>	DCCalVal <4>	DCCalVal <3>	DCCalVal <2>	DCCalVal <1>	DCCalVal <0>
0x63	AdaptFFTap	Forward filter tap fixed (freeze)							
			Tuforc	Agc Byp	Adapt FFTap <4>	Adapt FFTap <3>	Adapt FFTap <2>	Adapt FFTap <1>	Adapt FFTap <0>
0x64	DisFFTap	Forward filter tap disable							
			Ekforc	Ftforc	DisFFTap <4>	DisFFTap <3>	DisFFTap <2>	DisFFTap <1>	DisFFTap <0>
0x65	FFGain	Forward filter tap weight update gain, μ_{ff}							
		FFGain <2>	FFGain <1>	FFGain <0>	<4>	<3>	<2>	<1>	<0>
0x66	DCCntl	Delay cell control register							
			Calib Error	Calib Done	Wait2	GainCntl Off	SelTest Phase	StartDly Calib	Dis FFPDn
0x67	DCTest	Forward filter test control register							
		FFTH<3>	FFTH<2>	FFTH<1>	FFTH<0>	FFTL<3>	FFTL<2>	FFTL<1>	FFTL<0>
0x68 - 0x7F	Reserved								

Since the serial interface will only receive six bits of register address from the microprocessor, only 64 register locations can be directly addressed at one time. As a result, the registers have been divided into two banks of 64-register space to get around this limitation. Bank 0 is mapped into addressing space from 0x00 to 0x3F, and bank 1 is mapped into addressing space from 0x41 to 0x7F. The seven-bit address is formed by using the RegBank bit in register 0x00 as the MSB and concatenating the six-bit serial interface address as the LSBs. Since the RegBank bit needs to be accessed regardless of its value, there is no register 0x40.

In order to minimize bank switching, all of the control registers and most of the operating parameters are placed in bank 0 while bank 1 contains only the equalization parameters. This way, bank 1 is accessed only during power-on reset and zone change. When the equalizer parameters are loaded, the RegBank bit should be reset so that subsequent serial interface operations address only bank 0.

SerIntf Register (0x00)

Bit	Name	POR State	Description
7	RegBank	0	Register bank selection - This bit is added as the MSB to the 6-bit serial interface address. This bit must be set when addressing registers 0x41 to 0x7F. It must be reset when addressing registers 0x00 to 0x3F. This bit does not affect the addressing of register 0x00, i.e., register 0x40 is the same as register 0x00
6	ChipReset	0	Chip reset - Setting this bit resets the DFE9952R to power-on state. It has the identical effect as asserting the $\overline{\text{POR}}$ pin. The only exception is that the serial interface and this register are not reset by this bit. This bit is latched until it is reset.

Status Register (0x01)

Bit	Name	POR State	Description
7	Alarm	R/O	Alarm - This bit is set whenever an error is detected in the DFE9952R. The exact error that caused the alarm can be found by reading bits 4 - 0 of this register. This bit is automatically reset when the error source has been cleared.
<6:5>	OpMode<1:0>	R/O	The operational mode of the DFE9952R is encoded in these two bits as follows: 00 - standby or sleep mode, 01 - read mode, 10 - write mode, 11 - servo mode. (Check bit 0 of Control1 register (0x02) for sleep mode.)
4	ModeError	0	Operating mode error - This bit is set if any two of SVOGT, $\overline{\text{WRTGT}}$ or RDGT are active. This bit is latched. When the error condition is removed, you must reset this bit. ModeError does not prevent DFE9952R from operating. The actual operating mode of the DFE9952R is determined based on SVOGT having the highest priority and $\overline{\text{WRTGT}}$ having the lowest.
2	SMNotFound	R/O	Sync Mark not found error - This bit is set if the Sync Mark is not found within the Sync Mark search window. This bit is automatically cleared at the beginning of a Read operation.

Control1 Register (0x02)

Bit	Name	POR State	Description
7	NRZwidth8	0	NRZ width selection - Setting this bit selects the NRZ interface to be eight bits wide. Otherwise, the NRZ interface is four bits wide.
6	EnRandom	0	Enable randomizer - Setting this bit enables the randomizer in read and write modes. When Bypass ENDEC is set, the Randomizer is always off.
5	BypassSM	0	Bypass Sync Mark detection - Setting this bit disables the Sync Mark detection circuit and allows the data to be read even if the Sync Mark is not found. Usually, this bit is set only when Bypassing the ENDEC.
4	EnSupvsry	0	Enable supervisory mode - Setting this bit enables the supervised training mode for the DFE9952R.
3	BypassENDEC	1	When set, the write data is not encoded and the read data is not decoded.
2	DisRWCLK	0	Disable RWCLK during non-read and non-write modes - Setting this bit disables RWCLK during non-read and non-write modes. Resetting this bit allows the RWCLK to toggle at all times.
1	BypassPrecomp	0	Bypass precomp - Setting this bit disables the precomp control logic so that the write data transitions are not precomped.
0	BypassPrecoder	0	Bypass precoder - Setting this bit bypasses the precoder so that the output of the serializer becomes the write current to the pre-amplifier.

Control2 Register (0x03)

Bit	Name	POR State	Description
7	EnSleep	0	Enable sleep mode - Setting this bit will place the DFE9952R in sleep mode, regardless of the power management override bits. Resetting this bit will place the DFE9952R in active mode. Transition from sleep to active mode requires considerable wakeup time.
6	DisEndPdn	0	Disable powering down ENDEC section - Setting this bit will override the power management of the ENDEC section so that it is never powered down unless in sleep mode. Resetting this bit will allow the ENDEC section to be powered down based on the power management scheme of the DFE9952R.
5	EnRdTest	0	Enable read path testing - Setting this bit will allow the NRZI read data to be multiplexed from the external read data pin. This feature is provided for testing purposes only. In normal operation, this bit must be reset to pass the NRZI read data from the decision section to the read data path.

SyncTol Register (0x04)

Bit	Name	POR State	Description
<6:4>	SMTol<2:0>	N/A	Sync Mark detection error tolerance. Number of bits in error allowed for detection.
<3:0>	SMTO<3:0>	N/A	Sync Mark detection time-out count

DGSeedLSB Register (0x05)

Bit	Name	POR State	Description
<7:0>	DGSeedLSB<7:0>	N/A	Data generator seed value (lower 8 LSBs)

DGSeedMSB Register (0x06)

Bit	Name	POR State	Description
<3:0>	DGSeedMSB<11:8>	N/A	Data generator seed value (upper 4 MSBs). MSB (bit 11) must be reset.

RefClkDiv Register (0x07)

Bit	Name	POR State	Description
6	DC50K	0	Select forward filter delay-cell calibration clock - Setting this bit will select the 50 KHz clock. Resetting this bit will select the 100 KHz clock.
<5:4>	RefDiv<1:0>	N/A	Divider to generate 10 MHz ADC clock - These two bits will divide the SFREF clock frequency by 2, 3, or 4 to generate a 10 MHz internal ADC clock. The divider must be selected to produce an ADC clock that is as close to 10 MHz as possible but must not exceed 10 MHz. Since the SFREF clock frequency has a range of 20 - 40 MHz, the resulting ADC clock will have a frequency of 6.66 - 10 MHz.
<3:0>	ClkDiv<3:0>	N/A	Divider to generate 1 MHz internal clock - The ADC clock is divided by (ClkDiv + 1) to generate the 1 MHz internal clock. The divider must be selected to produce an internal clock that is as close to 1 MHz as possible but must not exceed 1 MHz. Since the ADC clock frequency has a range of 6.66 - 10 MHz, the resulting internal clock will have a frequency of 0.875 - 1 MHz. It is used to digitize the filter coefficients.

WriteDAC Register (0x0B)

Bit	Name	POR State	Description
7	WriteDACOff	N/A	Write current DAC power control - Setting this bit will override the power management scheme and power down the write current DAC in all operating modes. This is useful if the preamp contains built-in write current DAC. Resetting this bit will allow the write current DAC to be powered on and off based on the power management scheme.
<5:0>	Iwrite<5:0>	N/A	Programmable write current DAC value - 0.5 - 2.5 mA ±5%.

MRDAC Register (0x0C)

Bit	Name	POR State	Description
7	MRDACOff	N/A	MR bias DAC power control - Setting this bit will override the power management scheme and power down the MR bias DAC in all operating modes. This is useful if the preamp contains built-in MR bias DAC. Resetting this bit will allow the MR bias DAC to be powered on and off based on the power management scheme.
<5:0>	IMR<5:0>	N/A	Programmable MR bias current DAC value -0.1 to 1.6 mA ±5%.

Precomp Register (0x0D)

Bit	Name	POR State	Description
7	DisWDPdn	0	Disable powering down write data path section - Setting this bit will override the power management of the write data path section so that it is never powered down unless in sleep mode. Resetting this bit will allow the write data path section to be powered down based on the power management scheme of the DFE9952R.
3	PrecompTest	0	Enable precomp test
<2:0>	Precomp<2:0>	N/A	Programmable precompensation control - These three bits selects the amount of delay for precompensation. Precompensation can be disabled by setting the BypassPrecomp bit in the Control1 register (0x02).

AGCDataRef Register (0x10)

Bit	Name	POR State	Description
<6:0>	AGCDataRef<6:0>	N/A	Sets gain regulation in data read mode. The Prefilter output is 4 times the programmed value, differential peak to peak. Data amplitude ranges from 0 to 1.6Vppd. Nominal setting is 1.0Vppd (register setting 0x50).

AGCDataBW Register (0x12)

Bit	Name	POR State	Description
7	DisVGAPdn	0	Disable powering down VGA/AGC section - Setting this bit will override the power management of the VGA/AGC section so that it is never powered down unless in sleep mode. Resetting this bit will allow the VGA/AGC section to be powered down based on the power management scheme of the DFE9952R.
<5:0>	AGCDataBW<5:0>	N/A	AGC data mode programmable charge pump current. Full-scale = 100 µA. Recommended 1 µA/MHz of preamble frequency.

VGASQ Register (0x14)

Bit	Name	POR State	Description
<7:5>	AGCTest<0:2>	0	Not used. VGA test selects. Set to 0.
4	DisSvoSQ	0	Set to 1.
<3:0>	VGASQ<3:0>	N/A	AGC squelch time. Setting is from .2 to 3.2 µsec.

PFBW Register (0x17)

Bit	Name	POR State	Description
<7:4>		N/A	Not used
<3:0>	DatBW<3:0>	N/A	Prefilter data mode cutoff frequency

PFCntl Register (0x18)

Bit	Name	POR State	Description
5	DisPFPdn	0	Disable powering down Prefilter section - Setting this bit will override the power management of the Prefilter section so that it is never powered down unless in sleep mode. Resetting this bit will allow the Prefilter section to be powered down based on the power management scheme of the DFE9952R.
<4:0>	PFRF<4:0>	N/A	Prefilter reference frequency control.

PFTest Register (0x1A)

Bit	Name	POR State	Description
<7:0>	PFTest<7:0>	0	Prefilter test control. Set to 0. Prefilter test control: 0000000 no output 0000001 VGA Output on ATSTIOX ATSTIOY 0000010 FSREF Output on ATSTIOX ATSTIOY 0000100 Prefilter Normal output for data output on ATSTOX ATSTOY 0001000 Prefilter Normal output for servo output on ATSTOX ATSTOY 0010000 Prefilter differentiated for servo output on ATSTOX ATSTOY 0100000 Reference frequency tuning off, input from ADCX ADCY 1000000 Reference frequency tuning on, output to ADCX ADCY

DkGain Register (0x1C)

Bit	Name	POR State	Description
<7:0>	dkGain<7:0>	N/A	Target amplitude - scaling factor for equalizer error. IMPORTANT: The factory will supply the value to be loaded here with the sample ICs.

SlicerThresh Register (0x1D)

Bit	Name	POR State	Description
<7:0>	SlicerThresh<7:0>	N/A	Slicer threshold. Nominal setting is 0x7F

AGCTrack Register (0x1E)

Bit	Name	POR State	Description
7	DisDecPdn	0	Disable powering down decision section - Setting this bit will override the power management of the decision section so that it is never powered down unless in sleep mode. Resetting this will allow the decision section to be powered down based on the power management scheme of the DFE9952R.
<6:4>	DecTst<10:8>	0	Test control bits. Set to 0.
<3:0>	AGCTrack<3:0>	N/A	AGC Data read tracking current multiplier. These 4 bits set the multiplier of the error current $\varepsilon_k/2k\Omega$ in decision directed data read mode.

SynthCntl Register (0x20)

Bit	Name	POR State	Description
3	forc_vctl	0	Force control voltage - When set, this bit causes the differential voltage on the DC test bus to be imposed on the synthesizer's compensator. This voltage controls the VCO frequency. While forc_vctl is asserted, pd_clr should also be asserted. Nominal level is VCC/2.
2	mon_vctl	0	Read control voltage - When set, this bit places the buffered differential VCO control voltage on the DC test bus. This allows the VCO control voltage to be monitored off-chip.
1	forc_clk	0	Force clock - When set, this bit disconnects the VCO from the input of the prescaler and injects the TST_CK1 signal.
0	pd_clr	0	Phase detector clear - When set, this bit disables the phase detector and allows the chip's TST_CK1 signals to force pump-up and pump-down signals.

SynthM Register (0x21)

Bit	Name	POR State	Description
<7:6>	i_pmp<1:0>	N/A	Synthesizer charge pump current control - Charge pump current is varied as follows: <00> 16.67 µA <01> 22.22µA <10> 27.78µA <11> 33.33µA
<5:0>	SynthM<5:0>	N/A	Synthesizer feedback counter (M) value - The VCO frequency is first divided by 8 in a prescaler, and then divided by the value M+1.

SynthN Register (0x22)

Bit	Name	POR State	Description
<7:6>	lpf<1:0>	N/A	Low pass filter control - These bits control the zero and pole frequency of the synthesizer's compensator. The nominal value of the integrator capacitor is 205pF. The nominal zero/pole frequencies are as follows: Zero ------- Pole <00> 11.9 kHz / 572.9kHz <01> 13.7 kHz / 661.0 kHz <10> 16.2 kHz / 781.2 kHz <11> 19.8 kHz / 954.8 kHz
<5.0>	SynthN<5:0>	N/A	Synthesizer reference counter (N) value - The reference frequency supplied at SFREF is divided by the value N+1.

SynthCF Register (0x23)

Bit	Name	POR State	Description
<6:4>	svco_ld_en<2:0>	N/A	Synthesizer VCO load control
<3:0>	svco_ctl<3:0>	N/A	Synthesizer VCO center frequency control

TRCalib Register (0x24)

Bit	Name	POR State	Description
7	zero_cmp	N/A	Force Synthesizer VCO to center frequency
6	start_cf_calib	0	Start VCO center-frequency calibration
5	cf_calibrating	R/O	VCO center-frequency calibration in progress
4	vco_overflow	R/O	VCO center-frequency calibration overflow
<3:0>	vco_offset<3:0>	N/A	VCO center-frequency offset. 0x00 is lowest offset.

TRCntl1 Register (0x25)

Bit	Name	POR State	Description
7	dvco_up	0	Data VCO charge up
6	dvco_dn	0	Data VCO charge down
5	pdinsel_nrd	0	
<4:3>	Ichg<1:0>	N/A	Charge pump current. Sets current in tracking mode in read only. A set of 11 is track current equal to acquire, 00 is 25%.
<2:0>	ZP<2:0>	N/A	Zero-phase start threshold. Recommended value is 110 for 200 Mbits/sec and 000 for 64 Mbits/sec.

TRCntl2 Register (0x26)

Bit	Name	POR State	Description
7	IchgAdj	0	Increases the Read mode Timing Recovery charge pump current by 50% when set.
<6:4>	dvco_ld_en<2:0>	N/A	Data VCO load control
<3:0>	dvco_ctl<3:0>	N/A	Data VCO center frequency

TRTest1 Register (0x27)

Bit	Name	POR State	Description
7	VCOinTest	0	When set, the VCO Control Voltage is driven directly by the ADCX and ADCY pins. Requires bit VCOout Test to be set as well.
6	EnTestClk	0	All internal clocks will be driven by TST_CK1 and TST_CK2. These will have TST_CK1 leading TST_CK2 by 90 degrees. Both pairs are CML differential inputs.
5	RefDiv4	0	Meant for characterization use only.
4	TRAcqOn	0	Hold timing recovery in acquisition for testing
3	VCOoutTest	0	If set and VCOinTest is set, the ADCX and ADCY pins drive the VCO Control voltage. If set and VCOinTest is reset, allows monitoring of the VCO Control Voltage for testing.
<2:0>	TRTest<2:0>	0	Bits 2 & 1 not used. Bit 0 when set forces VCO Control voltage circuit to follow the ADCX pin DC level as the Common Mode voltage of the Loop Filter.

TRTest2 Register (0x28)

Bit	Name	POR State	Description
3	Ck2Sel	0	When set, the Timing recovery VCO is output on the TST_CK2 pins @ CML levels. Reset selects the Frequency Synthesizer VCO.
2	Ck2Drv	0	Set selects the TST_CK2 pins to be output drivers
1	Ck2En	0	Set enables the TST_CK2 pins for both input and output
0	Ck1En	0	Set selects the TST_CK1 pins to be input receivers

ADCntl Register (0x30)

Bit	Name	POR State	Description
6	ErrLevOn	0	Power on ErrLev circuit -
4	SingleTrigger	0	Manual control of a single digitization - do an A to D conversion. The ADC output can be read from the ADData register (0x3F). When AutoADC is set, the value of this bit is ignored.
3	AutoTrigger	0	Manual control of digitization of filter tap weights - When AutoADC is reset, setting this bit will cause all of the filter tap weights to be digitized and stored in their respective registers. When AutoADC is set, the value of this bit is ignored.
2	AutoADC	N/A	Automatic digitization of filter tap weights - Setting this bit will cause all of the filter tap weights to be digitized and stored in their respective registers at the end of each read operation. Resetting this bit will allow manual control of ADC by SingleTrigger and AutoTrigger.
1	ErrLevtoADC	N/A	ADC input selection - When the ADC is in single-trigger mode, this bit selects the ErrLev as the input to the ADC when it is set, otherwise, the DC test bus is selected as the input to the ADC.
0	ADCDone	R/O	Digitization completed - This bit is reset at the start of a digitization cycle and is set when the cycle has completed.

ADData Register (0x3F)

Bit	Name	POR State	Description
<7:0>	ADData<7:0>	R/O	ADC output data register - This register holds the output of the ADC when a conversion is done in the single-trigger mode.

ADTest Register (0x32)

Bit	Name	POR State	Description
7	ErrLevReset	0	Reset ErrLev circuit.
6	ErrLevBWLo	0	ErrLev bandwidth select - Setting this bit selects low bandwidth. Resetting this bit selects high bandwidth.
5	HSOon	0	Enable high-speed output test bus - Setting this bit enables the high-speed output test bus buffer. Resetting this bit disables the buffer.
4	HSIOon	0	Enable high-speed input/output test bus driver - Setting this bit enables the buffer circuit. Resetting this bit powers off the buffer circuit.
3	HSIOin	0	Select high-speed input/output test bus direction - Resetting this bit allows the contents of the test bus to be driven out to the pad. Setting this bit allows the external signal to be driven onto the test bus.
<2:0>	DCIOctl<2:0>	02	DC Bus control bits. These bits control the ADCX/ADCY bus per the following:

2	1	0	
0	0	0	ADCX/ADCY off
1	0	0	ADCX/ADCY read test voltages from IC
0	1	1	ADCX/ADCY drive IC with external voltages

ChipID Register (0x3F)

Bit	Name	POR State	Description
<7:0>	none	R/O	Read only value of 0 which identifies the DFE9952R rev. 0.

FBFGain Register (0x41)

Bit	Name	POR State	Description
<5:3>	LGain<2:0>	N/A	Linear feedback filter tap weight update multiplier, μ_{fb}
<2:0>	RGain<2:0>	N/A	RAM feedback filter update multiplier, μ_{ram}

FBFCntl Register (0x42)

Bit	Name	POR State	Description
5	FBFAdapt	0	When set, the Feedback Filter Adaptive operation is enabled. All portions (RAM and linear) are Adaptive.
4	TestMode	0	Enables the TstAddr bits.
<3:0>	none	0	Test Address bits. Set to 0.

RFBn Register (0x50 - 0x57)

Bit	Name	POR State	Description
<7:0>	RFBn<7:0>	N/A	RAM feedback filter cell n value, n = 0 to 7. RFB0 register corresponds to address 0x50, and RFB7 corresponds to address 0x57. RFB0 is the cell for the most recent decisions being -1, -1, -1. RFB7 is for most recent decisions being 1,1,1.

LFBn Register (0x58 - 0x5C)

Bit	Name	POR State	Description
<7:0>	LFBn<7:0>	N/A	Linear feedback filter tap n weight, n = 0 to 4. LFB0 register corresponds to address 0x58, and LFB4 corresponds to address 0x5C. LFB0 is the cell closest to the Decision block, i.e., the most recent decision.

FFWn Register (0x5D - 0x61)

Bit	Name	POR State	Description
<7:0>	FFWn<7:0>	N/A	Forward filter tap n weight, n = 0 to 4. FFW0 register corresponds to address 0x5D, and FFW4 corresponds to address 0x61. FFW0 is the closest to the input.

These five registers hold the digitized tap weights of the forward filter. When tap n is fixed by resetting bit n of the AdaptFFTap register (0x63), the value programmed in the corresponding FFWn register is converted by tap n DAC into the fixed tap weight. When the weight of tap n is digitized with the 8-bit ADC, the result is stored in the corresponding FFWn register.

DCCalVal Register (0x62)

Bit	Name	POR State	Description
<6:0>	DCCalVal<6:0>	N/A	Delay cell calibration value

AdaptFFTap Register (0x63)

Bit	Name	POR State	Description
6	Tuforc	0	Connects a path through one of the low-speed buses (operated in INPUT mode) to the master tuning voltage at the delay line (overriding the Cal-DAC output).
5	AgcByp	0	Enables AgcByp mode, which connects external input pins of DFE directly to forward filter, bypassing AGC and Prefilter.
<4:0>	AdaptFFTap<4:0>	0	Adapt forward filter tap weight - Setting any bit will enable adaptation for the corresponding forward filter tap, and vice versa. Bits<4:0> correspond to tap <4:0>, respectively. One bit should be reset during Normal Operation.

This register allows independent control of all five tap weights of the forward filter. When tap n is fixed, the value programmed in the corresponding FFWn register is converted by tap n DAC into the fixed tap weight. When tap n is allowed to adapt, the tap weight is continuously updated during read operations based on the equalizer error, ε_k.

DisFFTap Register (0x64)

Bit	Name	POR State	Description
6	Ekforc	0	Forces the error signal, "ε_k", for the whole DFE, from an external source via the high-speed analog I/O bus.
5	Ftforc	0	Forces output signal of forward-filter, from an external source via high-speed analog I/O bus.
<4:0>	DisFFTap<4:0>	0	Disable forward filter tap weight - Setting any bit will disconnect the tap from the Forward filter output, and vice versa. Bits <4:0> correspond to tap <4:0>, respectively. Setting any bit is equivalent to loading the corresponding tap-weight register with zero and resetting the corresponding AdaptFFTap bit.

FFGain Register (0x65)

Bit	Name	POR State	Description
<7:5>	FFGain<2:0>	N/A	Forward filter tap weight update multiplier, μ_{ff}

DCCntl Register (0x66)

Bit	Name	POR State	Description
6	CalibError	R/O	Delay cell calibration error - This bit is set if the delay cell fails to re-calibrate itself. This bit is reset at the beginning of the delay cell re-calibration operation.
5	CalibDone	R/O	
4	Wait2	0	
3	GainCntlOff	0	Calibration gain control off - Setting this bit will disable gain control in the calibration circuit.
2	SelTestPhase	0	
1	StartDlyCalib	0	Start delay cell calibration - Setting this bit starts the calibration of the delay cell. This bit must be reset before it can be set to start the next calibration cycle.
0	DisFFPdn	0	Disable powering down forward filter section - Setting this bit will override the power management of the forward filter section so that it is never powered down unless in sleep mode. Resetting this bit will allow the forward filter section to be powered down based on the power management scheme of the DFE9952R.

FFTest Register (0x67)

	Name	POR State	Description
<7:4>	FFTH<3:0>	0	High-speed buffer control 0000 - off 0001 - Forward filter tap weight #0 0010 - Forward filter tap weight #1 0011 - Forward filter tap weight #2 0100 - Forward filter tap weight #3 0101 - Forward filter tap weight #4 0110 - Forward filter output 0111 - error signal input at Forward filter
<3:0>	FFTL<3:0>	0	Low-speed buffer control 0000 - off 0001 - first derived tuning voltage 0010 - second derived tuning voltage 0011 - third derived tuning voltage 0100 - Cal DAC output 0101 - delay-cell amplitude-control voltage 0110 - balance voltage (Vcc / 2)

PARAMETRIC SPECIFICATIONS

Unless otherwise specified, the following specifications are valid over the temperature range of 0 °C to 70 °C and for Vcc between 4.5 V and 5.5 V. Currents flowing into a pin are positive. Maximum values are values with the largest absolute value.

Nominal Operating Conditions

Parameter	Rating	Units
Temperature (ambient)	0 to 70	°C
Supply Voltage (V_{CC})	4.5 to 5.5	V_{DC}

Power Supply Current and Power Dissipation

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
I_{CC}		Outputs and all test points open @200 Mbit/s T_{amb} = 27 °C V_{CC} = 5 Vdc		180 (target)		mA

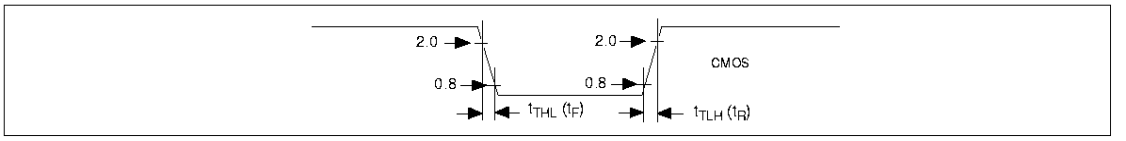
DIGITAL INPUTS AND OUTPUTS

TTL Compatible Inputs

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
I_{IL}	Input Low Current	V_{IL} = 0.4 V			-400	µA
I_{IH}	Input High Current	V_{IH} = 2.4 V			50	µA
	Input Leakage Current		-1		+1	µA
C_{IN}	Input Capacitance				2.7	pF
	Internal Pull-up Resistor		10		30	kΩ

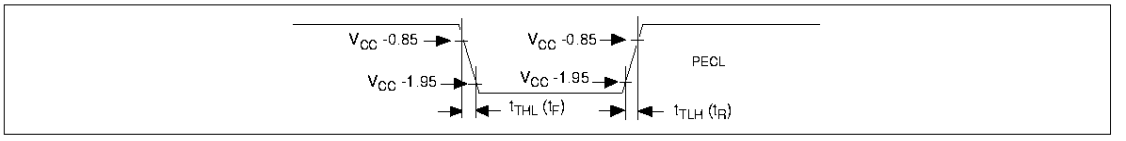
CMOS Compatible Inputs and Outputs

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{IL}	Input Low Voltage		-0.3		1.5	V
V_{IH}	Input High Voltage		3.5		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	V_{CC} = 5.0 V, T_{amb} = 25 °C, I_{OL} = 5.0 mA			0.5	V
V_{OH}	Output High Voltage	V_{CC} = 5.0 V, T_{amb} = 25 °C, I_{OH} = -5.0 mA	4.5			V
t_R	Rise Time	V_{CC} = 4.5V, T_{amb} = 70 °C, C_L = 15 pF			3.0	ns
t_F	Fall Time	V_{CC} = 4.5V, T_{amb} = 70 °C, C_L = 15 pF			4.0	ns
	Output Capacitive Load			15		pF



PECL Output Levels

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{OH}	Output High Voltage		V_{CC}- 1.0	V_{CC} - 0.85	V_{CC} - 0.7	V
V_{OL}	Output Low Voltage		V_{CC} - 2.2	V_{CC} - 1.95	V_{CC}- 1.7	V
t_R, t_F	Rise/fall time	10% - 90% swing			1.0	ns
	Standard single load capacitance			14.0	30.0	pF



CML (Test Point) Input and Output Levels

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{OH}	Output High Voltage			V_{CC}		V
V_{OL}	Output Low Voltage			V_{CC} - .15		V
V_{IH}	Input High Voltage			V_{CC}		V
V_{IL}	Input Low Voltage			V_{CC} - .15		V
t_R, t_F	Rise/fall time	10% - 90% swing			1.0	ns

Variable Gain Amplifier (VGA)

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
	Differential Input Range (peak-to-peak amplitude)	Input signal frequency from 10 to 50 MHz, Minimum Boost	35		600	mVppd
V_{OO}	Offset Referred to Input		-10		10	mV
	Squelch Duration	VGASQ<3:0> = 0x00		0.2		µs
		VGASQ<3:0> = 0xFF		3.2		µs
	Output Swing	Differential, at 0.1% THD		1.0		Vppd
A_V	Gain Range		2		35	V/V
	Gain Control Sensitivity	per volt of AGC control voltage, for reference only. Not Tested.		15		dB/V
Z_{IN}	Differential Input Impedance	Normal Mode	3.0	4.0	5.0	kΩ
		Squelched Mode	50	150	200	Ω
CMRR	Common Mode Rejection	Gain = max, f = 10 MHz	40			dB
PSRR	Power Supply Rejection	Gain = max, f = 10 MHz	45			dB
BW	Bandwidth	Gain = 35 V/V @ -3 dB point		TBD		MHz
e_{in}	Input-referred Noise Voltage	Gain = max, Inputs shorted			10	nV/ $\sqrt{Hz}$

Automatic Gain Control (AGC)

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
	Input Signal Range			1.0		Vppd
I_C	Peak Detector charge Current	AGCDatBW<5:0> = 0x00		1		µA
		AGCDatBW<5:0> = 0x3F		100		µA
I_D	Peak Detector discharge Current			10*Ic		µA
	V_{AGC} Capacitor Value			20		pF
	Gain Decay Time	65% drop in level of 4T signal, symbol rate = 225 MHz, to 85% of correct signal level		TBD		ns
	Gain Decay Time	65% drop in level of 4T signal, symbol rate = 225 MHz, 95% of correct signal level		TBD		ns
	Gain Attack Time	Initial gain = 2X correct value, 4T input signal, symbol rate = 225 MHz, settled to 115% of correct signal level.		TBD		ns
	Gain Attack Time	Initial gain = 2X correct value, 4T input signal, symbol rate = 225 MHz, settled to 105% of correct signal level		TBD		ns

Automatic Gain Control (AGC) *Continued*

	Gain Decay Time	50% drop in level of 4T signal, data synchronizer CCF = 35 MHz to 85%		TBD		µs
	Gain Decay Time	50% drop in level of 4T signal, data synchronizer CCF = 35 MHz, V_{AGC} = 330 pF, to 95%		TBD		µs

Prefilter

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
f_c	Cutoff Frequency	Unboosted response @ -3 dB point	30		86.25	MHz
	Cutoff Frequency Step	Unboosted response @ -3 dB point		3.75		MHz
f_cA	Cutoff Frequency Accuracy			±10		%
	Group Delay Variation	From 0.2 f_c to f_c.		±10		%
THD	Total Harmonic Distortion	Vppd=1.0 V, f = 0.5 f_c.		1.0		%
A_V	Filter Gain	Vppd=0.5 V, f = 0.5 f_c.	0.8		1.2	V/V
	Differential Input/Output Range	THD = 0.1%. (measured as a peak-to-peak differential signal)			1.2	Vppd
PSRR	Power Supply Rejection	DC, 10% change at V_{CC}		60		dB
		5 MHz, 10 mVpp at V_{CC}		40		dB
CMRR	Common Mode Rejection	input f = 5 MHz		40		dB
SNR	Output Signal to Noise	f_c = 36 MHz. Not tested in ATE		50		dB
R_{IN}	Filter Differential Input Resistance	Not tested in ATE	5.0			kΩ
C_{IN}	Filter Differential Input Capacitance	Not tested in ATE			5.0	pF
e_{out}	Filter Output Noise	BW = TBD MHz, Rs = 50 Ω f_c = 80.25 MHz Not tested in ATE		3.8		mV RMS
	Filter Output Noise	BW = TBD MHz, Rs = 50 Ω f_c = 80.25 MHz Not tested in ATE		6.9		mV RMS
	Filter Output Sink Current	Not tested in ATE		0.5		mA
	Filter Output Source Current	Not tested in ATE	2.0			mA
	Filter Output Resistance	Single ended. Not tested in ATE		TBD		Ω
SFREF	Reference Frequency		10		38.75	MHz

Forward Filter

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
	Number of Taps			5		taps
	Delay Cell Input Voltage				1.2	Vppd
D	Delay Time	each cell	4.0		14.0	ns
	Tuning Granularity				0.2	ns
	Delay cell calibration time				1300	µs
	Short Range Calibration time	< 5 steps			60	µs

Timing Recovery

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
f_{VCO}	VCO Center Frequency Range	After offset and Calibration	78		225	MHz
$f_{VCO}A$	VCO Center Frequency Accuracy				±10	%
	Input Voltage Range	To internal loop filter nodes			±1	V
	Dynamic Range	-1.0 V < LPFP - LPFN < +1.0 V	±16		±24	%
K_{VCO}	VCO Gain	$\omega_0 = 2\pi / T_{VCO}$	$0.16\omega_0$		$0.24\omega_0$	rad / V· sec
	Phase Detector Range	Non-read mode		$\pm 2\pi$		rad
		Read mode during acquisition		$\pm 2\pi$		rad
K_D	Phase Detector Charge Pump Gain	Non-read mode: $K_D = I_{chg}/2\pi$.	$0.9K_D$		$1.1K_D$	A/rad
		Read mode: $K_D = I_{chg}/\pi$.	$0.9K_D$		$1.1K_D$	A/rad
	1 σ Generated Jitter	Decision directed			TBD	ps
	RWCLK Duty Cycle	Measured at 1.5 V	40		60	%
	K_{VCO} * K_D Accuracy		-28		28	%

Frequency Synthesizer

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
	SFREF Frequency		20		40	MHz
	SFREF Duty Cycle	Measured at 1.5 V	40		60	%
K_{VCO}	WrtClk Frequency		78		225	MHz
	WrtClk Duty Cycle		40		60	%
	WrtClk 1 σ Generated Jitter	PLL locked at 225 MHz. Measured falling edge to falling edge, SFREF TBD, loop filter TBD			TBD	ps RMS
	M Counter Range	Feedback Counter	15		64	
	N Counter Range	Reference Counter	1		64	
t_{ACQ}	Acquisition time	To 1% of final value. F_{VCO} = 225 MHz.			100	µs
	Loop bandwidth	Open loop derived. F_{VCO} = 225 MHz.	50		70	KHz
	Synthesizer VCO Dynamic Range	WrtClk = 200 MHz		±20		%
K_{VCO}	Synthesizer VCO Control Gain			$0.2f_c$	0.26	MHz/V
	Charge Pump Current	Refer to register 0x21				
	KVCO * KD Accuracy		-28		+28	%

Write Current DAC

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
I_W	Output Current Range		0.5		2.5	mA
	Output Current Step Size			31.65		µA
	Output Current Step Size Accuracy		-50		-50	% of LSB
	Output Current Step Size Monotonicity		-50		+50	% of LSB
	Turn On Time	After Assertion of $\overline{WRTGT}$		43		ns
	Turn Off Time	After Deassertion of $\overline{WRTGT}$		7		ns

MR Bias Current DAC

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
I_{MR}	Output Current Range		0.1		1.6	mA
	Output Current Step Size			23.9		µA
	Output Current Step Size Accuracy		-50		+50	% of LSB
	Output Current Step Size Monotonicity		-50		+50	% of LSB
	Turn On Time	After deassertion of $\overline{WRTGT}$		33		ns
	Turn Off Time			7		ns

Write Precompensation Circuit

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
	Precompensation Range		0		30	% bit cell
	Precompensation Resolution			5		% bit cells
	Precompensation Programming Accuracy	of setting		±25		%

TIMING CHARACTERISTICS

Serial Interface

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
t_{CC}	SCLK Period	20 pF load	25			ns
t_{CD}	SCLK Low Time	20 pF load	10			ns
t_{CH}	SCLK High Time	20 pF load	10			ns
t_{DS}	SDATA Setup Time	20 pF load	8			ns
t_{DH}	SDATA Hold Time	20 pF load	3			ns
t_{EC}	$\overline{SDEN}$ Falling Edge to First SCLK Rising Edge	20 pF load	10			ns
t_{CE}	Last SCLK Rising Edge to $\overline{SDEN}$ Rising Edge	20 pF load	15			ns
t_{NO}	Last SCLK Falling Edge to $\overline{SDEN}$ Rising Edge	20 pF load	5			ns
t_{EL}	$\overline{SDEN}$ Low Time	20 pF load	405			ns
t_{EH}	$\overline{SDEN}$ High Time	20 pF load	25			ns

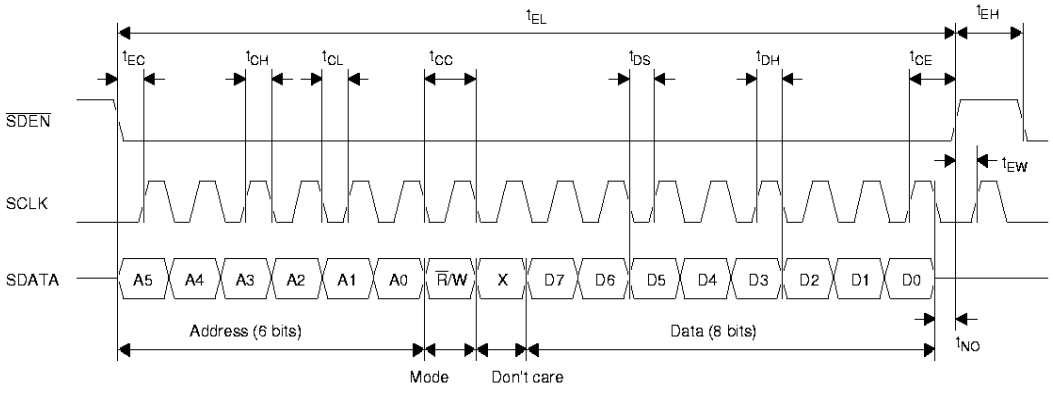
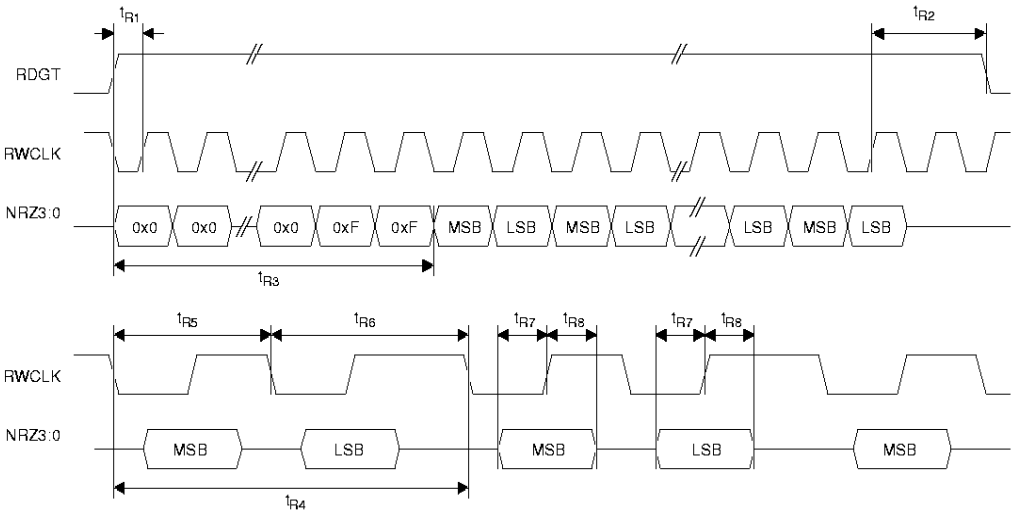


FIGURE 11. Serial Interface Timing Diagram

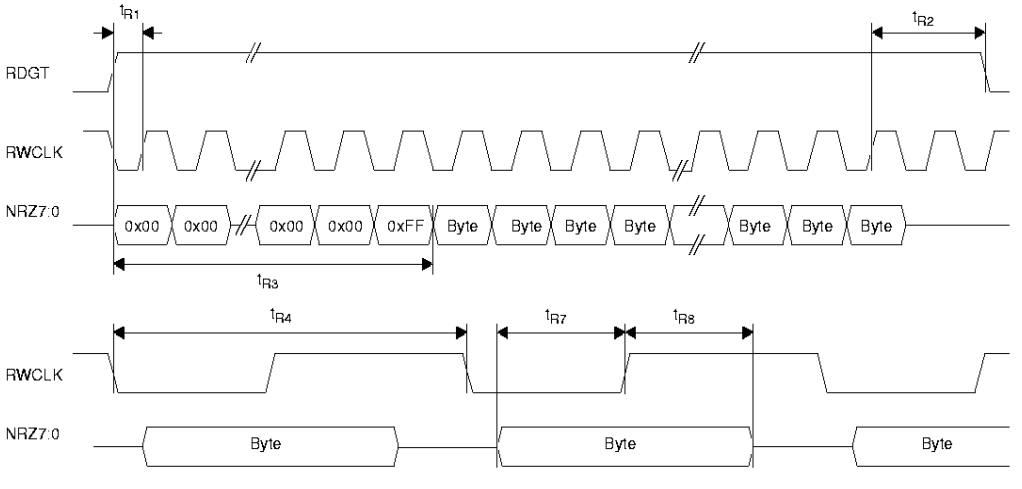
NRZ Data Read Mode

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
t_{R1}	RDGT Assertion to First Rising Edge of RWCLK				$2t_{R4}$	ns
t_{R2}	Last valid data transfer to deassertion of RDGT		t_{R4}			ns
t_{R3}	Sync Mark Search Time Out				144	T
t_{R4}	One Byte Transfer Period	@ 200 Mbit/s, ENDEC enabled		40		ns
		@ 64 Mbit/s, ENDEC enabled		125		ns
		@ 200 Mbit/s, ENDEC bypassed		35.6		ns
		@ 64 Mbit/s, ENDEC bypassed		111.1		ns
t_{R5}	One Nibble Transfer Period	4-bit NRZ, MSB, ENDEC enabled		$4t_{R4/9}$		ns
t_{R6}		4-bit NRZ, LSB, ENDEC enabled		$5t_{R4/9}$		ns
t_{R5}, t_{R6}		4-bit NRZ, MSB & LSB, ENDEC bypassed		4/2		ns
	RWCLK Duty Cycle	4-bit NRZ, MSB		50		%
		4-bit NRZ, LSB, ENDEC enabled		60		%
		4-bit NRZ, LSB, ENDEC bypassed		50		%
		8-bit NRZ, ENDEC enabled		55.5		%
		8-bit NRZ, ENDEC bypassed		50		%
t_R	RWCLK Rise Time	0.8 to 2.0 V, $C_L \leq 15$ pF			5	ns
t_F	RWCLK Fall Time	2.0 to 0.8 V, $C_L \leq 15$ pF			5	ns
t_{R7}	NRZ7:0 Setup Time				5	ns
t_{R8}	NRZ7:0 Hold Time				2	ns



In Training mode the Sync Mark is detected, the Sync Mark place nibbles are output, and MSB and LSB are output but are not readback data.

FIGURE 12. 4-Bit NRZ Data Read Mode Timing Diagram

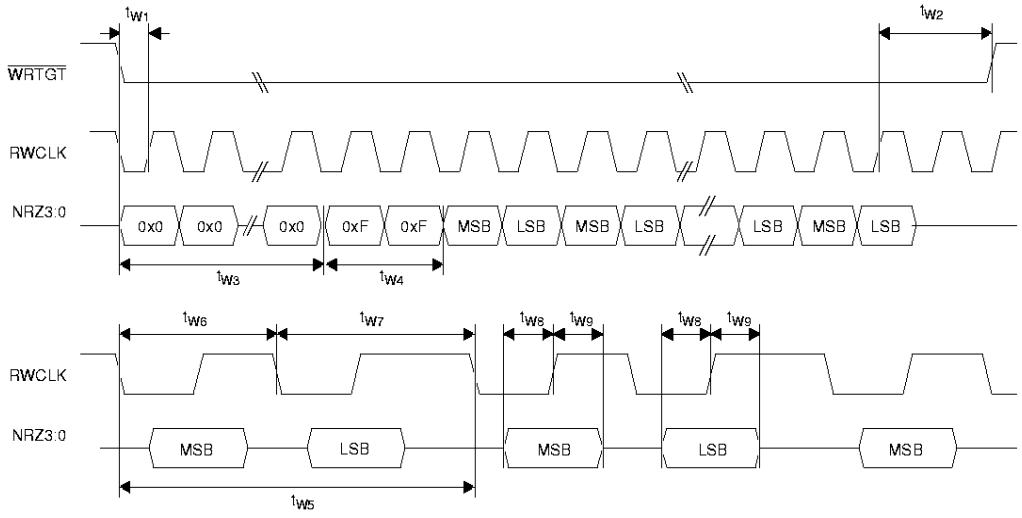


In Training mode the Sync Mark is detected, the Sync Mark place byte is output, and Data "Byte" is output but is not readback data.

FIGURE 13. 8-Bit NRZ Data Read Mode Timing Diagram

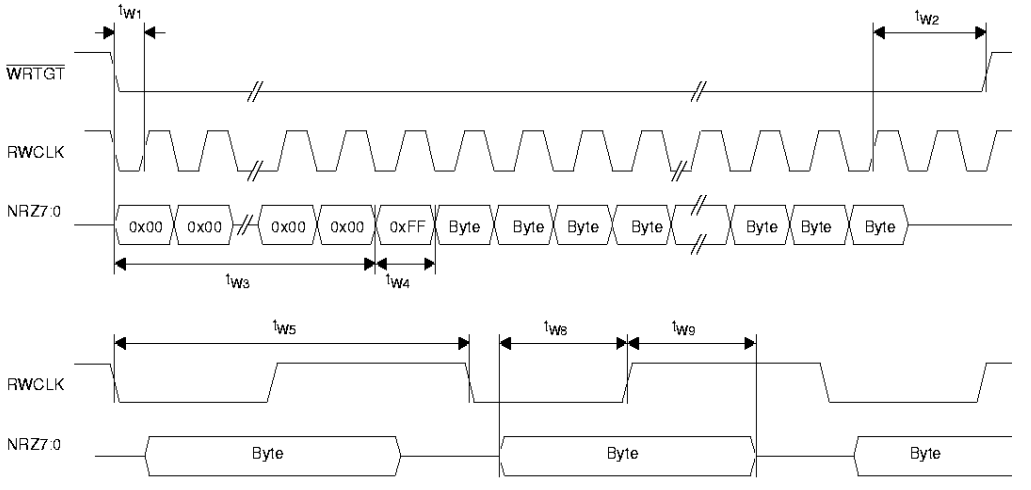
NRZ Data Write Mode

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
t_{W1}	$\overline{WRTGT}$ Assertion to First Rising Edge of RWCLK				$2t_{W5}$	ns
t_{W2}	Last valid data transfer to deassertion of $\overline{WRTGT}$		$3t_{W5}$			ns
t_{W3}	Preamble Length		12			byte
t_{W4}	Sync Mark Length			1		byte
t_{W5}	One Byte Transfer Period	@ 200 Mbit/s, ENDEC enabled		40		ns
		@ 64 Mbit/s, ENDEC enabled		125		ns
		@ 200 Mbit/s, ENDEC bypassed		35.6		ns
		@ 64 Mbit/s, ENDEC bypassed		111.1		ns
t_{W6}	One Nibble Transfer Period	4-bit NRZ, MSB, ENDEC enabled		$4t_{W5/9}$		ns
t_{W7}		4-bit NRZ, LSB, ENDEC enabled		$5t_{W5/9}$		ns
t_{W6}, t_{W7}		4-bit NRZ, MSB & LSB, ENDEC bypassed		$t_{W5/2}$		ns
	RWCLK Duty Cycle	4-bit NRZ, MSB		50		%
		4-bit NRZ, LSB, ENDEC enabled		60		%
		4-bit NRZ, LSB, ENDEC bypassed		50		%
		8-bit NRZ, ENDEC enabled		55.5		%
		8-bit NRZ, ENDEC bypassed		50		%
t_R	RWCLK Rise Time	0.8 to 2.0 V, $C_L \leq 15$ pF			5	ns
t_F	RWCLK Fall Time	2.0 to 0.8 V, $C_L \leq 15$ pF			5	ns
t_{W8}	NRZ7:0 Setup Time				9	ns
t_{W9}	NRZ7:0 Hold Time				4	ns



In Training mode the Sync Mark is written at the location of the first 0xF input nibble. The nibbles MSB and LSB must be input on NRZ3:0. The data written is from the Pattern Generator.

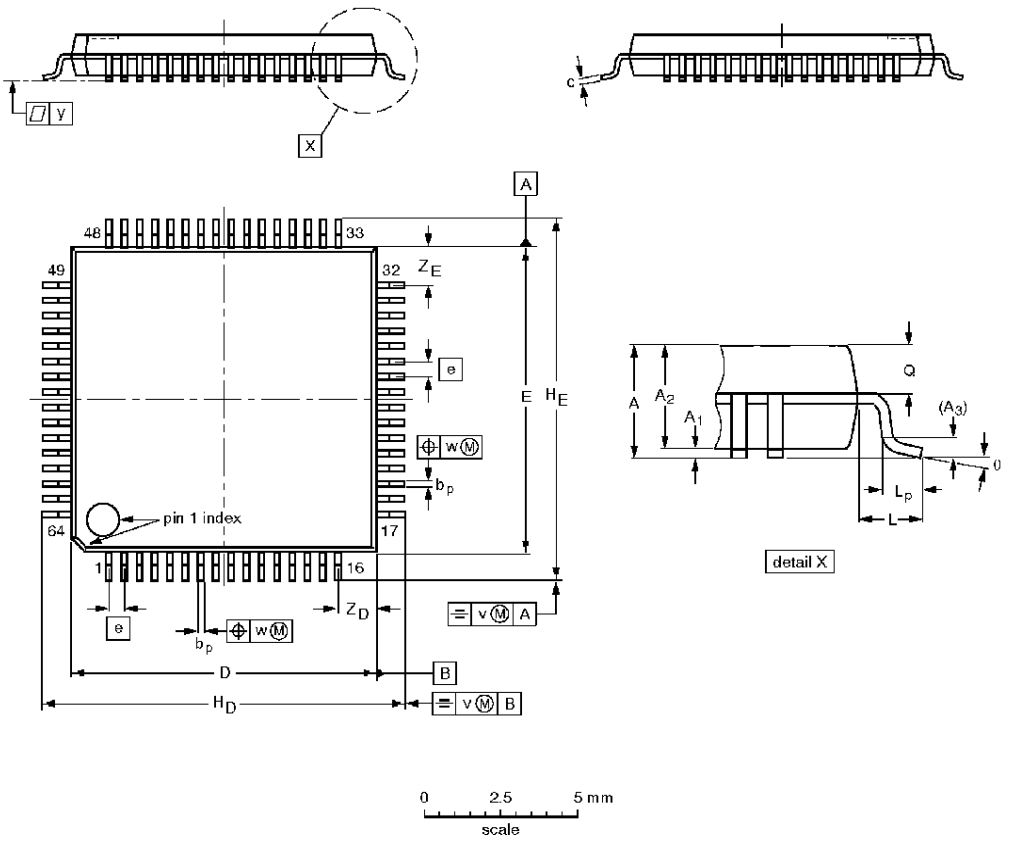
FIGURE 14. 4-Bit NRZ Data Write Mode Timing Diagram



In Training mode the Sync Mark is written at the location of the first 0xFF input byte. Data "Byte" must be input on NRZ7:0. The data written is from the Pattern Generator.

FIGURE 15. 8-Bit NRZ Data Write Mode Timing Diagram

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-02-25

FIGURE 16. Package Diagram

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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