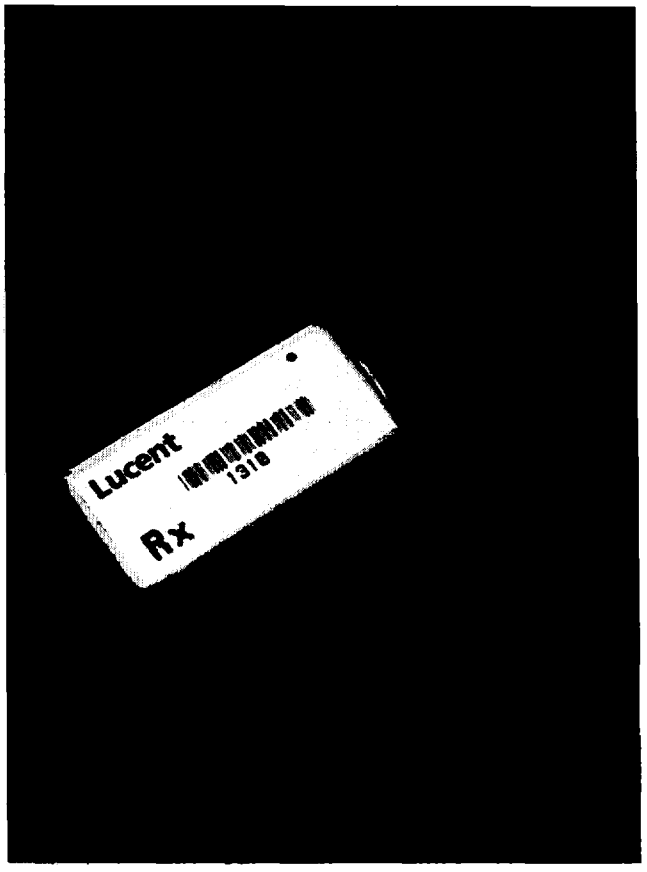
Data Sheet
November 1996

microelectronics group

Lucent Technologies
Bell Labs Innovations

1310-Type *ASTROTEC*® Lightwave Receiver



The 1310-Type Receiver is manufactured in a 20-pin DIP with a multimode fiber pigtail.

Features

- Data rates to 1100 Mbits/s
- Wide dynamic range
- SONET/SDH compliant models for OC-3/STM-1 and OC-12/STM-4
- Space-saving, self-contained, 20-pin DIP
- Single +5 V power supply operation
- Lucent Technologies Microelectronics Group's Reliability and Qualification Program for built-in quality
- Meets requirements for uncontrolled environments as specified in Bellcore 983
- Positive ECL (PECL) data outputs
- Link status flag
- Operating case temperature ranges of 0 °C to +65 °C and –40 °C to +85 °C

Applications

- Telecommunications
  - —Inter- and intraoffice SONET/SDH
  - —Subscriber loop
  - —Metropolitan area networks
- High-speed data communications
  - —Fibre channel
  - —Single-mode *ESCON**
  - —Single-mode FDDI
  - —Asynchronous transfer mode
  - —Gigabit ethernet

* *ESCON* is a registered trademark of International Business Machines Corporation.

Description

The 1310-Type *ASTROTEC* Lightwave Receiver is designed for use in transmission systems or medium- to high-speed data communications applications at data rates up to 1100 Mbits/s. Compact packaging, along with wide dynamic range, makes these receivers ideal for both telecommunications and data communications applications.

Three versions of the receiver are available: SONET/SDH compliant for the OC-3/STM-1 data rate of 155 Mbits/s, SONET/SDH compliant for the OC-12/STM-4 data rate of 622 Mbits/s, and a high-speed version for operation at data rates up to 1100 Mbits/s for applications such as fibre channel.

The SONET/SDH versions of the receiver are fully compliant with the latest issue of Bellcore GR-253-CORE and the most recent issues of ITU recommendations G.957 and G.958.

The 155 Mbits/s 1310-type receiver requires only a single +5 V power supply for operation. However, the 622 Mbits/s and 1100 Mbits/s receivers require an additional –5 V power supply for the PIN bias. All versions of the receiver are characterized for operation over the case operating range of –40 °C to +85 °C at data rates from 20 Mbits/s to the maximum data rate specified for each version.

Manufactured in a 20-pin DIP, the receivers use a planar, rear illuminated InGaAs PIN photodetector that allows these receivers to be used at wavelengths from 1.1 µm to 1.6 µm. The photocurrent output of the PIN detector is amplified and converted to a voltage by a GaAs transimpedance amplifier. A silicon quantizer provides additional signal amplification, data threshold detection, and PECL data outputs. The incoming optical signal is coupled into the receiver through a 62.5 µm core multimode fiber pigtail. Depending on model selected, the outer jacket diameter of the pigtail will be either 900 µm or 2400 µm. The receiver can be ordered with the pigtail terminated in an FC/PC, *ST*®, or SC optical connector. Other connectors are available on special order. See your Lucent account representative for ordering conditions and information.

The receiver has differential PECL data outputs and, depending on version selected, either differential PECL link status flag or complementary CMOS link status flag outputs. The link status flag outputs indicate the presence or absence of a minimum acceptable level of optical input signal.

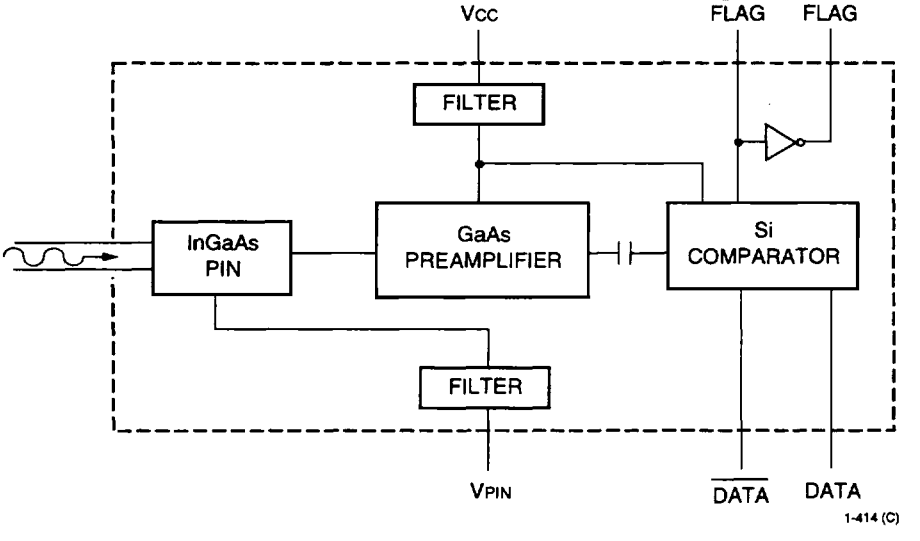


Figure 1. Block Diagram

Description (continued)

To help ensure high product reliability and customer satisfaction, Lucent is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing and shipping process. Lightwave subsystems are qualified to Lucent internal standards using MIL-STD-883 test methods and procedures and sampling techniques consistent with Bellcore requirements. The 1310 receiver has been subjected to the qualification test program outlined in the table of qualification tests shown later in this document. The 1310 receiver qualification program meets the intent of Bellcore TR-NWT-000468 and TA-TSY-000983.

Application Information

The 1310 receiver is a highly sensitive fiber-optic receiver. Although the data outputs are digital logic levels (PECL), the device should be thought of as an analog component. When laying out the printed-wiring board (PWB), the 1310 receiver should be given the same type of consideration one would give to a sensitive analog component.

At a minimum, a double-sided printed-wiring board with a large component-side ground plane beneath the receiver must be used. In applications that include many other high-speed devices, a multilayer PWB is highly recommended. This permits the placement of power and ground connections on separate layers, which helps minimize the coupling of unwanted signal noise into the power supplies of the receiver.

Layout Considerations

A fiber-optic receiver employs a very high-gain, wide-bandwidth transimpedance amplifier. The amplifier detects and amplifies signals that are only tens of nA in amplitude. Any unwanted signal currents that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's loss of signal (FLAG) circuit.

To minimize the coupling of unwanted noise into the receiver, route high-level, high-speed signals such as transmitter inputs and clock lines as far away as possible from the receiver pins. If this is not possible, then the PWB layout engineer should consider interleaving the receiver signal and flag traces with ground traces in order to provide the required isolation.

Noise that couples into the receiver through the power supply pins can also degrade device performance. The application schematics, Figures 3—5, show recommended power supply filtering that helps minimize noise coupling into the receiver. The bypass capacitors should be high-quality ceramic devices rated for RF applications. They should be surface-mount components placed as close as possible to the receiver power supply pins. The ferrite bead should have as high an impedance as possible in the frequency range that is most likely to cause problems. This will vary for each application and is dependent on the signaling frequencies present on the application circuit card. Surface-mount, high-impedance beads are available from several manufacturers.

Data and Flag Outputs

The data outputs of the 1310 receiver are driven by open-emitter NPN transistors which have an output impedance of approximately 7 Ω. Each output can provide approximately 50 mA maximum output current. Due to the high switching speeds of ECL outputs, transmission line design must be used to interconnect components. To ensure optimum signal fidelity, both data outputs (DATA and $\overline{\text{DATA}}$) should be terminated identically. The signal lines connecting the data outputs to the next device should be equal in length and should have matched impedances. Controlled impedance stripline or microstrip construction must be used in order not to degrade the quality of the signal into the next component and to minimize reflections back into the receiver. Excessive ringing due to reflections caused by improperly terminated signal lines makes it difficult for the component receiving these signals to decipher the proper logic levels and may cause transitions to occur where none were intended. Also, by minimizing high frequency ringing due to reflections caused by improperly designed and terminated signal lines, possible EMI problems can be avoided. The applications sections in the Signetics* *ECL 10K/100K* Data Manual or the National Semiconductor† *ECL Logic Databook and Design Guide* provide excellent design information on ECL interfacing.

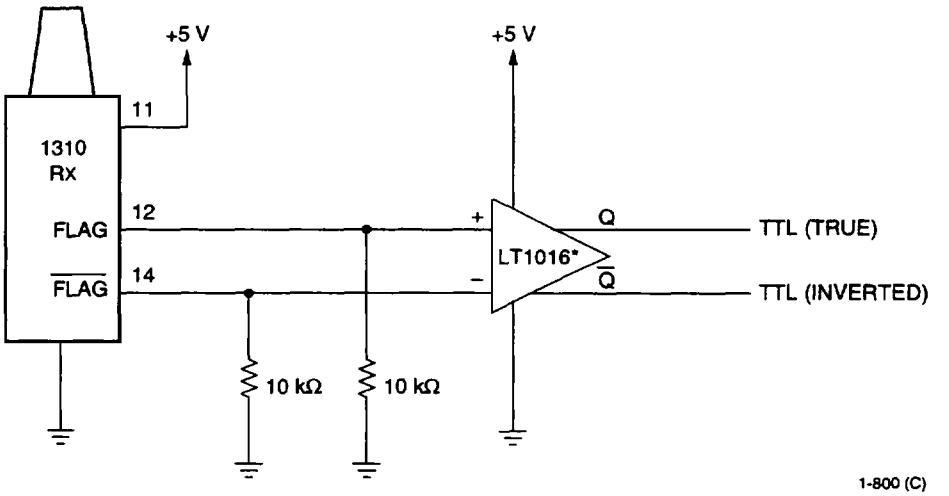
The FLAG and $\overline{\text{FLAG}}$ outputs of the OC-3/STM-1 155 Mbits/s version of the 1310 receiver are PECL logic levels driven by open emitter transistors with the same characteristics as the data outputs. These outputs must be properly terminated in order to obtain the correct logic levels. Since the FLAG function is basically a dc switch which indicates the loss of optical

* *Signetics* is a registered trademark of Signetics Corp.
† *National Semiconductor* is a registered trademark of National Semiconductor Corporation.

Application Information (continued)

input signal, it can be interfaced to much slower TTL or CMOS logic circuits. The circuit shown in Figure 2 provides one example of how to create a TTL logic output from the PECL FLAG output signal. The outputs of the LT1016 are TTL-compatible and provide both true and inverted logic levels. The Q output of this circuit will be a TTL high (>2.5 V) when the 1310 is receiving an optical signal greater than the FLAG switching threshold and will be a TTL low (<0.4 V) whenever the optical signal is absent or is below the FLAG switching threshold.

The FLAG and $\overline{\text{FLAG}}$ outputs of the OC-12/STM-4 622 Mbits/s receiver and the 1 Gbits/s receiver are +5 V TTL logic level compatible. The $\overline{\text{FLAG}}$ output is provided directly by the comparator IC. However, the FLAG output is derived from the $\overline{\text{FLAG}}$ output through an inverter. Excessive loading of the $\overline{\text{FLAG}}$ output can cause the FLAG output to malfunction.



* Part available from Linear Technology Corporation of Milpitas, CA 95035.

Figure 2. Converting PECL FLAG Outputs to TTL

Recommended User Interface

The 1310 receiver is designed to be operated from a +5 V power supply and provides raised or pseudo-ECL (PECL) data outputs. Figures 3 and 4 show two possible application circuits for the 1310 receiver. Figure 3 represents an application for the version with PECL FLAG outputs while Figure 4 shows a possible application for the version with the TTL-compatible FLAG outputs.

In both instances, the DATA outputs are terminated with a Thévenin equivalent circuit, which provides the equivalent of a 50 Ω load terminated to (Vcc – 2 V). A single 50 Ω resistor terminated to (Vcc – 2 V) could also be used, but this requires a second power supply. Other methods of terminating ECL-type outputs are discussed in the references previously mentioned.

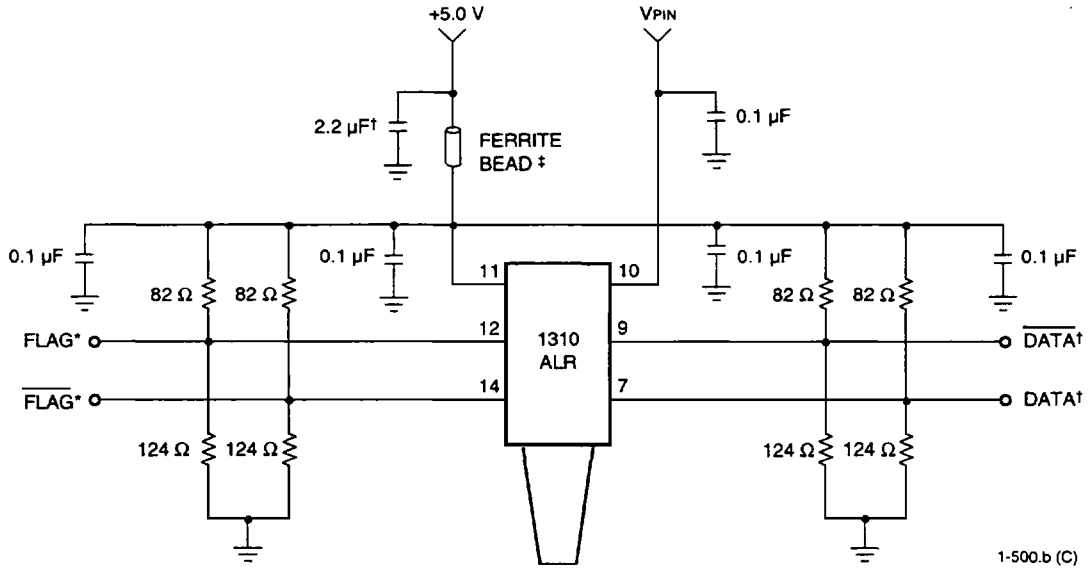
Figure 5 shows an example of a circuit that can be used to interface the PECL outputs of the 1310 receiver with a device which requires true, negative voltage ECL inputs. The 100314 is an ECL line receiver and is shown here only as an example to demonstrate this coupling procedure. The DATA lines are terminated in a 50 Ω equivalent impedance but are ac-coupled to the 100314. The capacitive coupling isolates and permits level shifting of the positive DATA outputs of the receiver to the proper negative level required by the inputs of the 100314. The V_{BB} output of the 100314 provides the reference voltage required to center the voltage swing of the DATA signals around the input switching threshold of the 100314. The Thévenin equivalent of the 166 Ω and 250 Ω resistor pair is 100 Ω, which, in parallel with the 100 Ω resistor connected to V_{BB}, results in a 50 Ω equivalent impedance for the load on each of the data lines. Alternatively, if there is no V_{BB} reference available, a second pair of 166 Ω/250 Ω resistor networks could be used on the data lines on the 100314 side of the coupling capacitor.

V_{PIN} (Pin 10)

This lead supplies bias for the PIN photodetector diode.

For the 155 Mbits/s receiver codes, this input can be grounded or connected to a negative voltage between 0 and –10 V. DO NOT LEAVE THIS PIN UNCONNECTED! The advantage to using a negative bias is a slight improvement in receiver overload capability and, by using a separate negative power supply and a series resistor, it is possible to monitor the PIN photocurrent to create high- or low-limit alarms.

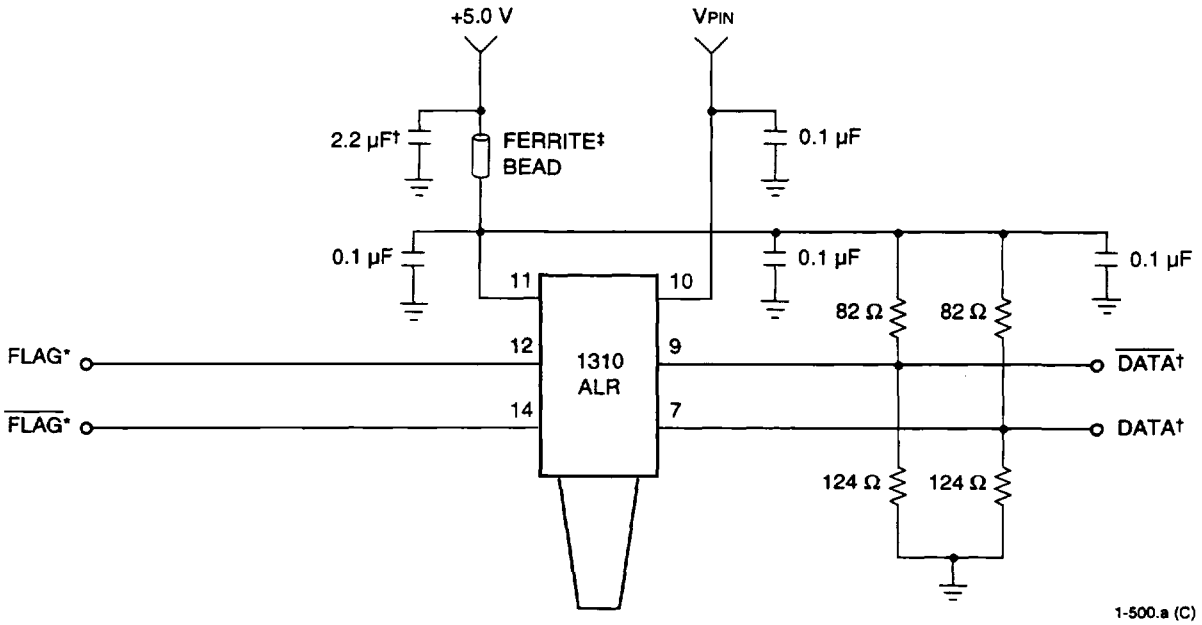
For the 622 Mbits/s and 1.1 Gbits/s receiver codes, this pin should be biased with a negative voltage to guarantee optimum receiver performance.



* 50 Ω to (VCC – 2) V.
† DATA and $\overline{\text{DATA}}$ are 50 Ω impedance transmission lines; both lines can be ac- or dc-coupled into the next device.
‡ Fair-Rite Products Corporation part number 2743037447 or equivalent.
Note: All unused outputs must be terminated as shown. All resistors are 1/8 W, thin-film, ceramic chips. All capacitors are 25 Vdc, ceramic X7R or equivalent

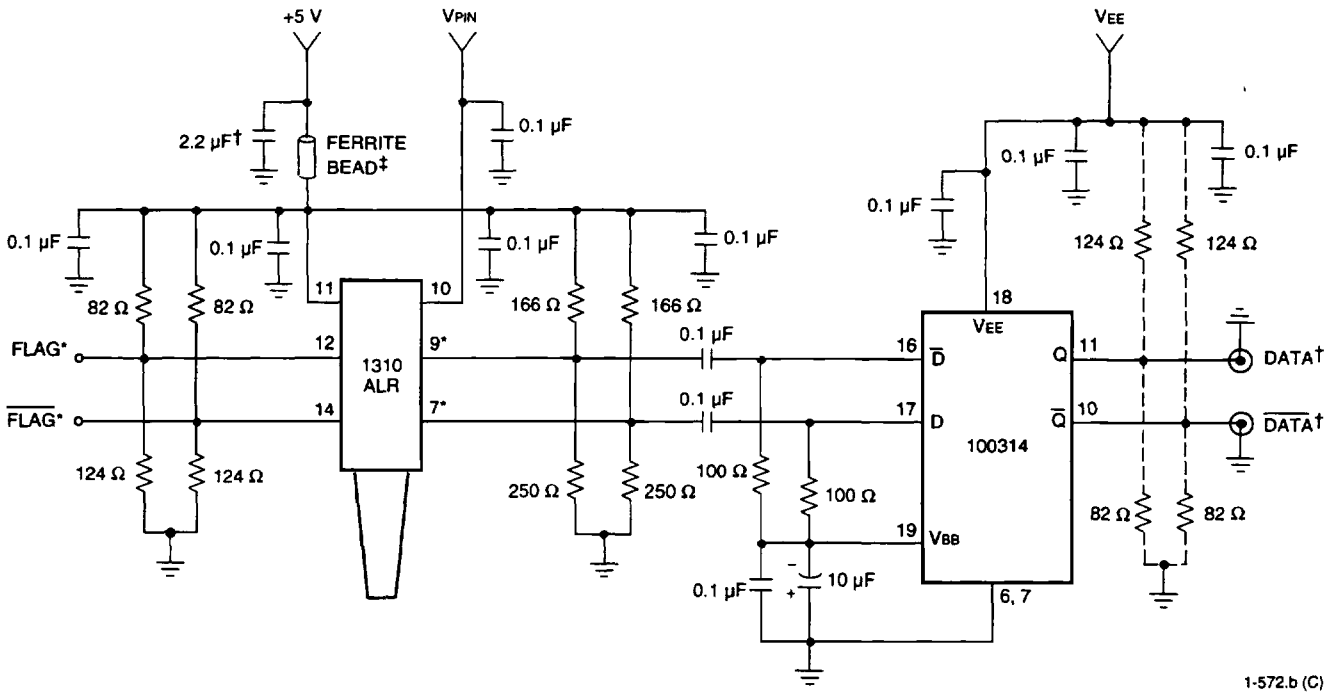
Figure 3. Interfacing to the 155 Mbits/s 1310 Receiver

Recommended User Interfaces (continued)



* TTL (CMOS) compatible level.
† DATA and $\overline{\text{DATA}}$ are 50 Ω impedance transmission lines; both lines can be ac- or dc-coupled into the next device.
‡ Fair-Rite Products Corporation part number 2743037447 or equivalent.

Figure 4. Interfacing to the 622 Mbits/s and 1100 Mbits/s 1310 Receivers



* 50 Ω to (VCC – 2) V.
† 50 Ω to –2 V. DATA and $\overline{\text{DATA}}$ are 50 Ω impedance transmission lines.
‡ Fair-Rite Products Corporation part number 2743037447 or equivalent.

Figure 5. Interfacing the 155 Mbits/s 1310 Receiver to a True ECL Circuit

Pin Information

Pin Number	Description
1	Ground
2	Ground
3	Ground
4	Ground
5	No User Connection*
6	Ground
7	DATA
8	Ground
9	$\overline{\text{DATA}}$
10	PIN Detector Bias (V_{PIN})†
11	Vcc (+5 V)
12	FLAG‡
13	Ground
14	$\overline{\text{FLAG}}$
15	Ground
16	Ground
17	No User Connection*
18	No User Connection*
19	No User Connection*
20	No User Connection*

* Pins designated as No User Connection are not connected internally within the receiver. However, to allow for future functional upgrades, it is recommended that the user not make any connections to these pin positions.

† This pin must either be grounded or biased within the limits shown in Table 1.

‡ The link-status flag is a logic output that indicates the presence or absence of a minimum acceptable level of optical input. A logic high on FLAG indicates the presence of a valid optical signal.

Handling Precautions

Mounting and Connections

The pigtail consists of a 39 in. ± 4 in. (1 m ± 10 cm), 62.5 µm core/125 µm cladding multimode fiber. The standard fiber has a 0.094 in. (2.4 mm) diameter, PVC jacket. However, some codes, as indicated in Table 3, have a 0.036 in. (914 µm) diameter PVC jacket.

The minimum fiber bending radius during operation is 1.5 in. (38 mm).

Electrostatic Discharge

Caution: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow JEDEC Publication No. 108-A.

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Lucent employs a human-body model (HBM) for ESD susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold established for the 1310 receiver is ±1000 V.

Receiver Processing

The 1310-type receiver devices can withstand normal wave-soldering processes. The complete receiver module is not hermetically sealed; therefore, it should not be immersed in or sprayed with any cleaning solution or solvents. The process cap and fiber pigtail jacket deformation temperature is 85 °C. The receiver pins can be wave-soldered at 250 °C for 10 seconds.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations section of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	T_C	–40	85	°C
Storage Case Temperature	T_{stg}	–40	85	°C
Operating Wavelength Range	λ	1.1	1.57	µm
Supply Voltages	V_{CC}	—	5.5	V
	V_{PIN}	0	–15	V
Lead Soldering Temperature/Time	—	—	250/10	°C/s

Operating Characteristics

Values specified over operating case temperature range.

Table 1. Optical Characteristics

At 1.3 µm wavelength operation, 10^{-10} BER over rated operating temperature range.

Parameter	Symbol	Data Rate (Mbits/s)	Min	Typ*	Max	Unit
Measured Average Sensitivity†	P_R	155	–36	–38	—	dBm
		622	–29	–32	—	dBm
		1106	–25	–29	—	dBm
Maximum Input Power†	P_{MAX}	155	–3.0	0	—	dBm
		622	–3.0	0	—	dBm
		1106	–5.0	0	—	dBm
Link Status Switching Threshold						
Decreasing Light Input	LST_D	155	–53.0	–40	–36.0	dBm
		622	–45.0	–34	–28.0	dBm
		1106	–36.0	–31	–26.0	dBm
Increasing Light Input	LST_I	155	–52.0	–38	–35.2	dBm
		622	–52.0	–31	–27.2	dBm
		1106	–35.5	–29	–25.2	dBm
Detector Responsivity	$\Re$	All Data Rates	0.6	0.8	0.95	A/W

* Typical values are measured at room temperature and beginning of life.
† For 1 x 10^{-10} BER with an optical input using a $2^{23} - 1$ pseudorandom word having a 50% average duty cycle.

Operating Characteristics (continued)

Table 2. Electrical Characteristics

Parameter	Symbol	Min	Typ*	Max	Unit
dc Power Supply Voltages	V_{CC}	4.8	5.0	5.3	V
	V_{PIN}†	—	—	−10	V
dc Power Supply Currents	I_{CC}	—	80	150	mA
	I_{PIN}	—	—	1	mA
Output Data Voltage‡					
Low	V_{OL}	−1.81	−1.70	−1.62	V
High	V_{OH}	−1.025	−0.95	−0.88	V
Output Rise Time/Fall Time					
155 Mbits/s Code	t_R/t_F	—	700	1400	ps
622 Mbits/s Code	t_R/t_F	—	350	400	ps
1100 Mbits/s Code	t_R/t_F	—	350	400	ps
Output Flag Voltage					
155 Mbits/s Code‡					
Low	V_{FL}	−1.81	−1.75	−1.62	V
High	V_{FH}	−1.025	−0.95	−0.88	V
622 Mbits/s and 1100 Mbits/s§					
Low	V_{FL}	0	—	0.5	V
High	V_{FH}	4.5	—	V_{CC}	V
Output Data Current‡					
Low	I_{OL}	—	5	50	mA
High	I_{OH}	—	20	50	mA
Output Flag Current					
155 Mbits/s Code					
Low	I_{OL}	—	5	50	mA
High	I_{OH}	—	20	50	mA
622 Mbits/s and 1100 Mbits/s					
Low	I_{OL}	0	10	15	mA
High	I_{OH}	0	10	15	mA

* Typical values are measured at room temperature and beginning of life.
† Optional for 155 Mbits/s codes. −5 V typical for 622 Mbits/s and 1100 Mbits/s codes. See V_{PIN} description.
‡ Measured from V_{CC} with a 50 Ω load to (V_{CC} − 2) V.
§ Internally terminated CMOS output.

Qualification Tests

The 1310-type receiver has successfully passed the following qualification tests and meets the intent of Bellcore TR-NWT-000468 and TA-TSY-000983.

Test	Conditions	Sample Size	Failure Criteria
Physical Dimensions	MIL-STD-883C-2016	90	Visual
External Visual	MIL-STD-883C-2009.8	90	Visual
Impact Shock	1500G, 5 hits, 6 dir., MIL-STD-883C-2002, Condition B	11	Electrical/optical
Variable Frequency Vibration	20G, 20 Hz to 2 kHz, 4 cycles, 3 directions, 4 min./cycle, MIL-STD-883C-2007.1	11	Electrical/optical
Solderability	MIL-STD-883C-2003.6	5	Visual
Lead Integrity	MIL-STD-883C-2004.5	5	Visual
Solvent Resistance	MIL-STD-883C-2015.7	5	Visual
Temperature Cycle	–40 °C to +85 °C, 500 cycles, MIL-STD-883C-1010.7	11	Electrical/optical
High Temperature, High Humidity, with Bias	85 °C, 85% relative humidity, rated bias, 2,000 hours	38	Electrical/optical
High Temperature with Bias	85 °C ambient, rated bias, 5,000 hours, MIL-STD-883C-1005.5	25	Electrical/optical
Internal Visual	MIL-STD-883C-2014	10	Visual
Electrostatic Discharge	Human-body model (to determine class)	3	Electrical/optical
Fiber Pull	1 kg	11	Electrical/optical
Low-temperature Storage	–40 °C, 2,000 hours	11	Electrical/optical
Voltage Stress	Maximum rated voltage	10	Electrical/optical
Power Cycling	MIL-STD-1006	5	Electrical/optical
Flammability	Fiber cable meets *UL** listed OFN	—	—

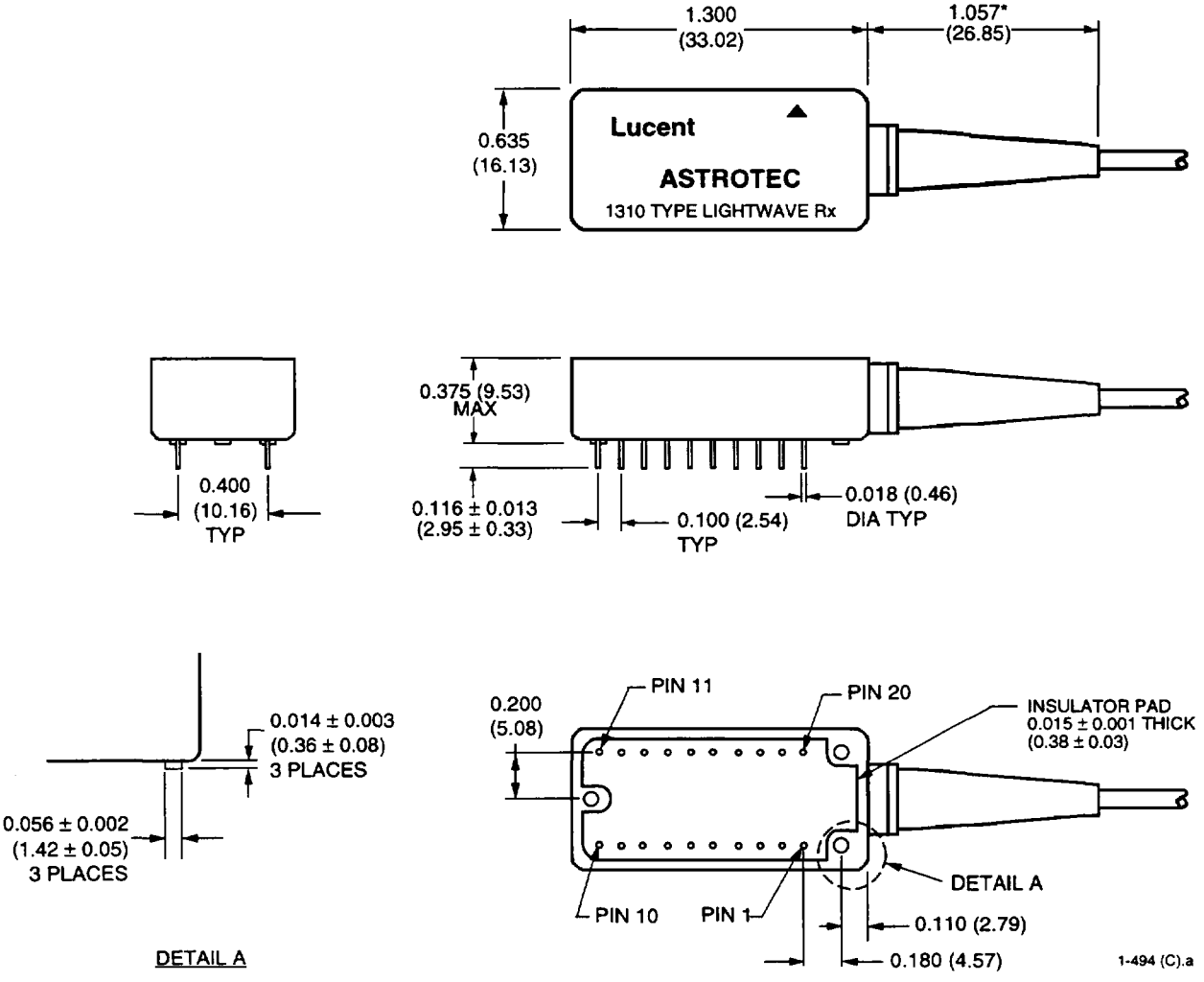
* *UL* is a registered trademark of Underwriters Laboratories, Inc.

Outline Diagram

Dimensions are in inches and (millimeters).

Tolerances are ±0.005 in. (±0.127 mm).

Weight = 1.3 oz. (37 g).



* Note: On receivers with 900 µm OD fiber, this dimension is 1.265 in. (32.13 mm).

Ordering Information

Table 3. 1310-Type Receiver Ordering Information

1310-Type Lightwave Receiver Options			Product Order Code	Lucent Comcode
Data Rate (Mbits/s)	Operating Case Temperature Range (°C)	Connector*		
155	0 to 65	FC-PC	1310C	106191885
155	0 to 65	*ST*	1310L†	106277379
155	0 to 65	SC	1310CB†	106924038
155	–40 to +85	FC-PC	1310E	106191901
155	–40 to +85	*ST*	1310N	106277403
155	–40 to +85	SC	1310ED†	106985336
622	0 to 65	FC-PC	1310MC	107231912
622	0 to 65	*ST*	1310MA†	107231896
622	0 to 65	SC	1310MB†	107231904
622	–40 to +85	FC-PC	1310PC	107231961
622	–40 to +85	*ST*	1310PA†	107231946
622	–40 to +85	SC	1310PB†	107231953
1100	0 to 65	FC-PC	1310GB	107841629

* These connectors listed are for standard product. Other connectors are available on special order.
† These codes have 900 µm OD multimode fiber pigtails. All others are 2400 µm OD.

Table 4. Related Products

Product	Description
1330B-Type	OC-3/STM-1 receiver module with integrated PLL clock recovery
1330D-Type	OC-12/STM-4 receiver module with integrated PLL clock recovery
1320	OC-12/STM-4 receiver module with integrated SAW filter clock recovery
1227	Uncooled 1.3 µm F-P laser transmitter for SONET/SDH applications
1229	Uncooled 1.3 µm or 1.55 µm DFB laser transmitter for SONET/SDH applications

For additional information, contact your Microelectronics Group Account Manager or the following:
OPTOELECTRONICS BUSINESS UNIT: Optoelectronics Center, 9999 Hamilton Blvd., Breinigsville, PA 18031-9359
610-391-2520, FAX 610-391-2535
INTERNET: **http://www.lucent.com/micro**
U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106), e-mail **docmaster@micro.lucent.com**
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
For data requests in Europe:
MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1734 324 299**, FAX (44) 1734 328 148
For technical inquiries in Europe:
OPTOELECTRONICS MARKETING: **(44) 1344 865 900** (Bracknell UK)

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