OKI Semiconductor E2D5029-27-50

MSM9841

Recording and Playback LSI with Built-in FIFO

GENERAL DESCRIPTION

The MSM 9841 is a recording and playback LSI with built-in FIFO memory.

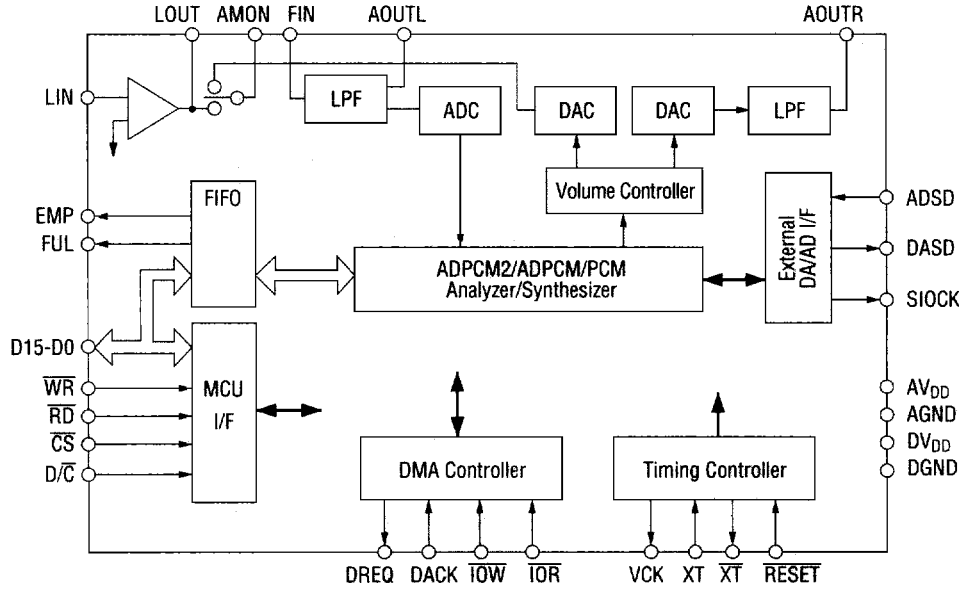
The MSM 9841 is based on the new OKI ADPCM2 system, which implements high sound quality, and recording and playback are controlled by a CPU via a 16/8-bit bus interface.

The MSM 9841 is a voice LSI which is most appropriate for systems which do not use semiconductor memory as the storage medium.

FEATURES

- 16/8-bit bus interface support
- FIFO capacity : 512-bits
  (buffering time of 16 ms when using 8 kHz sampling frequency, 4-bit OKI ADPCM2/ADPCM, and in monaural playback)
- Voice analysis and synthesis system : 4 systems
  4, 5, 6, 7, 8-bit OKI ADPCM2, 4-bit OKI ADPCM, 8, 16-bit PCM, and 8-bit OKI Nonlinear PCM
- Source oscillation frequency : 4.096 MHz
- Sampling frequency : 6.4kHz, 8.0 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz
- Volume control (8 steps: 0 dB-21dB)
- Built-in 14-bit A/D converter
- Built-in 14-bit D/A converter
- Built-in LPF : attenuation factor -40dbm/oct
- Package:
  56-pin plastic QFP (QFP56-P-910-0.65-K) (Product name: MSM9841GS-K)

BLOCK DIAGRAM



PIN DESCRIPTIONS

Symbol	Type	Description
D15-D8	I/O	Voice data input/output pins for 8-bit bus Interface For 16-bit interface, these pins are bidirectional data bus to input/output data with external microcontroller and memory.
D7-D0	I/O	Bidirectional data bus to input/output data and output status with external microcontroller and memory
$\overline{WR}$	I	Write pulse input pin. This pin inputs "L" pulse when command or data is input to D15-D0 pins.
$\overline{RD}$	I	Read pulse input pin. This pin inputs "L" pulse when status or data is output to D15-D0 pins.
$\overline{CS}$	I	Accepts write pulse and read pulse when this pin is "L". Does not accept write pulse and read pulse when this pin is "H".
D/$\overline{C}$	I	Inputs/outputs voice data from D15-D0 pins when this pin is "H" Inputs/outputs command and status from D7-D0 pins when this pin is "L"
EMP	O	"H" level indicates that there is no data in FIFO memory. Output conditions can be changed by command.
FUL	O	"H" level indicates that FIFO memory is full. Output conditions can be changed by command.
DREQ	O	DMA transfer request signal when FIFO is FUL (when recording) or EMP (when playback)
DACK	I	DMA transfer enable acceptance signal. Accepts signal of $\overline{IOR}$ pin and $\overline{IOW}$ pin when this pin is "H".
$\overline{IOW}$	I	Signal to write external memory data to MSM 9841 during DMA transfer
$\overline{IOR}$	I	Signal to read data of MSM 9841 for writing external memory during DMA transfer
ADSD	I	16-bit serial data input pin when external ADC is used
DASD	O	16-bit serial data output pin when external DAC is used
SIOCK	O	Synchronizing clock for 16-bit serial data input/output when external ADC or DAC is used
XT $\overline{XT}$	I O	Oscillator connection pin. When external clock is used, input clock from XT pin and leave $\overline{XT}$ pin open.
VCK	O	Outputs sampling frequency selected at recording/playback. This sampling frequency is used as synchronizing signals when external ADC or DAC is used.
$\overline{RESET}$	I	When "L" is input to this pin, LSI is initialized and enters power down status.
LIN	I	Inverting input pin for built-in OP amplifier Noninverting input pin is connected to SG (Signal Ground) internally.
LOUT	O	Output pin of built-in OP amplifier
AMON	O	Connected to LOUT pin when recording, and to built-in DAC output when playback. Connect this pin to input (FIN pin) for built-in LPF.

Symbol	I/O	Description
FIN	I	Input pin for built-in LPF
AOUTL	O	Left side output pin for built-in LPF. This is the output pin of playback waveforms, and is connected to the amplifier for driving speakers.
AOUTR	O	Right side output pin for built-in LPF. This is the output pin of playback waveforms, and is connected to the amplifier for driving speakers.
DV_{DD}	—	Digital power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and DGND pin.
DGND	—	Digital GND pin
AV_{DD}	—	Analog power supply pin. Insert minimum 0.1 μF bypass capacitor between this pin and AGND pin.
AGND	—	Analog GND pin

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	-0.3 to +7.0	V
Input Voltage	V_{IN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	DGND=AGND=0V	4.5 to 5.5	V
Operating Temperature	T_{op}	—	-40 to +85	°C
Master Clock Frequency	f_{OSC}	—	4.096	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

DV_{DD}=AV_{DD}=4.5 to 5.5V, DGND=AGND=0V, Ta=-40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level Input Voltage	V_{IH}	—	V_{DD}×0.8	—	—	V
Low-level Input Voltage	V_{IL}	—	—	—	V_{DD}×0.2	V
High-level Output Voltage	V_{OH}	I_{OH}=-40μA	V_{DD}-0.3	—	—	V
Low-level Output Voltage	V_{OL}	I_{OL}=2mA	—	—	0.45	V
High-level Input Current (*1)	I_{IH1}	V_{IH}=V_{DD}	—	—	10	μA
High-level Input Current (*2)	I_{IH2}	V_{IH}=V_{DD}	—	—	20	μA
Low-level Input Cerrent (*1)	I_{IL1}	V_{IL}=GND	-10	—	—	μA
Low-level Input Current (*2)	I_{IL2}	V_{IL}=GND	-20	—	—	μA
Operating Current	I_{DD}	f_{OSC}=4.096MHz, without load	—	5	10	mA
Standby Current	I_{DDS}	At power down, without load Ta=-40 to +70°C	—	—	10	μA
		At power down, without load Ta=70 to 85°C	—	—	50	μA

*1 Applies to input pins excluding XT pin.
*2 Applies to XT pin.

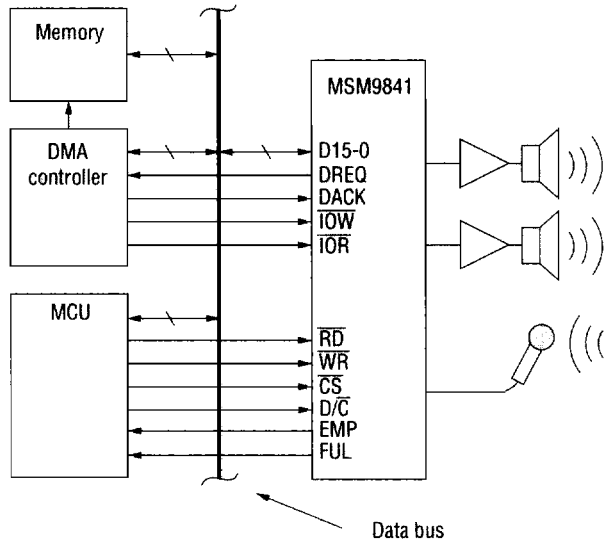
Analog Characteristics

$DV_{DD}=AV_{DD}=4.5$ to 5.5V, DGND=AGND=0V, Ta=-40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
D/A Output Relative Error	$\lvert V_{DAE} \rvert$	No load	—	—	10	mV
FIN Allowable Input Voltage Range	V_{FIN}	—	1	—	V_{DD}-1	V
FIN Input Impedance	R_{FIN}	—	1	—	—	MΩ
OP Amplifier Open Loop Gain	G_{OP}	f_{IN}=0 to 4kHz	40	—	—	dB
OP Amplifier Input Impedance	R_{INA}	—	1	—	—	MΩ
OP Amplifier Output Load Resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT Output Load Resistance	R_{AOUT}	—	50	—	—	kΩ
FOUT Output Load Resistance	R_{FOUT}	—	50	—	—	kΩ

CPU INTERFACE EXAMPLE

1) Interface using DMA controller (for 16-bit bus)



2) Interface with MCU and external memory (for 16-bit bus)