Signetics

54LS195A
Shift Register

4-Bit Parallel Access Shift Register

Product Specification

Military Logic Products

FEATURES

- **Buffered clock and control inputs**
- **Shift right and parallel load capability**
- **J-$\overline{K}$ (D) inputs to first stage**
- **Complement output from last stage**
- **Asynchronous Master Reset**

DESCRIPTION

The functional characteristics of the 54LS195A 4-bit Parallel Access Shift register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The 54LS195A operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input.

Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted 1 bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each Low-to-High clock transition. The J and $\overline{K}$ inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs (D_0 - D_3) is transferred to the respective Q_0 - Q_3 outputs.

Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input low.

ORDERING INFORMATION

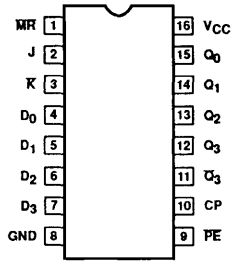
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS195A/BEA
Ceramic Flat Pack	54LS195A/BFA
Ceramic LLCC	54LS195A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
All	Outputs	10LSUL

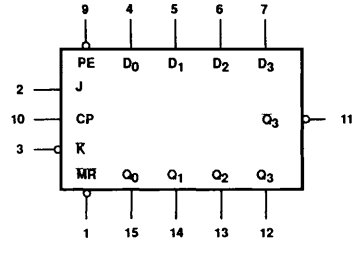
NOTE: Where a 54LS Unit Load (LSUL) is understood to be 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

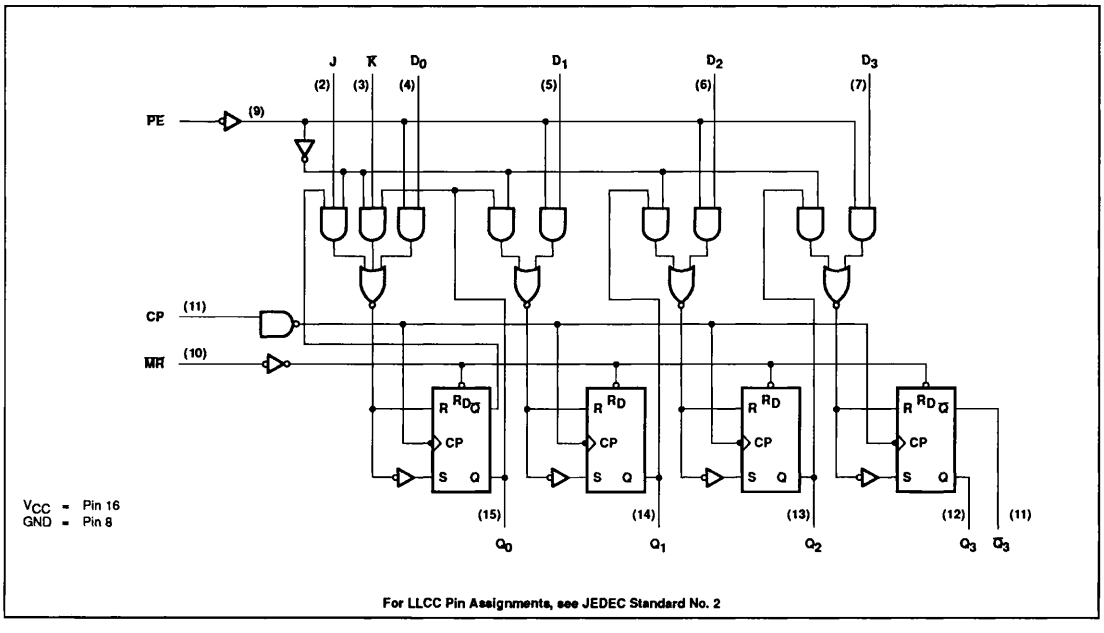
For LLCC pin assignments, see JEDEC Standard No. 2

Shift Register | 54LS195A

All parallel and serial data transfers are synchronous, occuring after each Low-to-High clock transition. The 54LS195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

A Low on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs Low, independent of any other input condition. The $\overline{MR}$ on the 54LS195 is gated with the clock. Therefore, the Low-to-High $\overline{MR}$ transition should only occur while the clock is Low to avoid false clocking on the 54LS195.

LOGIC DIAGRAM



For LLCC Pin Assignments, see JEDEC Standard No. 2

MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
Shift, set first stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, reset first stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, toggle first stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, retain first stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = High voltage level
L = Low voltage level
X = Don't care
l = Low voltage level one setup time prior to the Low-to-High clock transition
h = High voltage level one setup time prior to the Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		14	21	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		22 26	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		30	ns

AC SETUP REQUIREMENTS T_A 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	16		ns
t_W	Master Reset pulse width	Waveform 2	12		ns
t_s	Setup time, J, $\overline{K}$ and data to clock	Waveform 3	15		ns
t_h	Hold time, J, $\overline{K}$ and data to clock	Waveform 3	0		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 4	25		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 4	0		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	25		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 31	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		35	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		35 40	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		46	ns

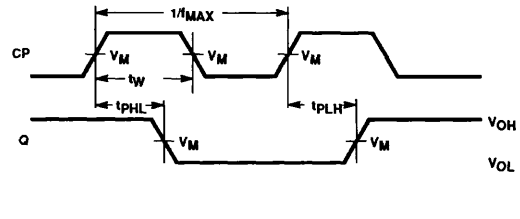
AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	18		ns
t_W	Master Reset pulse width	Waveform 2	12		ns
t_s	Setup time, J, $\overline{K}$ and data to clock	Waveform 3	20		ns
t_h	Hold time, J, $\overline{K}$ and data to clock	Waveform 3	10		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 4	25		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 4	10		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	25		ns

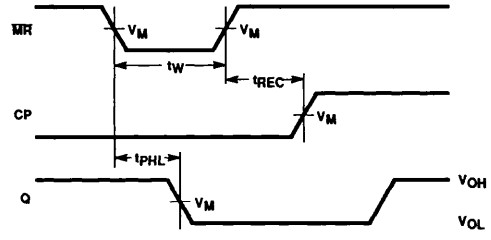
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open, $\overline{PE}$ grounded, and $\geq$ 4.0V applied to the J, $\overline{K}$, and Data inputs, I_{CC} is measured by applying a momentary ground, followed by $\geq$ 4.0V to $\overline{MR}$, and then a momentary ground, followed by $\geq$ 4.0V to clock.
5. These parameters are guaranteed, but not tested.

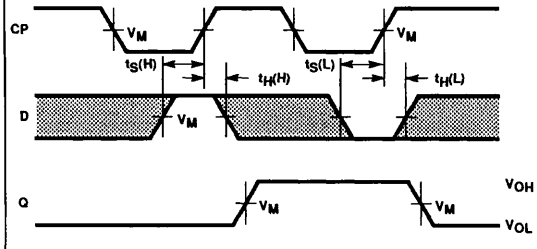
AC WAVEFORMS



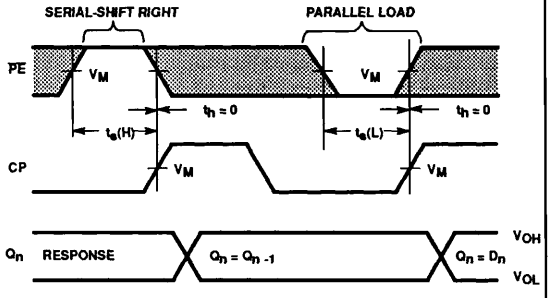
Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



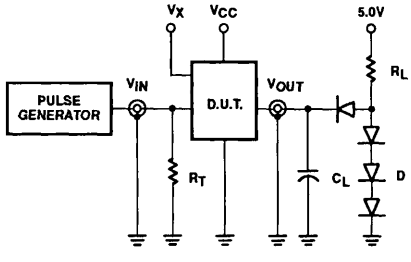
Waveform 3. Data Setup and Hold Times



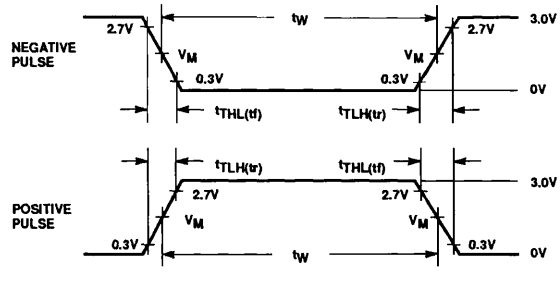
Waveform 4. Setup and Hold Times Parallel Enable to Clock

NOTE: V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.