SAA7323 – Stereo Bitstream D/A converter with digital filter

HBA9004

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ABSTRACT

The SAA7323 is a stereo D/A converter with integrated digital filter intended to be used in medium and high class digital audio applications. An extended temperature range and the single 5 volts supply make the device also suitable for portable and car applications. The use of the new Philips Bitstream conversion technique is giving the SAA7323 the benefits of good linearity and superior low-level performance. All of this is achieved without any external adjustments.

1. INTRODUCTION

The SAA7323 is a complete monolithic stereo 16-bit D/A converter with integrated digital filter [1] primarily intended for use in compact disc players and digital tape recorders.

Due to its extremely high level of integration only few external passive components (e.g., low-pass filter) are required. The device does not need any external adjustments. It is produced in a CMOS process and operates from a single (+5V) supply. An extended temperature range (-40°C to +85°C) makes the SAA7323 suitable both for car and portable applications.

In order to support the user in applying the SAA7323, a functional description, layout recommendations and a number of application concepts are described. To highlight the advantages of the Bitstream conversion technique, typical measurement curves are provided as well.

Note: The SAA7323 is the pin-compatible new version of the SAA7320. A low cost version of the SAA7323 with the part number SAA7322 is available.

2. FUNCTIONAL DESCRIPTION

The SAA7323 is a stereo D/A converter incorporating a four times oversampling FIR filter and two operational amplifiers per channel intended for analog low-pass filtering. A block diagram of the device is shown in Figure 2.1.

The device contains three main parts – a digital four times oversampling FIR low-pass filter, an additional oversampling/noise shaper section and an analog section with switched capacitor networks (SC-Networks) and operational amplifiers for analog post-filtering. Furthermore, an oscillator is integrated to generate the system clock with a frequency of 256 times the sampling frequency.

The interfaces of the SAA7323 (input and output of the digital filter) are according to the I²S standard [3]. All parts of the IC are described in the following chapters.

Figure 2.2 shows the passband and Figure 2.3 the stopband characteristic of this filter.

2.1 Digital Filter

The digital filter is a four times oversampling FIR filter with 128 taps. The coefficients' wordlength is 12 bits while the multiplier and accumulator do have a wordlength of 28 bits.

The output of the filter is scaled down by about 2dB, resulting in a better square-wave behavior (less clipping at full scale signals) and opening the opportunity to implement a compensation for the roll-off of the analog low-pass filter and the linear interpolator (see next chapter). The ripple in the passband is fairly small (±0.035dB).

For frequencies above 0.546 * fs the stopband attenuation is about 60dB. The first image of the passband can be found around 4 * fs.

A mute-function is implemented in the digital filter as well as an attenuation function of 12dB. Another feature of the digital filter is the first order noise shaper at its output. This minimizes the amount of additional quantization noise in the passband, if the 28 bit wordlength of the accumulator is reduced to 16 bit.

The I²S output interface provides digitally filtered data with all the above mentioned benefits.

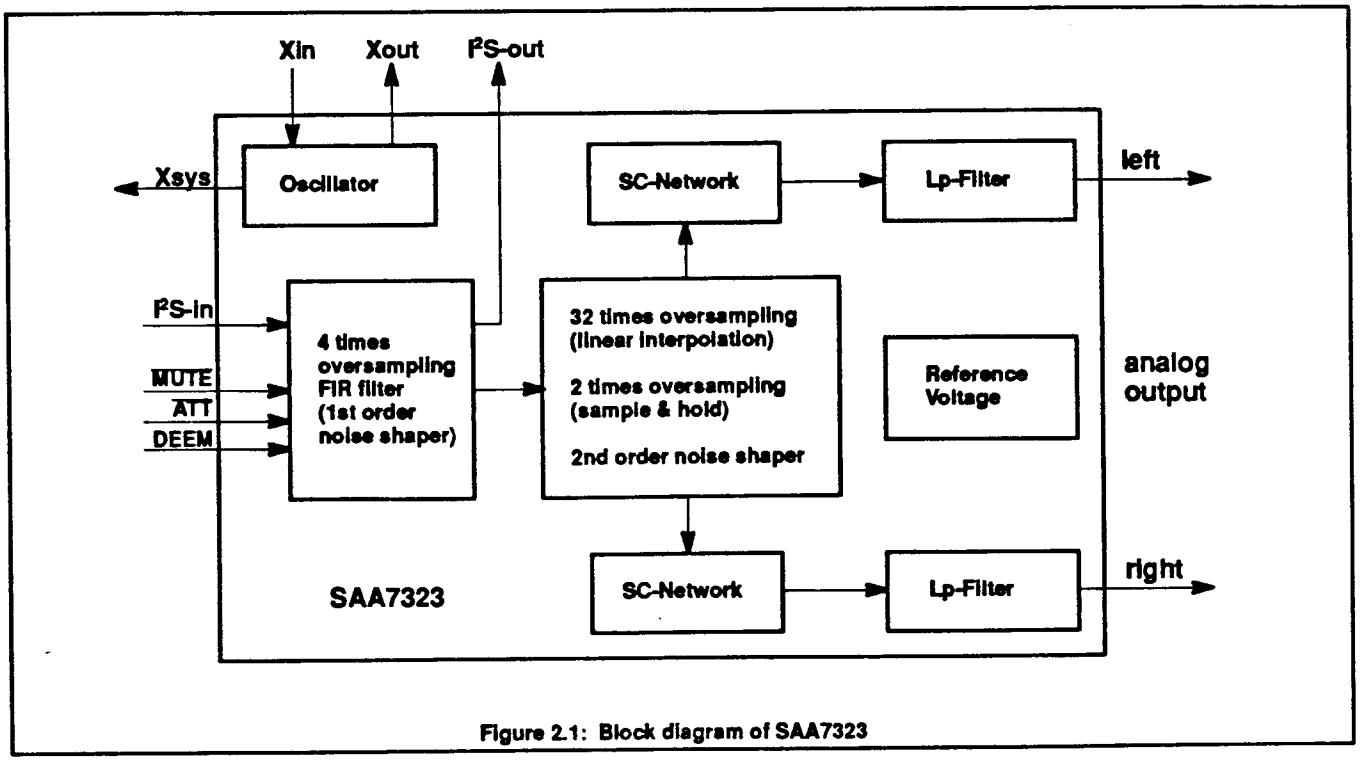

Figure 2.1: Block diagram of SAA7323

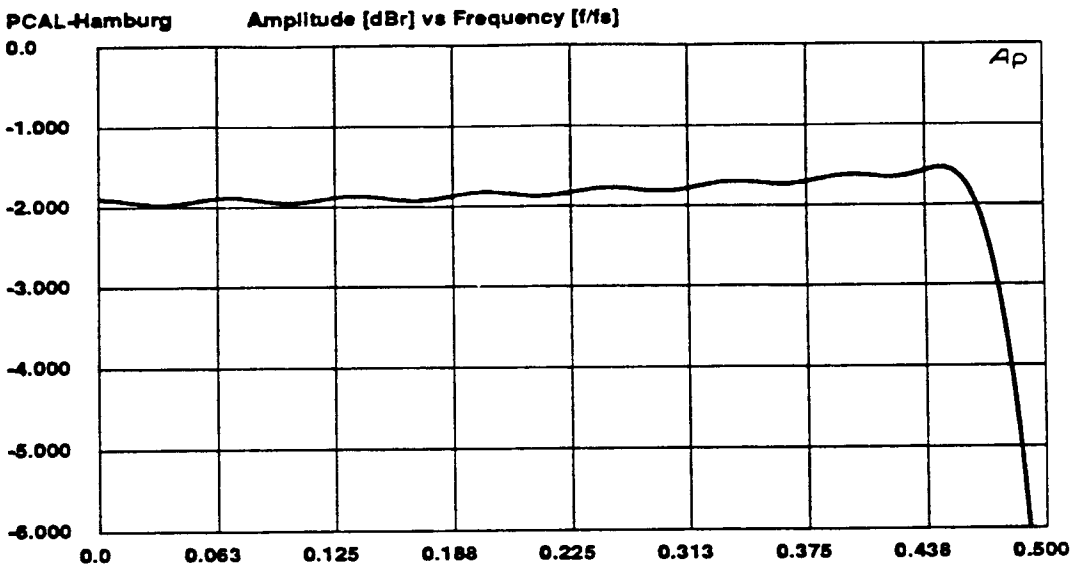

Figure 2.2: **Frequency Response of the Digital Filter (Passband).**
The frequency f is normalized to the sampling frequency f_s.

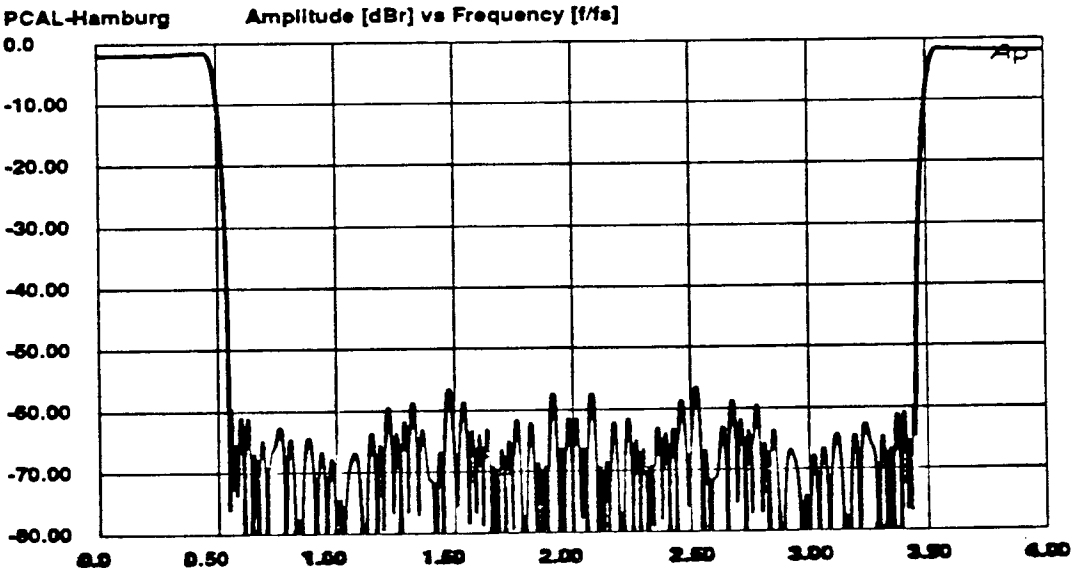

Figure 2.3: **Frequency Response of the Digital Filter (stopband).**
The frequency f is normalized to the sampling frequency f_s.

2.2 Oversampling/Noise Shaper Section

In this section, 32 times oversampling is performed by linear interpolation. The impulse response of a linear interpolator has a triangular waveform, which can be interpreted as a convolution of two hold-functions with rectangular waveform. Thus, the SAA7323 has a frequency roll-off due to the linear interpolator which is equivalent to $(\sin(x)/x)^2$. At the end of the passband (0.45*fs) the roll-off is about -0.38dB. Additional 2 times oversampling is done in a sample and hold stage. This results in a final sample rate of 256 times the sampling frequency which is identical to the system clock frequency of the device.

An internally generated out-of-band dither signal of -20dB at 8*fs is introduced to prevent any idling patterns in the following noise shaper structure. To accommodate the dither signal one MSB is added. Therefore the output of the oversampling stage is 17 bit samples at 256 times the sampling frequency.

This data D(n) is fed into a second order noise shaper. A simplified block diagram is shown in Figure 2.4.

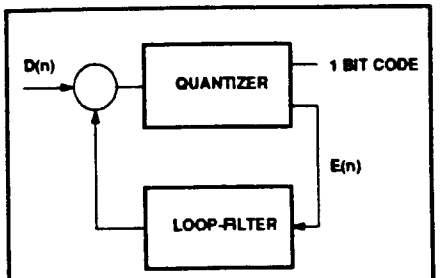

Figure 2.4: Block Diagram of the Noise Shaper

The 1-bit code from the quantizer (codec) is the sign bit. The rest of the sample, referred to as the quantization error E(n), is fed back. A second order loop-filter is implemented in the feedback loop.

With this configuration the S/N ratio in the audio band (20Hz to 20kHz) for a 44.1kHz CD-type application is about 105dB (more details in [4]).

2.3 Switched Capacitor Network

The 1-bit data stream is converted into an analog signal using a switched-capacitor network, the circuit diagram is shown in Figure 2.5. Two control signals representing logic "0" and "1" of the data stream, together with a continuous clock, control the switching of the capacitors C1 and C2 (both are approximately 2.7pF).

Figure 2.6 shows the timing diagram of these signals.

During the negative half of the clock, C2 is charged and C1 is discharged. If the 1-bit data is a logic "1", the capacitor is charged during the positive half of the clock by taking a fixed amount of charge from the summing node of the operational amplifier. For logic"0", a fixed amount of charge is transferred into the summing node from C2.

Feedback capacitor C4 (approximately 85pF) and resistor R1 serve as the first pole of a low-pass filter. C4 is integrated while R1 has to be added externally to define the output signal level.

The function of capacitor C3 is to prevent clipping in the differential input stage of the operational amplifier and has to be added externally.

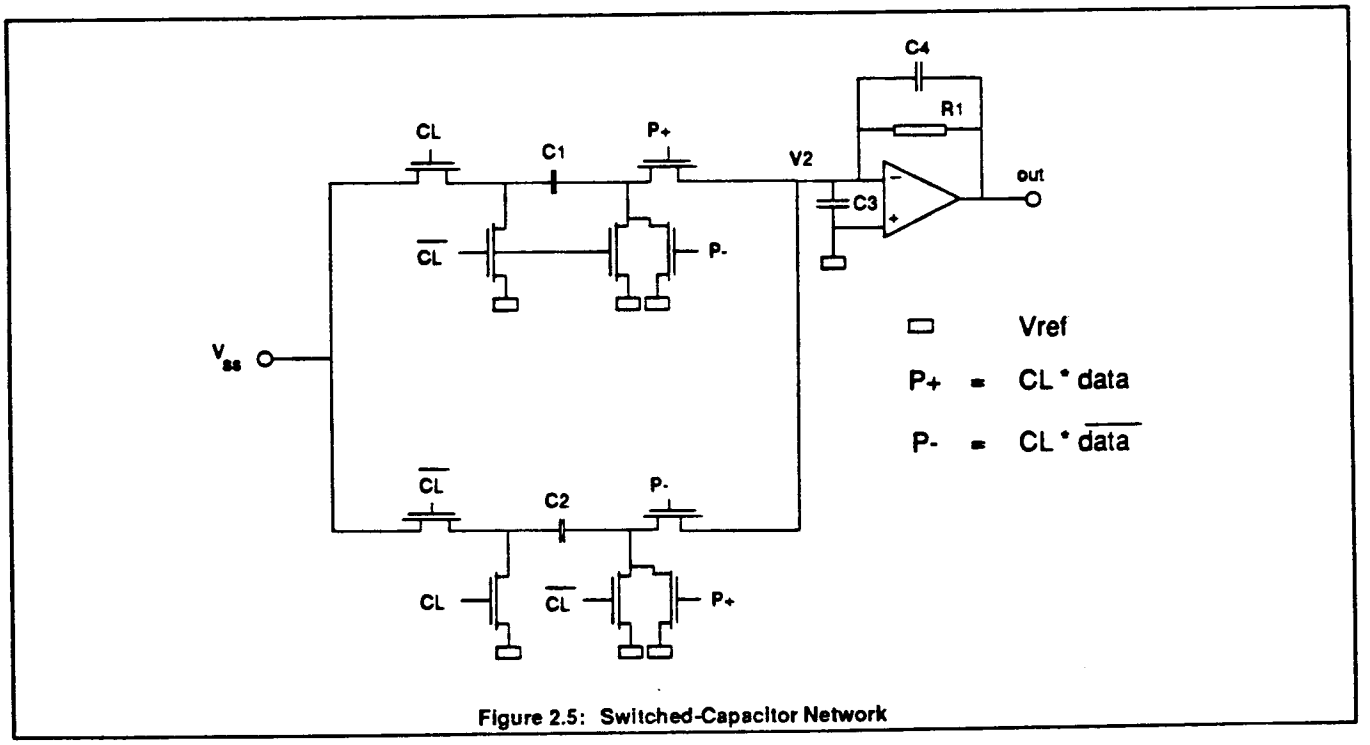

Figure 2.5: Switched-Capacitor Network

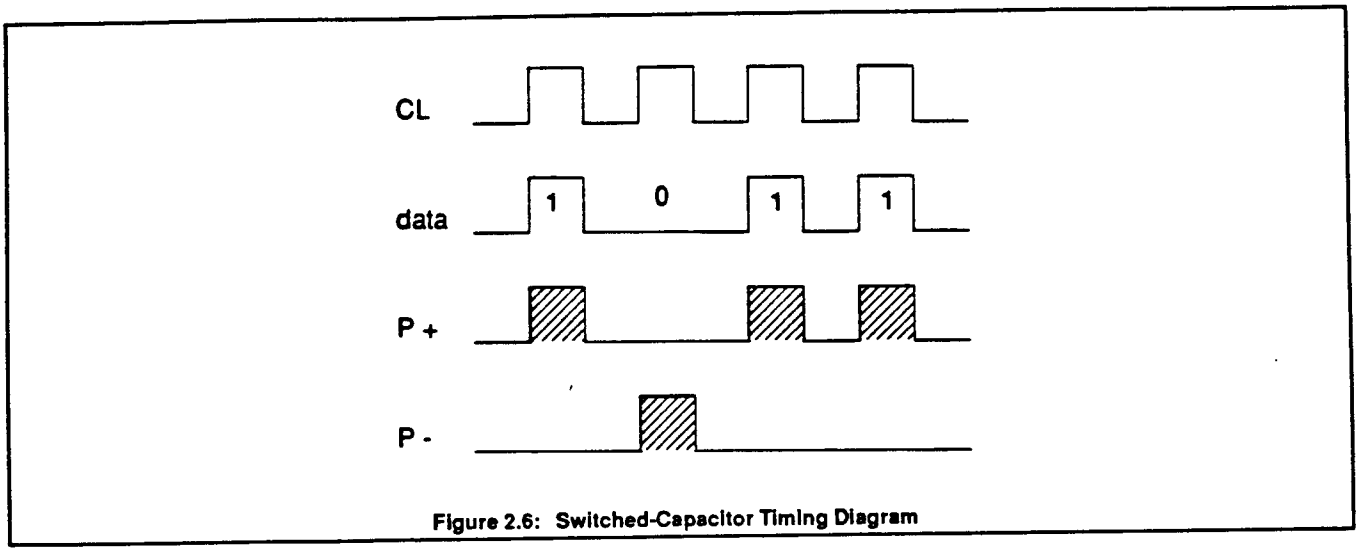

Figure 2.6: Switched-Capacitor Timing Diagram

2.4 Reference Generator

The reference generator (see Figure 2.7) is an operational amplifier in a voltage follower configuration. It is designed for a low input offset voltage and a low dynamic output impedance.

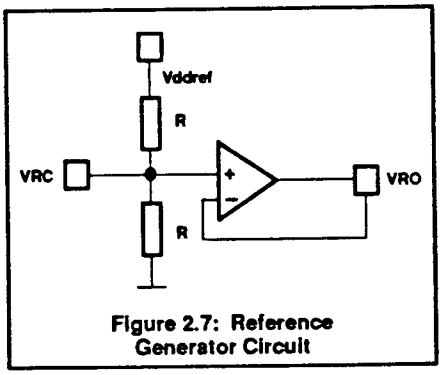

Figure 2.7: Reference Generator Circuit

The reference generator has three external connections: the reference generator input (VRC), the reference generator output (VRO), used to provide the reference voltage for the switched capacitor network, and Vddref. Vss is supplied from Vssa which is the main analog ground connection.

A reference voltage of Vddref/2 is provided at the voltage follower input. The feedback loop includes the sense line to the VRO pad, thus taking into account any voltage drop that may occur in the drive line from the output of the operational amplifier to the VRO pad.

For any kind of application the VRC voltage has to be a clean as possible, because any noise on this line is transferred to the output of the reference generator and thus influencing the analog performance of the whole device.

2.5 Operational Amplifier

The operational amplifier has a class AB output stage and is designed to have both low noise and high slew rate performance.

In the next two figures some characteristics of the operational amplifier in an inverter circuit with a gain of one and resistors of 10k are shown.

Figure 2.8 shows a THD+N versus frequency measurement of one of the operational amplifiers at +5.0 volts.

The THD+N performance at 1kHz versus input voltage is shown in Figure 2.9.

It can be seen that the operational amplifier's signal to noise ratio is about 100dB and it can handle maximum signal levels of about $1.2V_{rms}$.

3. APPLICATION BOARD

The application board is designed and optimized for 44.1kHz sampling frequency (e.g., CD application). Due to cost reasons the PCB is designed as a single-layer board.

On this PCB only conventional components are used. Using SMD components will reduce the board size but could be critical for components in the audio signal path.

In Figures 3.1 and 3.2 the circuit diagram of this PCB is given. Figure 3.1 shows mainly the external components of the SAA7323 to achieve the best possible performance, while Figure 3.2 contains a system clock buffer and the control switches (MUTE – mute function, ATT – attenuation (12dB) and DEEM – deemphasis switch) with pull-up resistors.

Some of the shown components are optional. The notch-filter configuration at the output (components L3, C40, C41 [right channel] and L4, C42, C43 [left channel]) can be omitted if the specification for the stopband attenuation in the application is not higher than 70dB.

Furthermore, the analog supplies (Vddal, Vddar and Vddref) can be tied together and decoupled by only one resistor/capacitor supply filter. This will reduce the analog performance slightly, but all figures will be still within the specification.

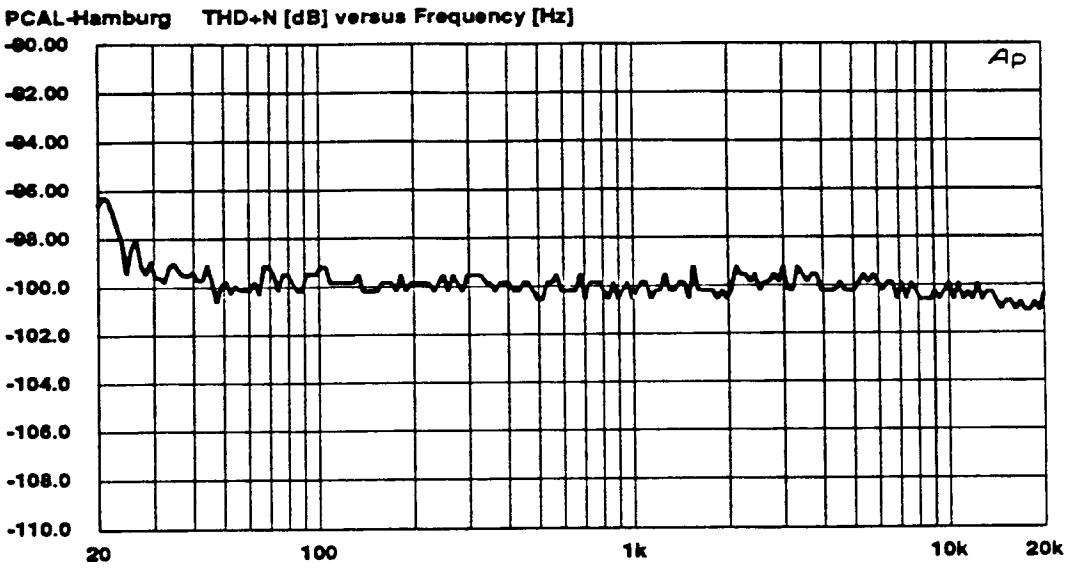

Figure 2.8: THD+N versus Frequency with $1.0V_{rms}$

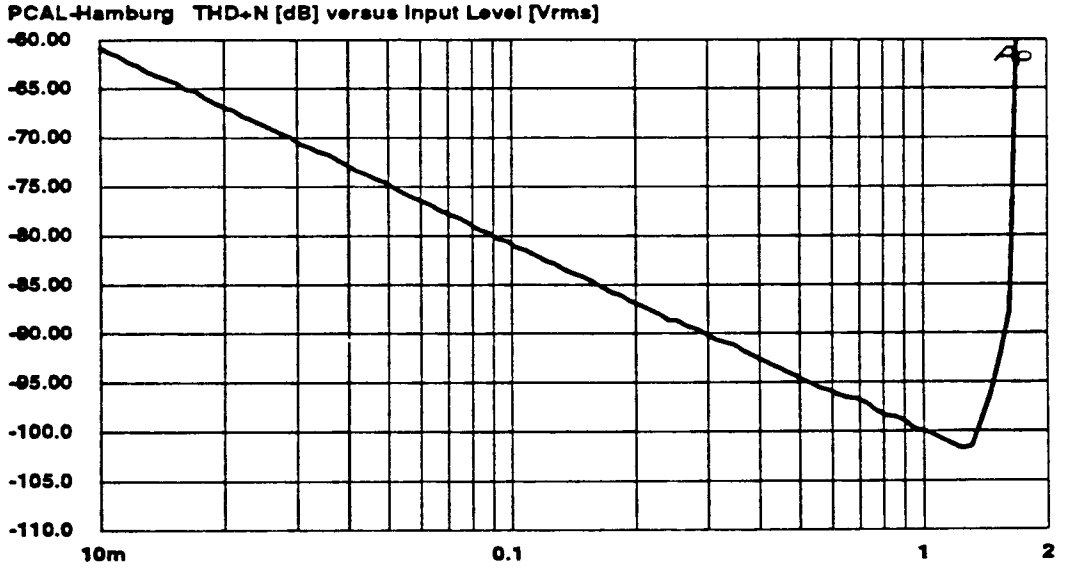

Figure 2.9: THD+N versus Input Level at +5.0V

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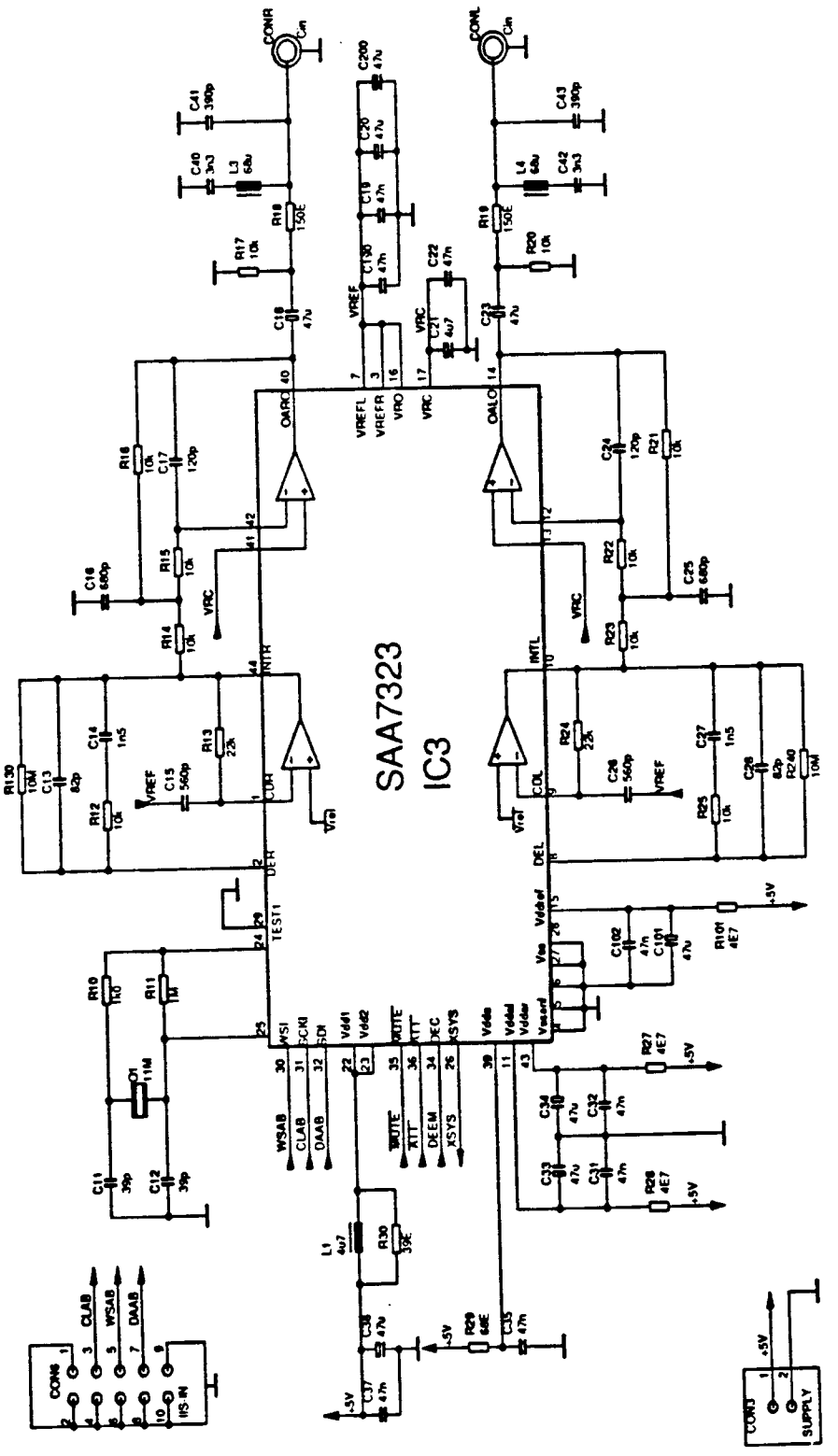

Figure 3.1: SAA7323 Circuit Diagram (Part 1)

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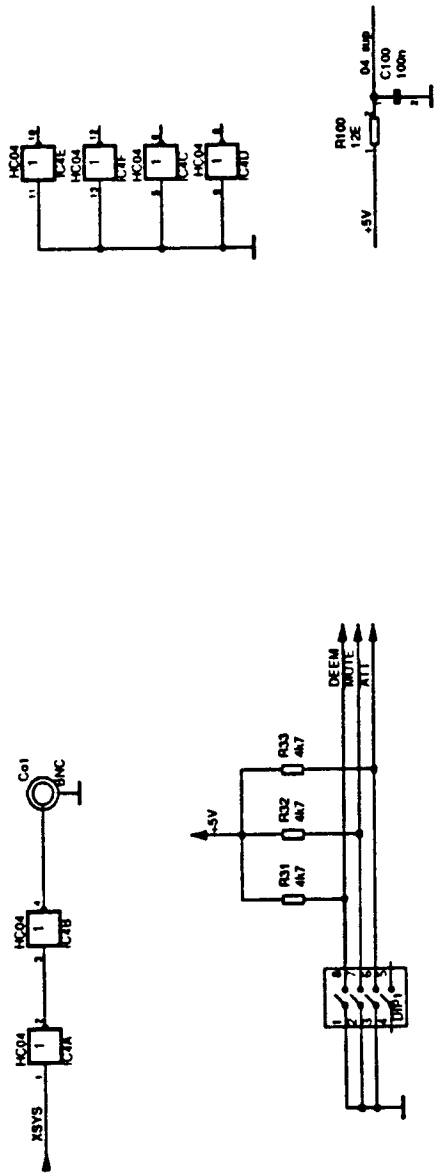

Figure 3.2: SAA7323 Circuit Diagram (Part 2)

3.1 Layout Description

Figure 3.3 shows the layout of the application board. The placement diagram can be seen in Figure 3.4.

A more detailed drawing of the critical layout part is given in Figure 3.5.

At the Vrefl and Vrefr pins the voltage for the switched capacitor network is supplied from the output of the reference generator.

Charging currents of the internal capacitors have to be smoothed as good as possible. Therefore the ceramic capacitors C19/C190 are placed close to the pins of the IC.

To prevent slew-rate distortion and overload at the differential input stage of the first operational amplifier the capacitors C15 and C26 are needed. Due to the high frequency current pulses (e.g., 11.28MHz) at the inverting input of the op-amp ceramic capacitors should be used and placed close to the IC.

The electrolytic capacitors C20/C200 clean the reference voltage line from any low-frequency noise and prevent crosstalk between the audio channels.

Instead of the fully symmetrical layout the capacitors C190/C200 can be omitted with only a slight drop in audio performance.

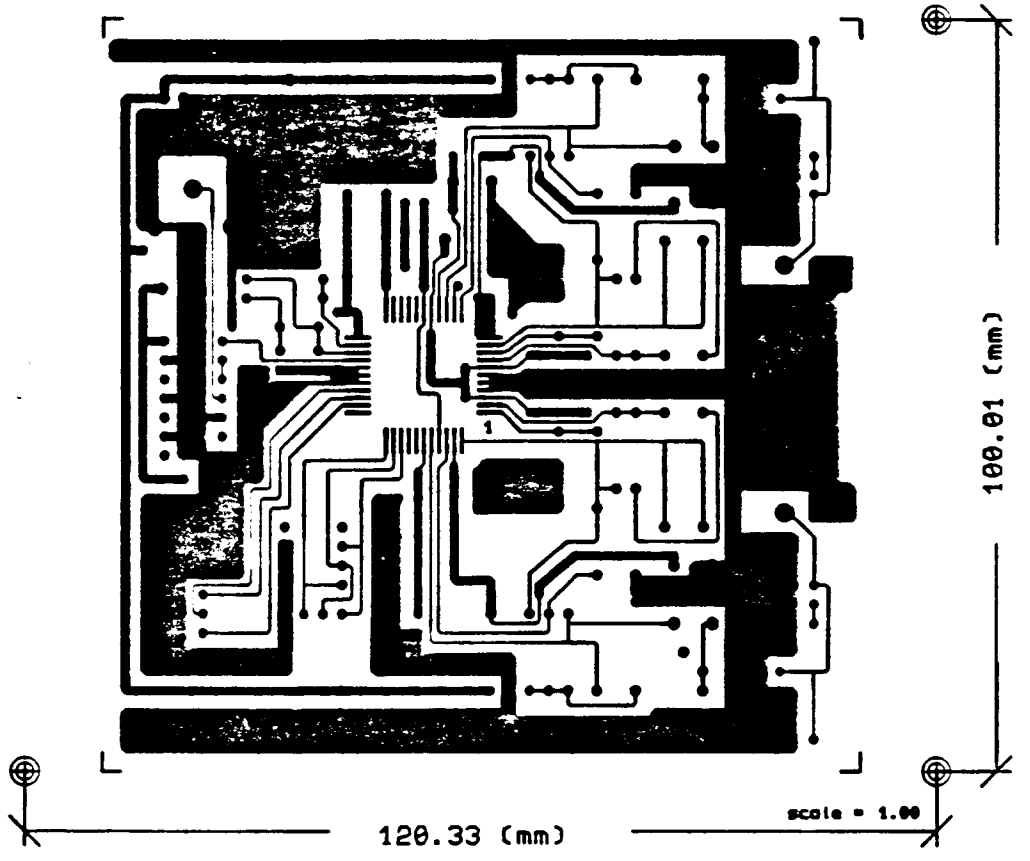

Figure 3.3: Layout of the PCB

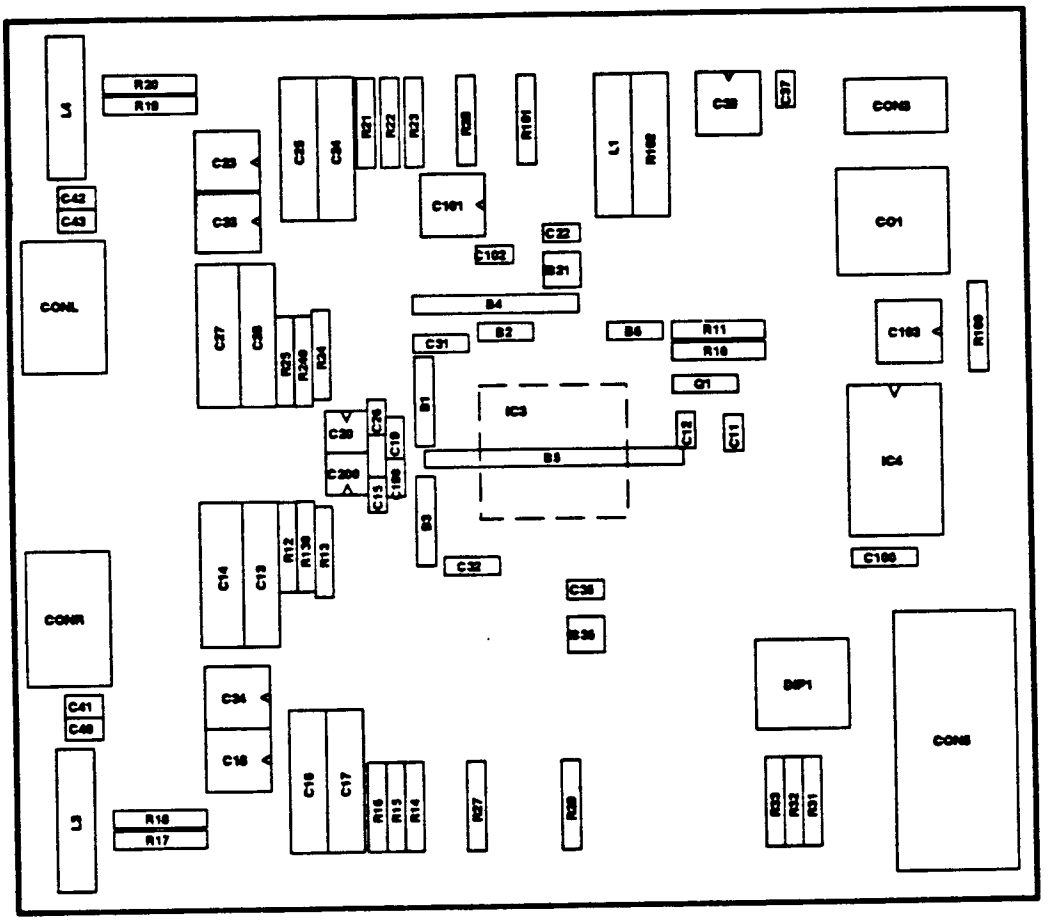

Figure 3.4: Placement Diagram

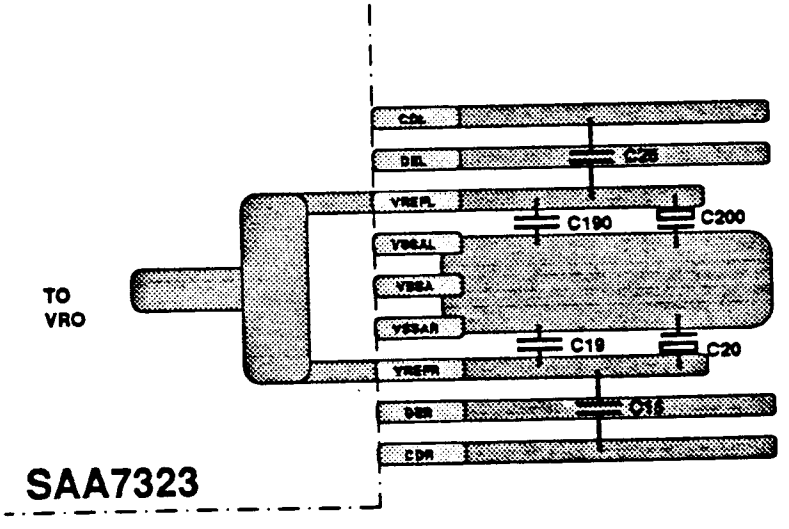

Figure 3.5: Critical Part of the Layout

3.2 Calculation of Output Voltage

All components around the first operational amplifier stage are determined by the application (e.g., sampling frequency fs) itself.

The output current of the switched-capacitor network can be calculated with the formula below.

$$V_{out(rms)} = V_{ref} * R * C_{SC} * f_{CLK} * A * \frac{1}{\sqrt{2}}$$

V_{ref}: 2.5V (nom. $V_{DD}/2$)
R: feedback resistor
C_{SC}: SC network capacitor (2.7pF)
f_{CLK}: system clock frequency
A: down scaling in digital filter (-2dB = 0.79)

Because of the single +5V supply of the SAA7323 the operational amplifier can handle up to $1.2V_{rms}$ without an essential drop of performance (see Figure 2.9). With 20% headroom for the output level, due to capacitor tolerances, the feedback resistor should be calculated for an output voltage of about $1.0V_{rms}$.

Table 10. Feedback Resistors and Output Voltage versus Sampling Frequency

fs [kHz]	f_{CLK} [MHz]	resistor [kΩ]	output voltage [V_{rms}]
32.0	8.19200	30.0	0.93
44.1	11.2896	22.0	0.94
48.0	12.2880	20.0	0.93

3.3 Calculation of the Analog Low-pass Filter

The low-pass filter described in this chapter is intended to be used in CD type applications (44.1kHz sampling frequency). If a 22kΩ feedback resistor for the first operational amplifier stage is chosen the first pole of the low-pass filter is fixed (a feedback capacitor of 85pF is integrated).

For the second operational amplifier stage, a second order low-pass filter should be designed which leads to a linear overall frequency response.

The digital filter provides a compensation for the roll-off of the $(\sin x/x)^2$ function of the linear interpolator (see section 2.2) and the analog low-pass filter of about 0.5dB at 20kHz. The roll-off of the $(\sin x/x)^2$ function can be calculated with the formula below.

$$A(f) = 20 * \log\left(\frac{\sin(\pi f/fs)}{\pi f/fs}\right)^2$$

f: signal frequency
fs: 4 times sampling frequency (176.4kHz)

At 20kHz the roll-off of the $(\sin x/x)^2$ function is

A(20kHz) = -0.37dB

Thus, 0.13dB attenuation at 20kHz is allowed for the third order low-pass filter. This is achieved with a second stage shown in Figure 3.6 below (additionally the first stage without deemphasis network is shown). The filter has a cut-off frequency of 52kHz.

Figure 3.7 shows the simulated frequency response of the whole filter up to 200kHz.

The periodic image around 176kHz (4 times the sampling frequency 44.1kHz) is suppressed by the analog filter by at least 25dB (-25dB at 152kHz). Additional attenuation of at least 32dB is caused by the linear interpolator's $(\sin x/x)^2$ roll-off.

Thus, the total suppression of the periodic image is at least 57dB which is sufficient for most applications.

The measurement results of this filter are presented in Chapter 4.3.

Before the upsampled data is fed into the noise shaper block a dither signal (-20dB, 352kHz) is added. This signal is attenuated by approximately 40dB in the analog post filter resulting in an absolute signal amplitude of about -60dB. If some more attenuation is needed an optional band-stop filter can be built up on the application board. Figure 3.8 shows this circuit. Furthermore the AC-coupling and an r.f. noise filter are shown.

Components C4 and R6 are necessary to get a DC-free output.

Figure 3.9 shows the simulated frequency response at the audio output inclusive of the third order low pass filter.

Once can see that the dip in the frequency response is at approximately 340kHz. The additional attenuation of the dither signal is about 20dB giving a total signal suppression of 80dB.

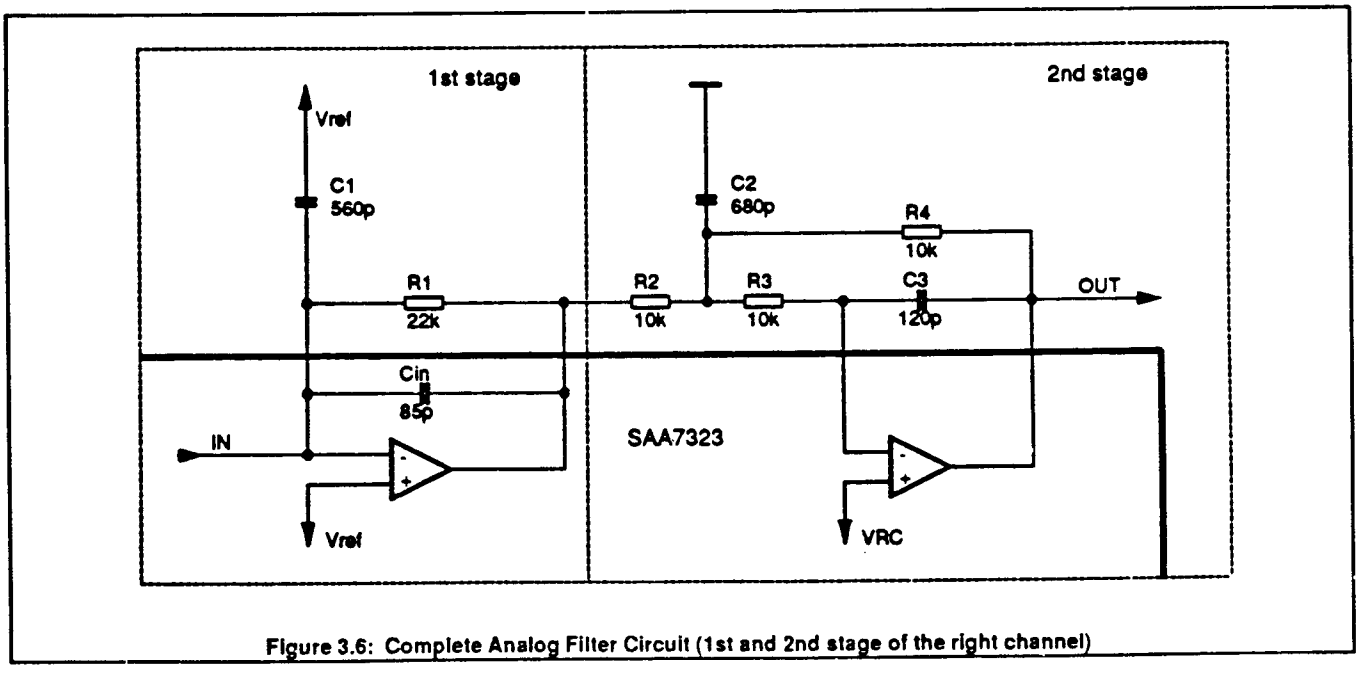

Figure 3.6: Complete Analog Filter Circuit (1st and 2nd stage of the right channel)

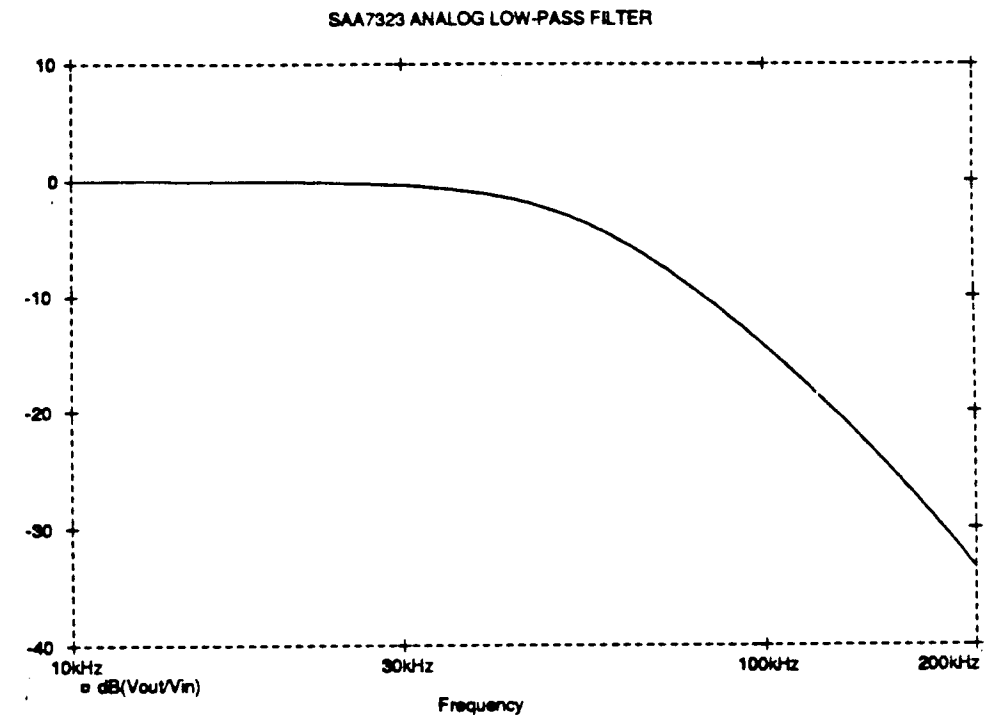

Figure 3.7: Simulated Frequency Response of the Low-pass Filter

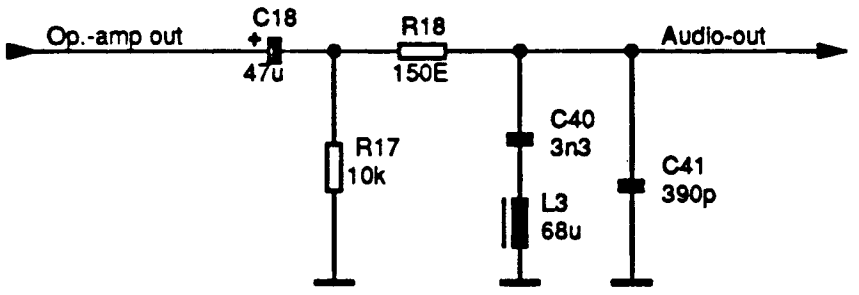

Figure 3.8: Band-Stop and R.F. Noise Filter of the Right Channel

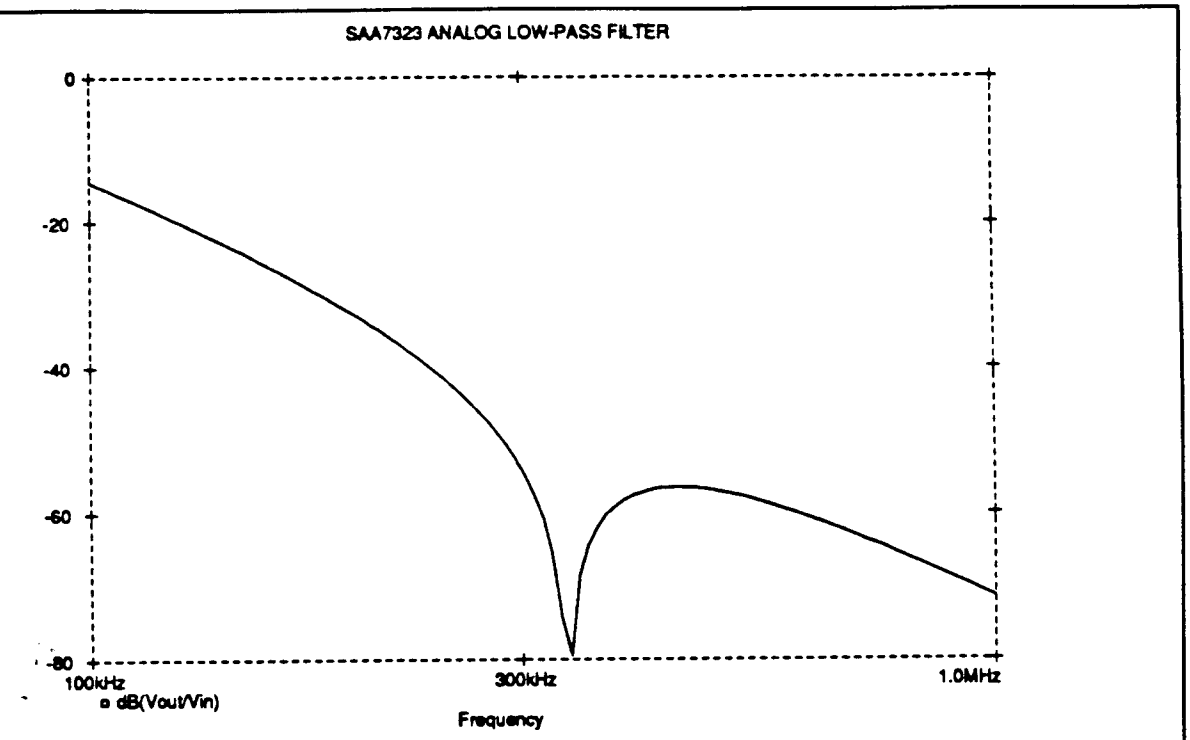

Figure 3.9: Simulated Frequency Response at Audio Output

3.4 Calculation of the Deemphasis Network

On the SAA7323 an analog switch is implemented to switch on/off a deemphasis network.

The time constants for a CD application are specified in the CD standard [5] with T_1 = 50µs and T_2 = 15µs. A plot of the preemphasis characteristic is given in Figure 3.10.

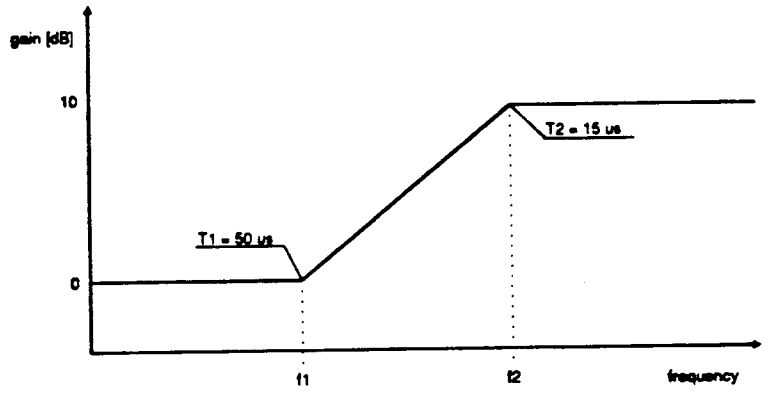

Figure 3.10: Preemphasis Characteristic

Figure 3.11 shows the complete circuitry if deemphasis is switched on.

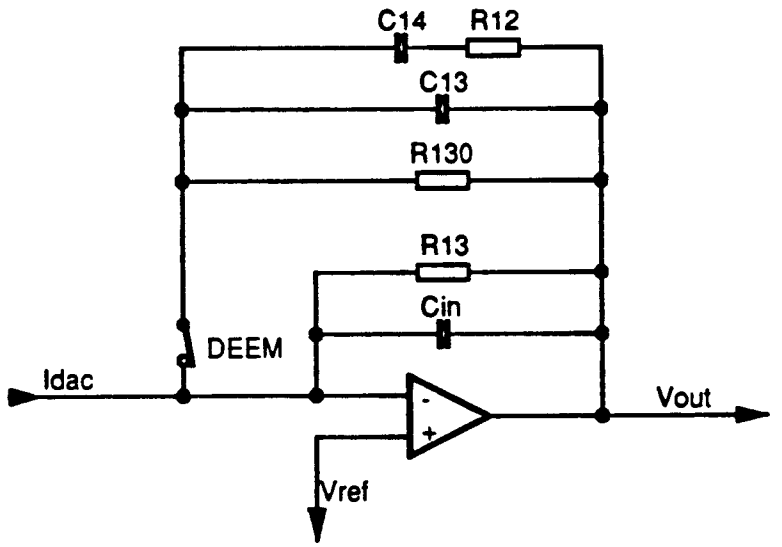

Figure 3.11: First Op-Amp Stage of SAA7323 (right channel) with Deemphasis Network

The capacitor C_{in} is integrated and its value is 85pF±20%. Capacitor C_{13} is optional but normally used to make the network insensitive to component tolerances. To prevent clicks at the audio output a high ohmic resistor R_{130} (e.g., 4.7M) is used. This resistor does not influence the frequency response and is not used in the following calculations.

The transfer function H(p) can be calculated to:

$$H(p) = \frac{1 + p\,R_{12} * C_{14}}{1 + p\,(R_{12}C_{14} + R_{13}(C_{in} + C_{14} + C_{13})) + p^2\,(R_{13}R_{12}C_{14}(C_{in} + C_{13}))}$$

This transfer function has one zero and two poles. The zero is proportional to

$$T_2 = R_{12}C_{14} \quad [3.4.1]$$

One pole is T_1 and the other belongs to the third order low pass filter. R_{13} is the feedback resistor and its value fixes the output level of the device. Recommended value for R_{13} is 22k.

The component C_{14} can be calculated with formula [3.4.1] if a value for R_{12} is chosen.

C13 can be calculated with equation [3.4.2].

$$C_{13} = -\frac{p_1 C_{14} R_{13} + T_2 p_1 + 1}{R_{13} p_1 (1 + p_h)} - C_{in} \quad [3.4.2]$$

$$\text{with } p_1 = \frac{1}{T_1}$$

Network components can be realized for R_{12} values of 10k or bigger.

To prevent distortion due to limited current drive capability the capacitive load for the operational amplifier should not exceed 200pF. More information about the calculation of the deemphasis network is given in [6].

The calculated values for the network components are:

R_{13} = 22k, C_{14} = 1n5
R_{12} = 10k, C_{13} = 51p

Measurements have shown slightly better results with C_{13} = 85p. This might be caused by differences of the calculated network to the real setup (e.g., impedance of the analog switch).

4. PERFORMANCE MEASUREMENTS

This chapter provides some more information about the performance of the SAA7323. All measurements were performed using an Audio Precision System One measurement equipment and the SAA7323 application board described before.

Signal sources were either a modified CD player with I²S interface or a digital signal generator. In combination with the CD player, test discs from CBS [7] and Philips [8], [9] were used.

The results were achieved with typical samples and should be regarded as an indication, not as a guarantee.

4.1 THD+N

Three kinds of THD+N measurements were carried out. All of these were done with an additional 20kHz brick-wall filter between audio output and analyzer. Figure 4.1 shows the THD+N results versus supply voltage.

The signal frequency for these measurements was 1kHz with a level of 0dB and -10dB referred to full scale. Both channels were driven and measured in parallel. Signal frequency and levels were chosen according to the data sheet of the SAA7323.

The THD+N performance versus signal frequency at full scale (0dB) and -60dB signal level can be seen in Figure 4.2.

The signal frequency for these measurements was 1kHz with a level of 0dB and -10dB referred to full scale. Both channels were driven and measured in parallel. Signal frequency and levels were chosen according to the data sheet of the SAA7323.

The THD+N performance versus signal frequency at full scale (0dB) and -60dB signal level can be seen in Figure 4.2.

The performance at full scale is always better than -90dB except for the small 5kHz peak. Around this frequency a slightly increased third harmonic can be detected which is only present at full scale levels. At -60dB signal level the THD+N performance is about -35dB which results in a dynamic range of 95dB. This is about constant over the whole frequency range.

The third kind of THD+N measurement was carried out with 1kHz signal frequency and over the input level range from 0dB down to -60dB. Figure 4.3 shows the result of this measurement. Please note that the THD result is always referred to full scale. Therefore it is possible to interpret the absolute value of the THD+N figures as the dynamic range of the SAA7323 for the different input levels.

This plot shows again that the performance is nearly constant. Around full scale levels a small amount of distortion can be seen. But below -10dB signal level the dynamic range in both channels is about 95dB.

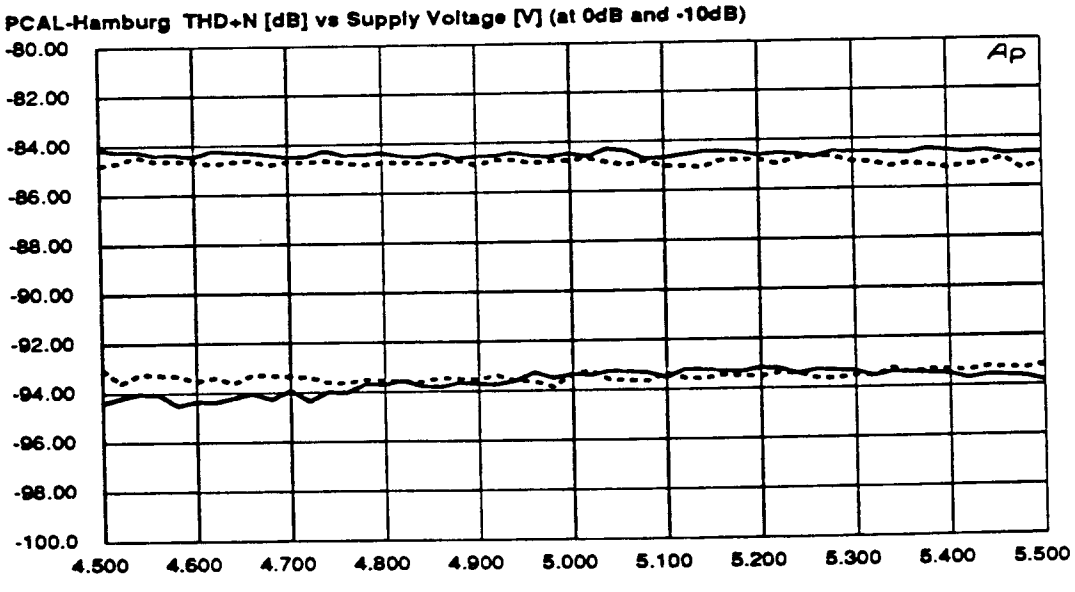

Figure 4.1: THD+N versus Supply Voltage (solid line – right channel, dashed line – left channel)

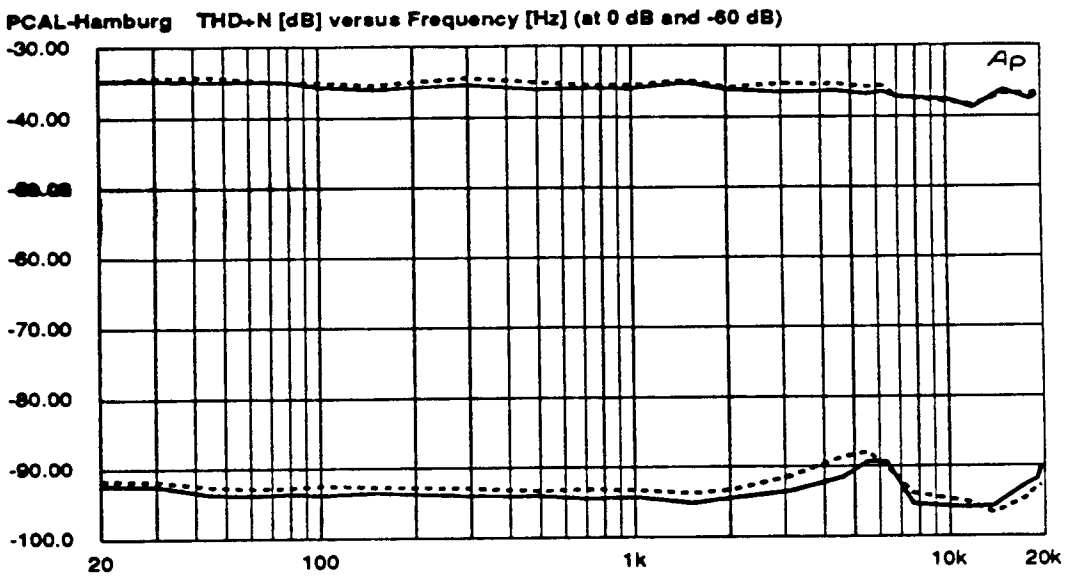

Figure 4.2: THD+N versus Frequency (solid line – right channel, dashed line – left channel)

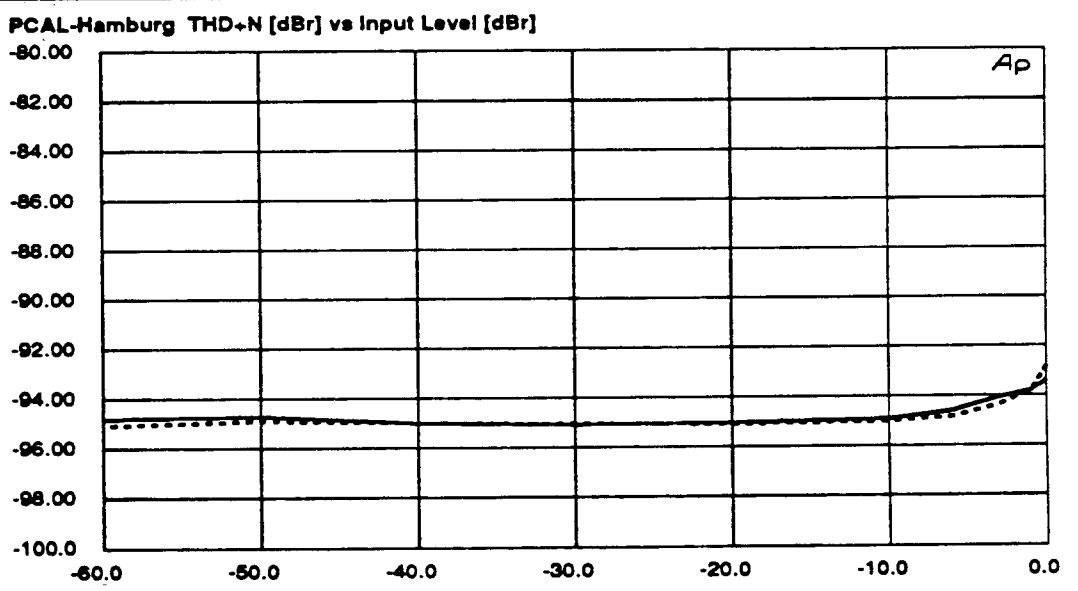

Figure 4.3: Dynamic Range versus Input Level (solid line – right channel, dashed line – left channel)

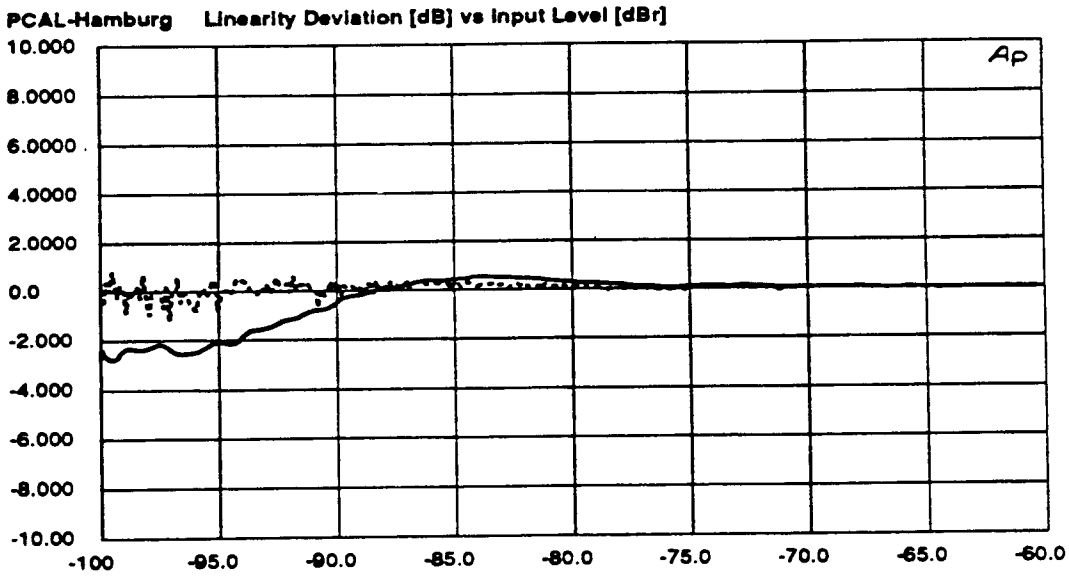

Figure 4.4: Linearity Deviation versus Input Level (solid line – right channel, dashed line – left channel)

4.2 Linearity

In this case linearity does mean a measurement of actual output versus input amplitudes. The deviation of linearity at low amplitudes is sometimes specified as the differential nonlinearity of a converter.

To measure this performance of the SAA7323 a 400Hz dithered signal is swept down from -60dB to -100dB. Theory about dithered signals and low signal amplitudes is presented in [10] and [11].

Figure 4.4 shows the deviation from perfect linearity of the SAA7323.

One can see that the linearity deviation down to signal amplitudes of -90dB is within 1dB.

4.3 Frequency Response

The frequency response in the audio range up to 20kHz is shown in Figure 4.5. For this measurement the deemphasis network was switched off.

Both channels show exactly the same performance, that's why two scales are used in this plot. The left scale belongs to the solid curve, while the right belongs to the dashed curve.

To achieve an adequate plot with the deemphasis network switched on, the ideal response curve of the preemphasis is added to the measurements. This seems to be a more accurate method than the use of a recorded preemphasis frequency sweep of test discs, because these frequency sweeps are produced with analog generators and do have all their imperfections.

However, the measured response of our network is shown in Figure 4.6.

Even with the deemphasis network switched on the frequency response is flat except a small peak at 20kHz of 0.1dB.

This kind of results strongly depend on tolerances of the components used in the analog low-pass filter. In the application board resistors with 1% tolerance and foil capacitors of 2% are built in.

4.4 Crosstalk

Channel separation or crosstalk was measured over the frequency range of 41Hz to 20kHz. Signal amplitude in one channel was 0dB (full scale) while the other channel was driven with digital silence. In the channel with digital silence the fundamental of the test frequency of the other channel was measured and referred to full scale. Figure 4.7 shows the results of these measurements.

The crosstalk results are always better than -95dB and for frequencies below 10kHz better than -100dB. In lower frequency range the crosstalk performance from the left to the right channel is about 5 to 10dB better. Herefore the reason might be that the reference voltage buffer is internally connected to the Vss track of the left channel. (Notice that there is only a separate Vdd pin for the reference buffer.)

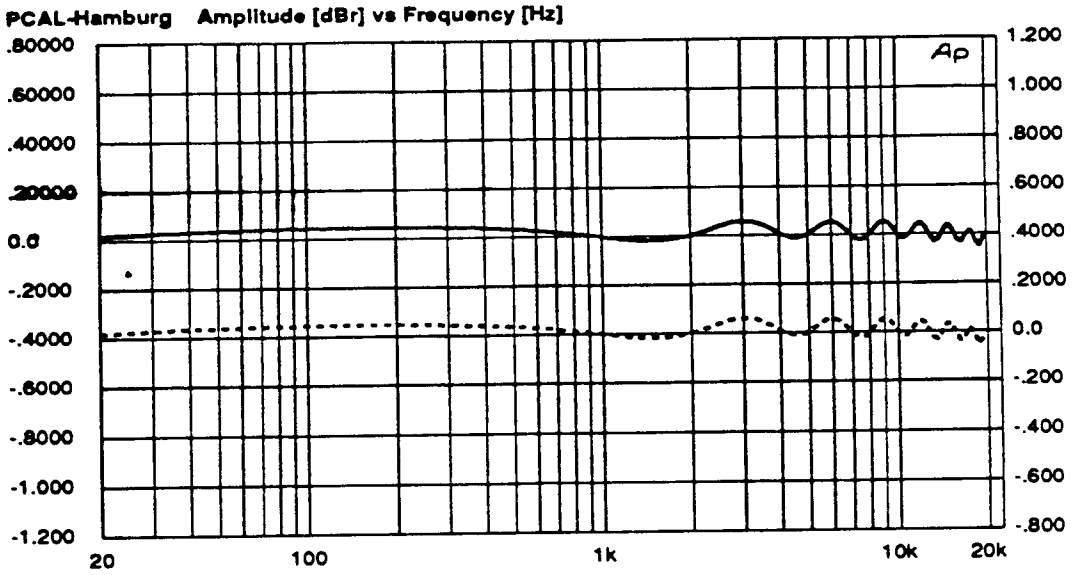

Figure 4.5: Frequency Response without Deemphasis (solid line – right channel, dashed line – left channel)

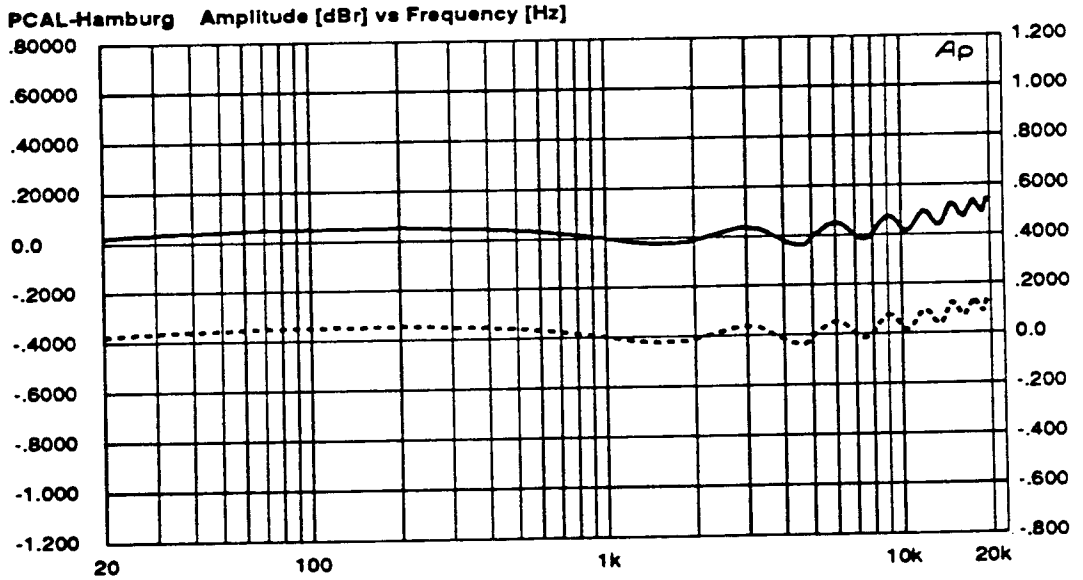

Figure 4.6: Frequency Response with Deemphasis Switched On (solid line – right channel, dashed line – left channel)

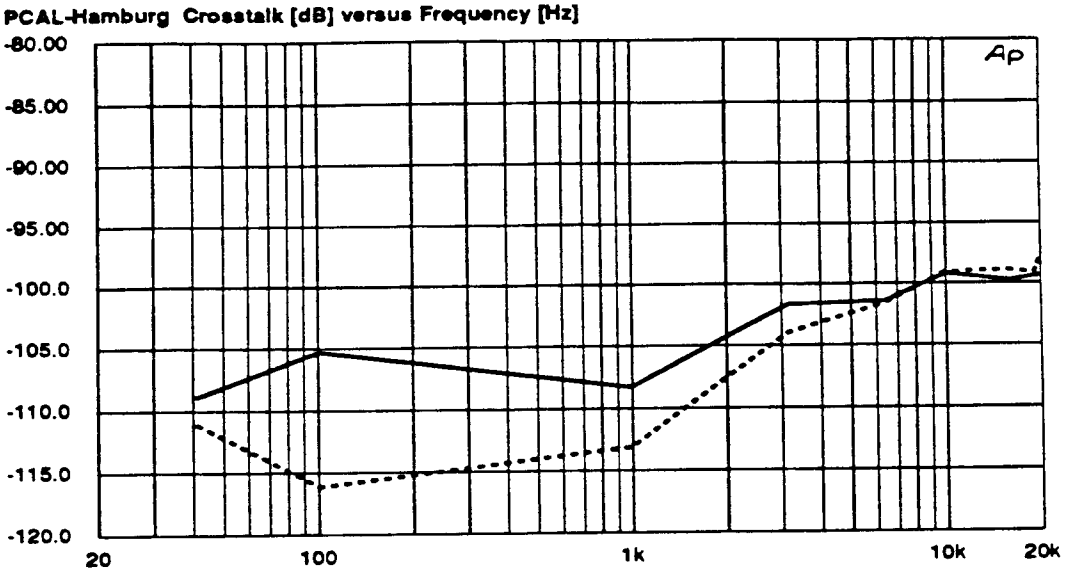

Figure 4.7: Crosstalk versus Frequency (solid line – right to left channel, dashed line – left to right)

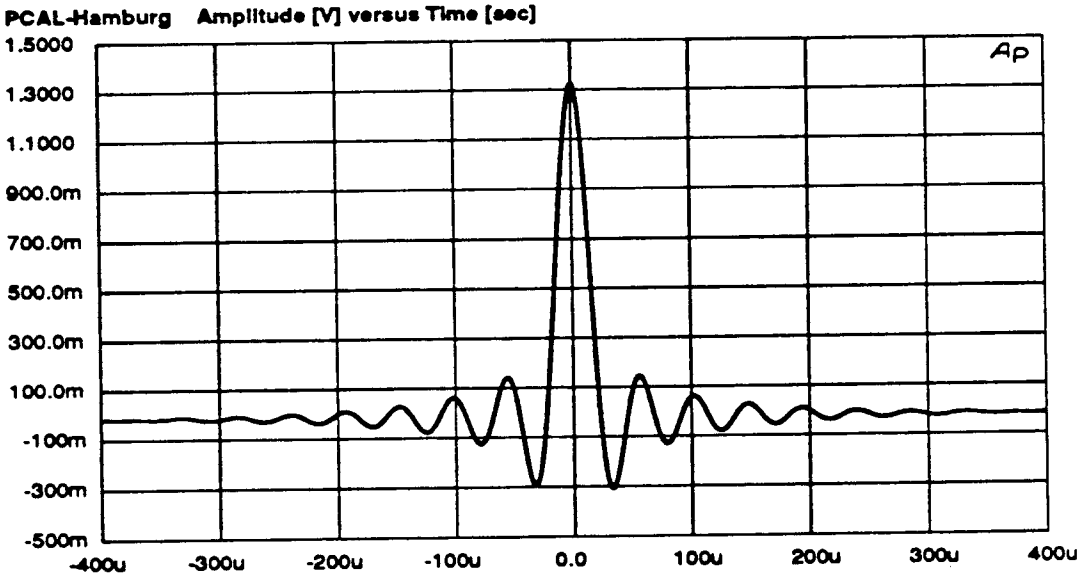

Figure 4.8: Impulse Response

4.5 Impulse Response

Two plots of the impulse behavior are presented in this chapter. Figure 4.8 shows the impulse response of a single digital full scale value.

Due to our digital FIR-filter we got a fully symmetrical response which indicates phase linearity.

With the recorded full scale square-wave, shown in Figure 4.9, it can be highlighted that the SAA7323 does not suffer from clipping effects. Again the waveform is fully symmetrical indicating a linear phase characteristic.

4.6 Signal to Noise Ratio

The signal to noise ratio (S/N) sometimes called idle channel noise is the weighted ratio of the reference signal level to the noise level when playing back a digital silence signal.

With an unweighted filter the S/N ratio is about 97dB with an 'A'-weighted filter it results in 101dB. Both measurements were done in RMS-detector mode.

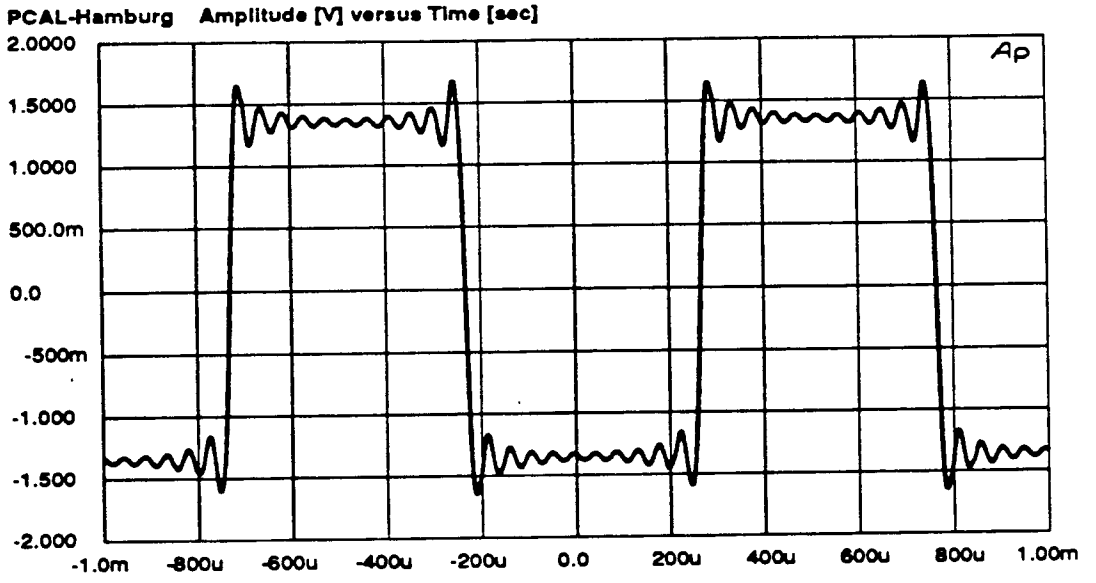

Figure 4.9: 1kHz Square Wave Response

5. APPLICATION EXAMPLES

Due to the fact that the SAA7323 can handle system clock frequencies up to 12.3MHz it can be used for all kinds of digital audio applications. Recognized sampling frequencies are 32kHz for digital satellite radio (DSR) and digital TV sound (NICAM), 44.1kHz for compact disc applications (CD) and 48kHz mainly for digital audio tape machines (DAT). The last one mentioned does include also the other sampling frequencies.

5.1 CD Application

The most common digital audio application is nowadays the compact disc application.

Figure 5.1 shows the SAA7323 in combination with the Philips CD decoder SAA7310, representing the complete signal decoding chain of the compact disc system.

Only five interconnections are required – three lines for the I²S bus, one for the deemphasis control line (DEEM) and one for the system clock. Attenuating or muting the audio output is possible with a microcontroller.

A 'high-end' CD application with an even better analog performance than presented in the previous chapters can be designed with two SAA7323 working in differential mode. One of several possibilities is shown in the block diagram in Figure 5.2.

In this application an external oscillator is required to drive all three ICs. Furthermore, some logic devices have to generate two different I²S buses, one only for the left channel and one only for the right channel, out of the one from the SAA7310. The intention is to have the inverted and non-inverted data of one channel on one I²S bus. This is provided by the LOGIC (e.g., with a few shift registers).

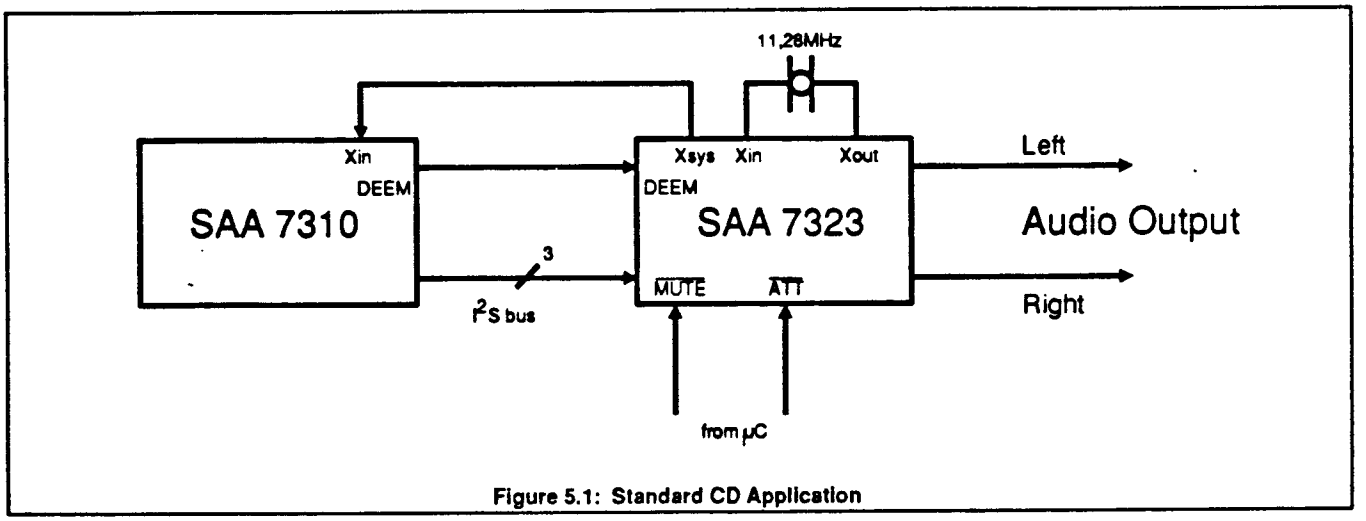

Figure 5.1: Standard CD Application

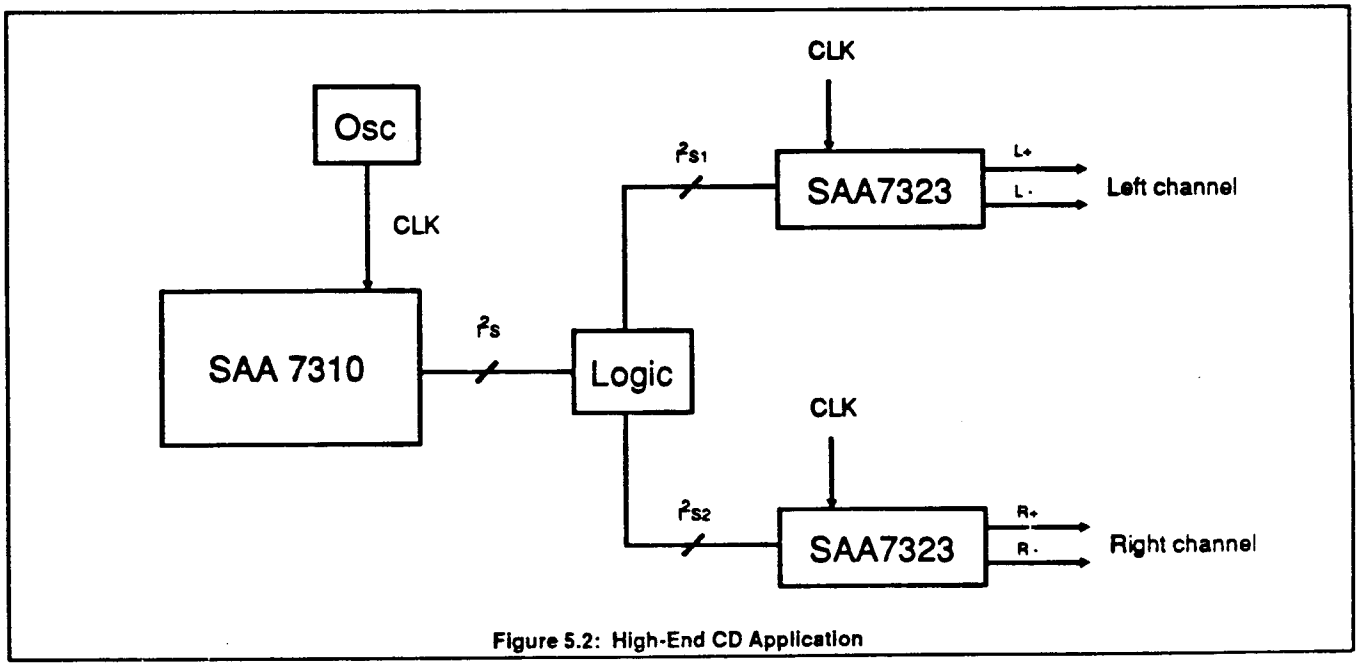

Figure 5.2: High-End CD Application

5.2 NICAM Application

NICAM 728 is a digital TV standard with 32kHz sampling frequency providing stereo sound or dual language transmissions. The application with TI's stereo demultiplexer CF70123 and the SAA7323 is shown in Figure 5.3.

With the control-line DAC_SEL the TI decoder can be switched to I^2S-output mode. Unfortunately, the MUTE control signal is active high and has to be inverted for the SAA7323. In the NICAM standard a fixed deemphasis is specified and has to be implemented in the analog filter section which has to be adapted to the 32kHz sampling frequency anyhow. Therefore the DEEM control line should be deactivated (connected to Vss).

5.3 Digital Satellite Radio Application

A digital satellite radio (DSR) application with the SAA7500 and the SAA7323 is shown in Figure 5.4. This application works again with 32kHz sample frequency. The system clock frequency in this application has to be doubled for the SAA7323 because the SAA7500 is working with only 128 times the sample frequency.

The output signals AWD, AWT and AWR have a format according to the I^2S-bus format. A modification of the analog post-filter is necessary because of the 32kHz sample frequency.

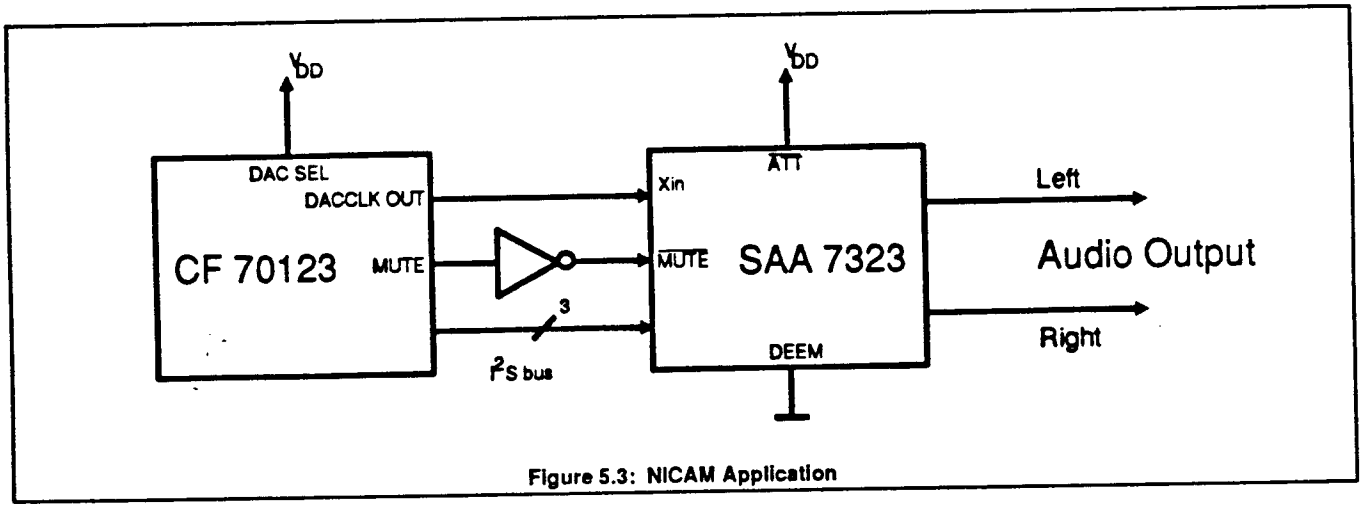

Figure 5.3: NICAM Application

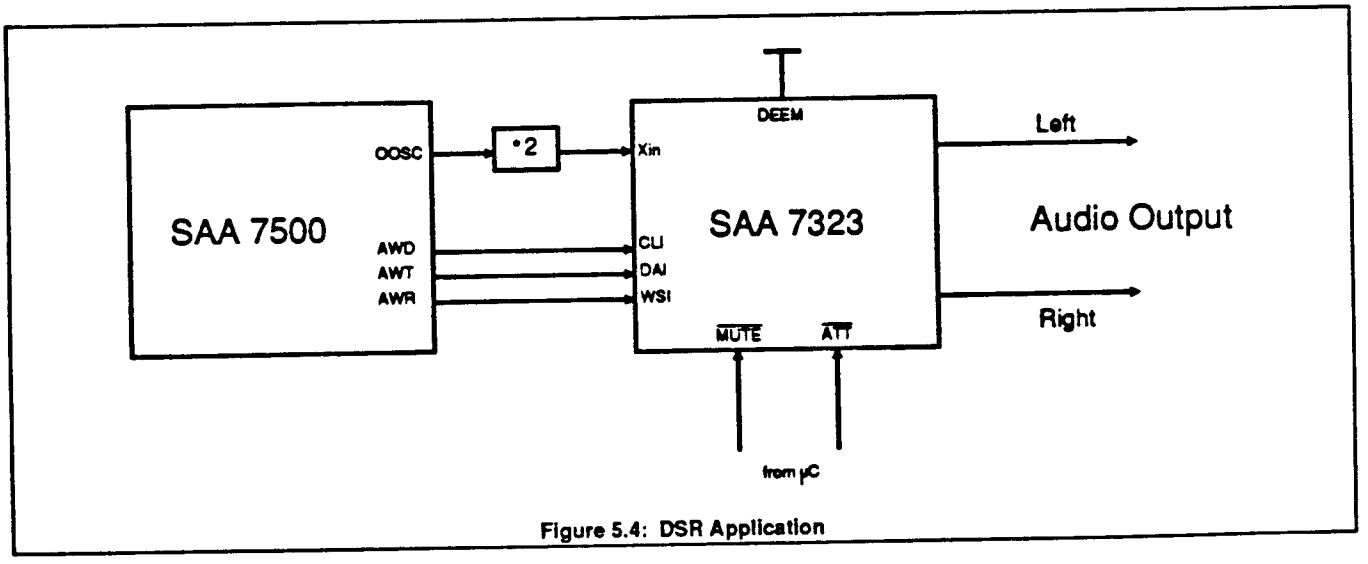

Figure 5.4: DSR Application

5.4 DAT Application

The DAT Application with the Sony decoder CXD1008 and the SAA7323 is shown in Figure 5.5. On the Sony IC the serial data output is according to the I²S-standard and the system clock is 256 times the sampling frequency.

In this kind of application the sampling frequency can be in the range of 32kHz up to 48kHz. If it is required to get a constant output voltage for all sample rates either the feedback of the first op-amp stage or the gain of an additional op-amp has to be adapted.

In case of using the 44.1kHz application described in Chapter 3 the output voltage will increase by about 1dB at 48kHz sampling frequency and decrease by about 3dB in case of 32kHz sample rate. On the other hand the frequency response will not be that as flat as shown in Chapter 4.

5.5 DSP Application

A basic application with the SAA7323 and the DSP PCF5020/A is shown in Figure 5.6.

The DSP is a pre-programmed digital signal processor which can perform either as a 7-band equalizer or a room simulator or as a scratch suppressor. More information is available in [13].

The system clock can be either generated in the SAA7323 (as shown in Figure 5.6) or in the PCF5020/A.

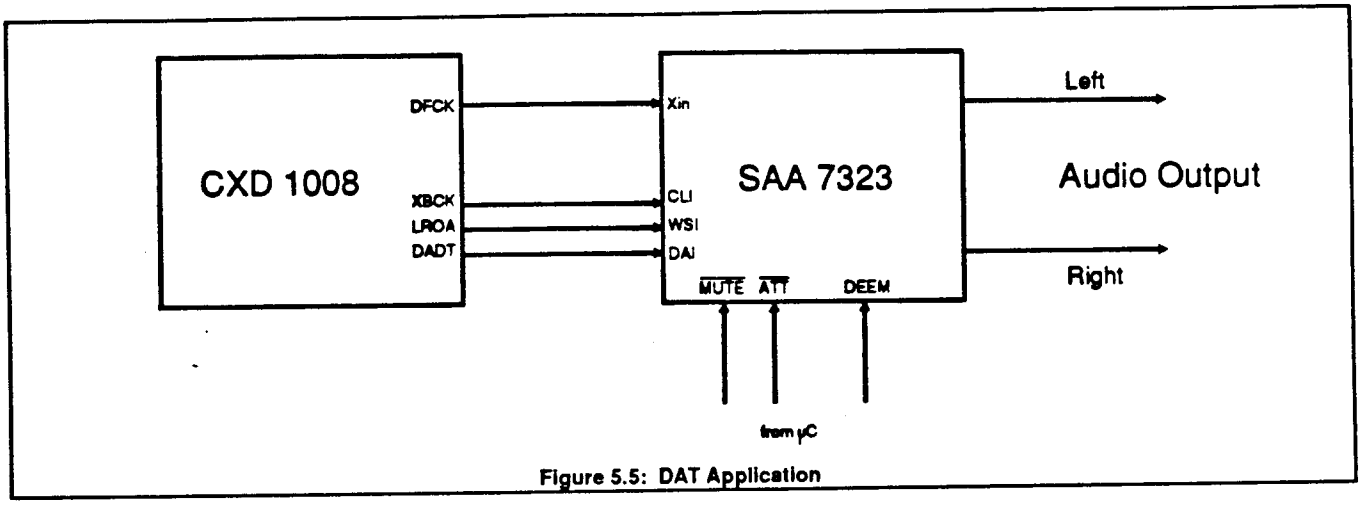

Figure 5.5: DAT Application

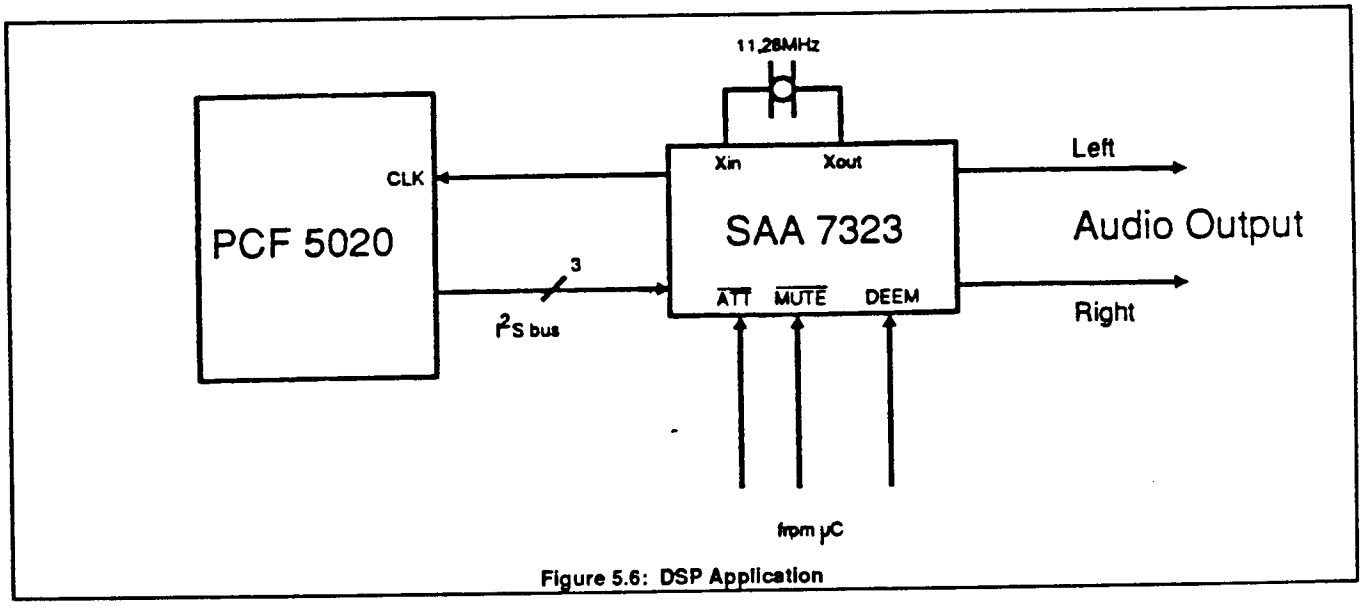

Figure 5.6: DSP Application

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