HN624116 Series

16M (1M x 16-bit) and (2M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN624116 is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 16-bit and 2,097,152 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

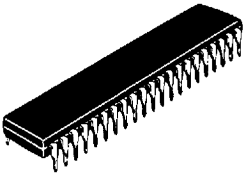
Hitachi's HN624116 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP and 48-lead Plastic TSOP packages. The HN624116 is also packaged in a 48-lead Plastic SOP.

■ FEATURES

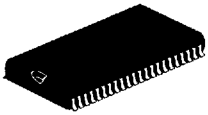
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  150 ns/200 ns (max)
- Low Power Consumption:
  Active Current: 275 mW (typ)
  Standby Current: 5 μW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  48-lead Plastic SOP
  48-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

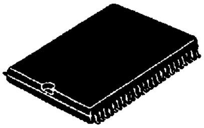
Type No.	Access Time	Package
HN624116P	150 ns 200 ns	42-pin Plastic DIP (DP-42)
HN624116FB	150 ns 200 ns	44-lead Plastic SOP (FP-44D)
HN624116F	150 ns 200 ns	48-lead Plastic SOP (FP-48DA)
HN624116TA	150 ns 200 ns	48-lead Plastic TSOP (TTP-48D)



(DP-42)



(FP-44D)

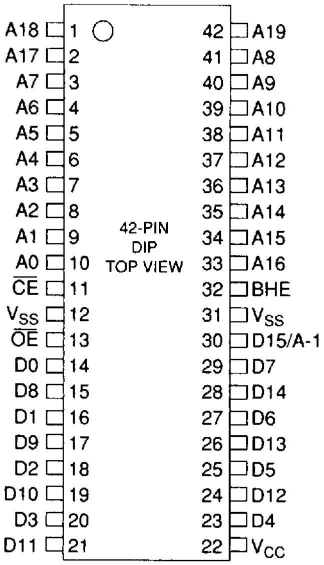


(FP-48DA)

(TTP-48D)

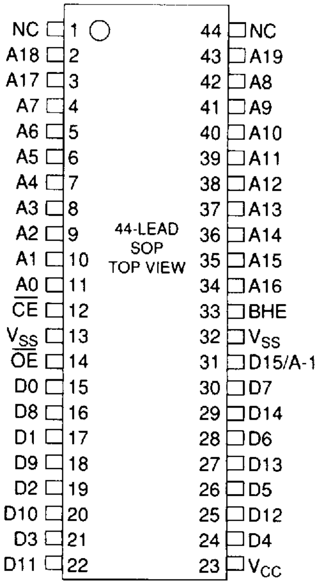
■ PIN ARRANGEMENT

HN624116P Series



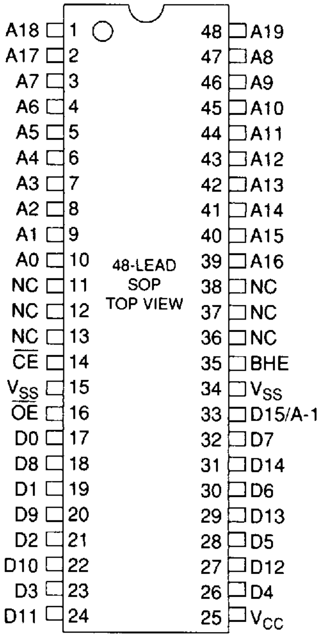
(PinD42.HN624116)

HN624116FB Series



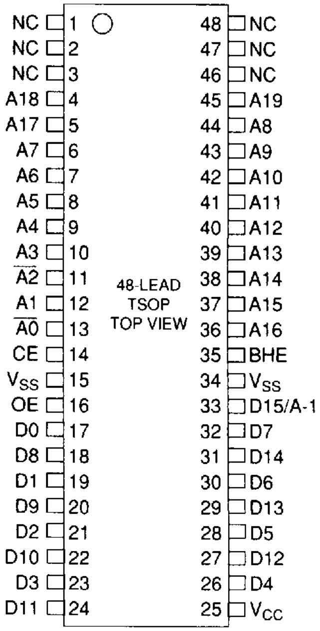
(PinT244.HN624116)

HN624116F Series



(PinT248.HN624116)

HN624116TA Series

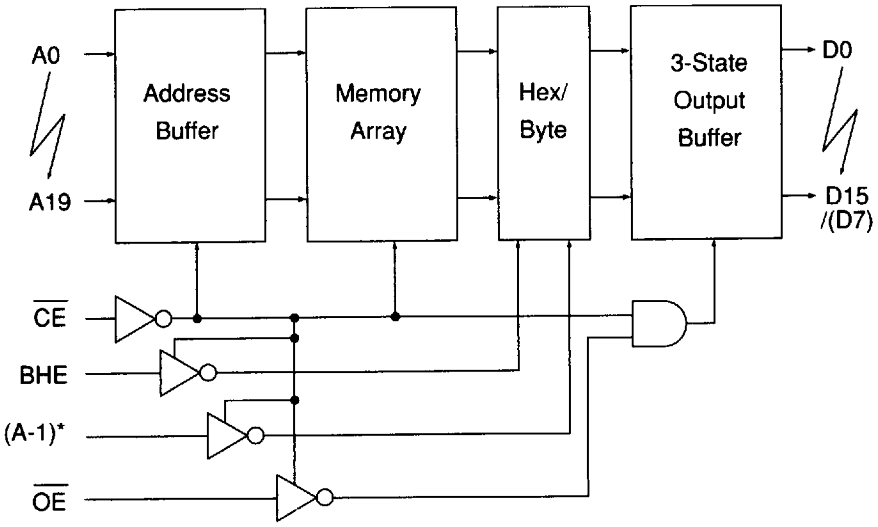


(PinT248.HN624116)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN624116)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_{IN}, V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance [1]	C_{IN}	-	-	15	pF	V_{IN} = 0V
Output Capacitance [1]	C_{OUT}	-	-	15	pF	V_{OUT} = 0V

Notes: 1. This parameter is sampledand not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	75	mA	V_{CC} = 5.5 V, I_{DOUT}=0 mA, t_{RC}=150ns
		-	-	65	mA	V_{CC} = 5.5 V, I_{DOUT}=0 mA, t_{RC}=200ns
Standby V_{CC} Current	I_{SB}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

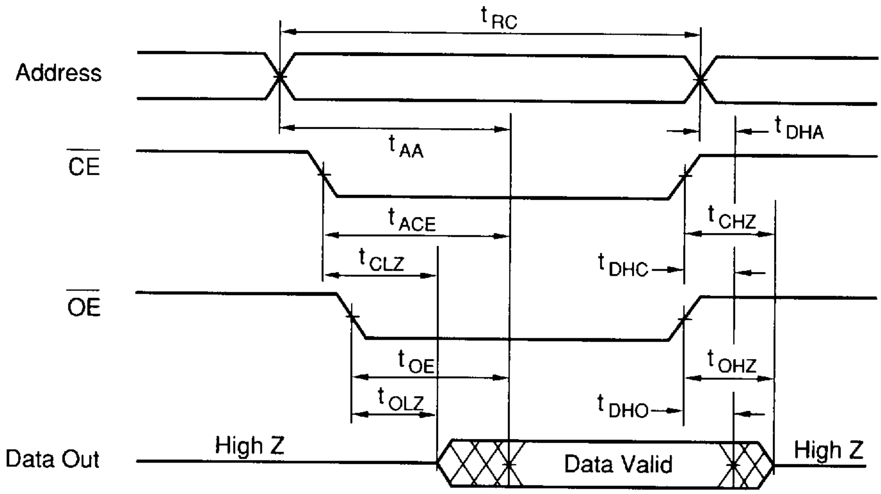
• Input pulse levels:	0.8 V / 2.4 V
• Input rise and fall times:	≤10 ns
• Output load:	1 TTL Gate + CL = 100 pF (Including jig capacitance)
• Reference level for measuring timing:	1.5 V

Item	Symbol	HN624116-15		HN624116-20		Test Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	150	-	200		ns
Address Access Time	t_{AA}	-	150	-	200	ns
Chip Enable Access Time	t_{CE}	-	150	-	200	ns
Output Enable Access Time	t_{OE}	-	70	-	100	ns
BHE Access Time	t_{BHE}	-	150	-	200	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	70	-	70	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	70	-	70	ns
BHE to Output in High-Z [1]	t_{BHZ}	-	70	-	70	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

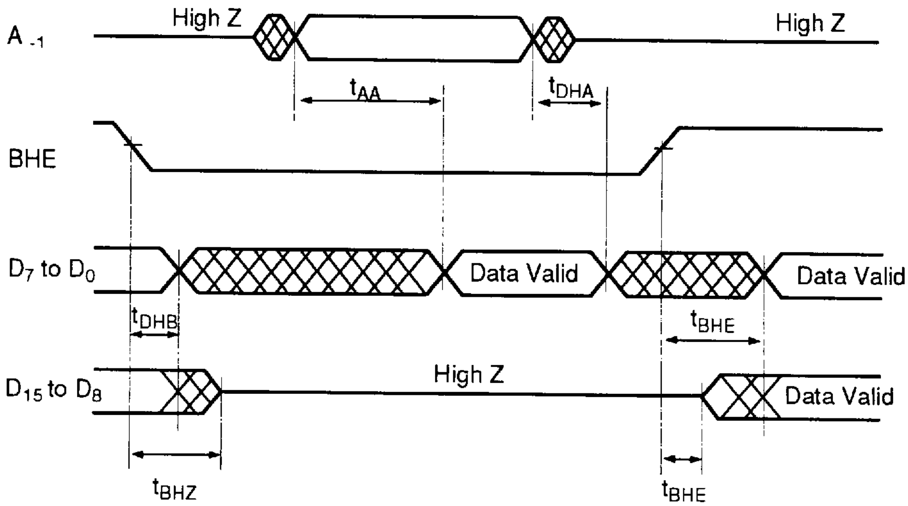
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN624116)

Note:
1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch



(TD R1.HN624116)

Note:
1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{19} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.