DRAM MODULE

MT9LD272A(X)
MT18LD472A(X)
MT36LD872A(X)

FEATURES

- JEDEC, eight CAS#, ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 16MB (2 Meg x 72), 32MB (4 Meg x 72), 64MB (8 Meg x 72)
- Nonbuffered
- State-of-the-art, high-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR), HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- Serial Presence-Detect (SPD)

OPTIONS — MARKING

- Package
  168-pin DIMM (gold) — G
- Timing
  50ns access — -5**
  60ns access — -6
- Access Cycle
  FAST PAGE MODE — Blank
  EDO PAGE MODE — X

**EDO version only

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

FPM Operating Mode

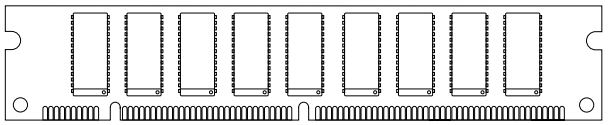
SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(DE-11) 2 Meg x 72 (shown)
(DE-12) 4 Meg x 72, (DE-24) 8 Meg x 72



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2#	86	DQ32	128	RFU
3	DQ1	45	RAS2#	87	DQ33	129	NC/RAS3#*
4	DQ2	46	CAS2#	88	DQ34	130	CAS6#
5	DQ3	47	CAS3#	89	DQ35	131	CAS7#
6	Vcc	48	WE2#	90	Vcc	132	RFU
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	RFU	104	DQ47	146	RFU
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0#	69	DQ24	111	RFU	153	DQ56
28	CAS0#	70	DQ25	112	CAS4#	154	DQ57
29	CAS1#	71	DQ26	113	CAS5#	155	DQ58
30	RAS0#	72	DQ27	114	NC/RAS1#*	156	DQ59
31	OE0#	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC (A11)	164	NC
39	NC (A12)	81	NC	123	NC (A13)	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	RFU	167	SA2
42	RFU	84	Vcc	126	RFU	168	Vcc

* 64MB version only

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	VERSION
MT9LD272AG-xx X	2 Meg x 72 ECC	Nonbuffered
MT18LD472AG-xx X	4 Meg x 72 ECC	Nonbuffered
MT36LD872AG-xx X	8 Meg x 72 ECC	Nonbuffered

xx = speed

FPM Operating Mode

PART NUMBER	CONFIGURATION	VERSION
MT9LD272AG-xx	2 Meg x 72 ECC	Nonbuffered
MT18LD472AG-xx	4 Meg x 72 ECC	Nonbuffered
MT36LD872AG-xx	8 Meg x 72 ECC	Nonbuffered

xx = speed

GENERAL DESCRIPTION

The MT9LD272A(X), MT18LD472A(X) and MT36LD872A(X) are randomly accessed 16MB, 32MB and 64MB solid-state memories organized in a x72 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 21/22 address bits, which are entered 11 bits (A0-A10) at RAS# time and 10/11 bits (A0-A10) at CAS# time.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO PAGE MODE DRAMs operate like FAST PAGE MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also High-Z the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Reference the MT4LC4M4E8 DRAM data sheet for additional information on EDO functionality.)

REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (A0-A9/A10) are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

SERIAL PRESENCE-DETECT OPERATION

This module family incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the serial PD device into standby power mode.

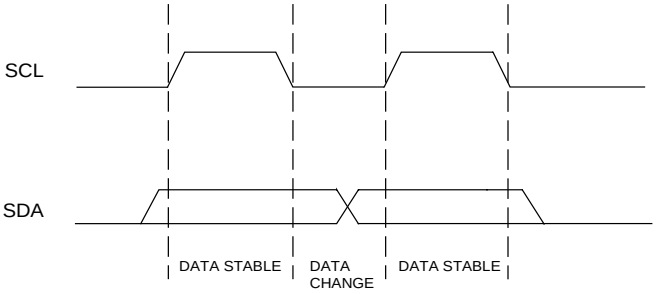


Figure 1
DATA VALIDITY

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

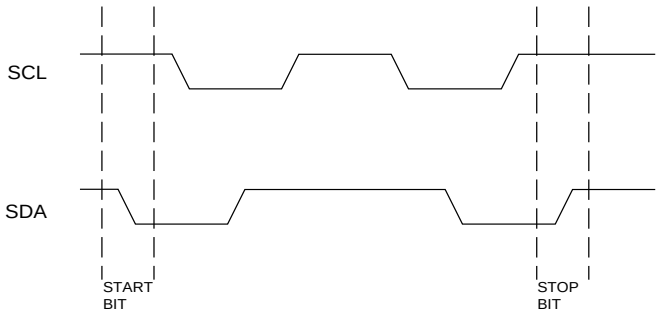


Figure 2
DEFINITION OF START AND STOP

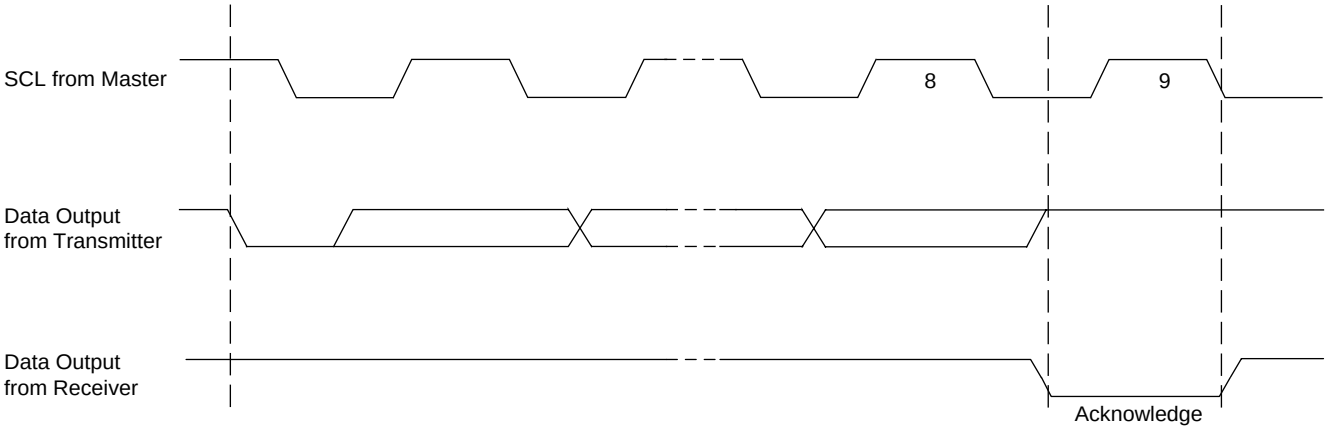
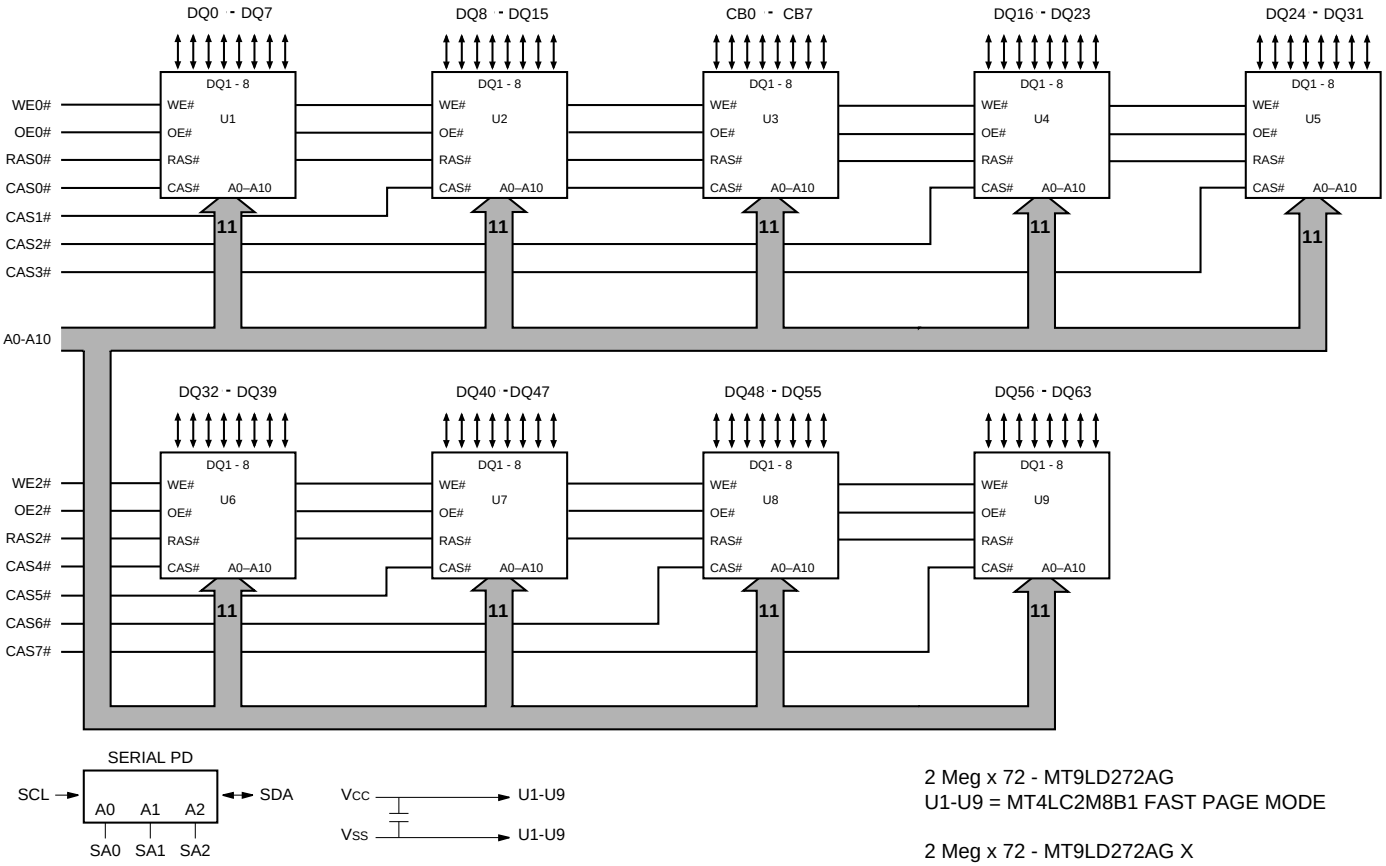


Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

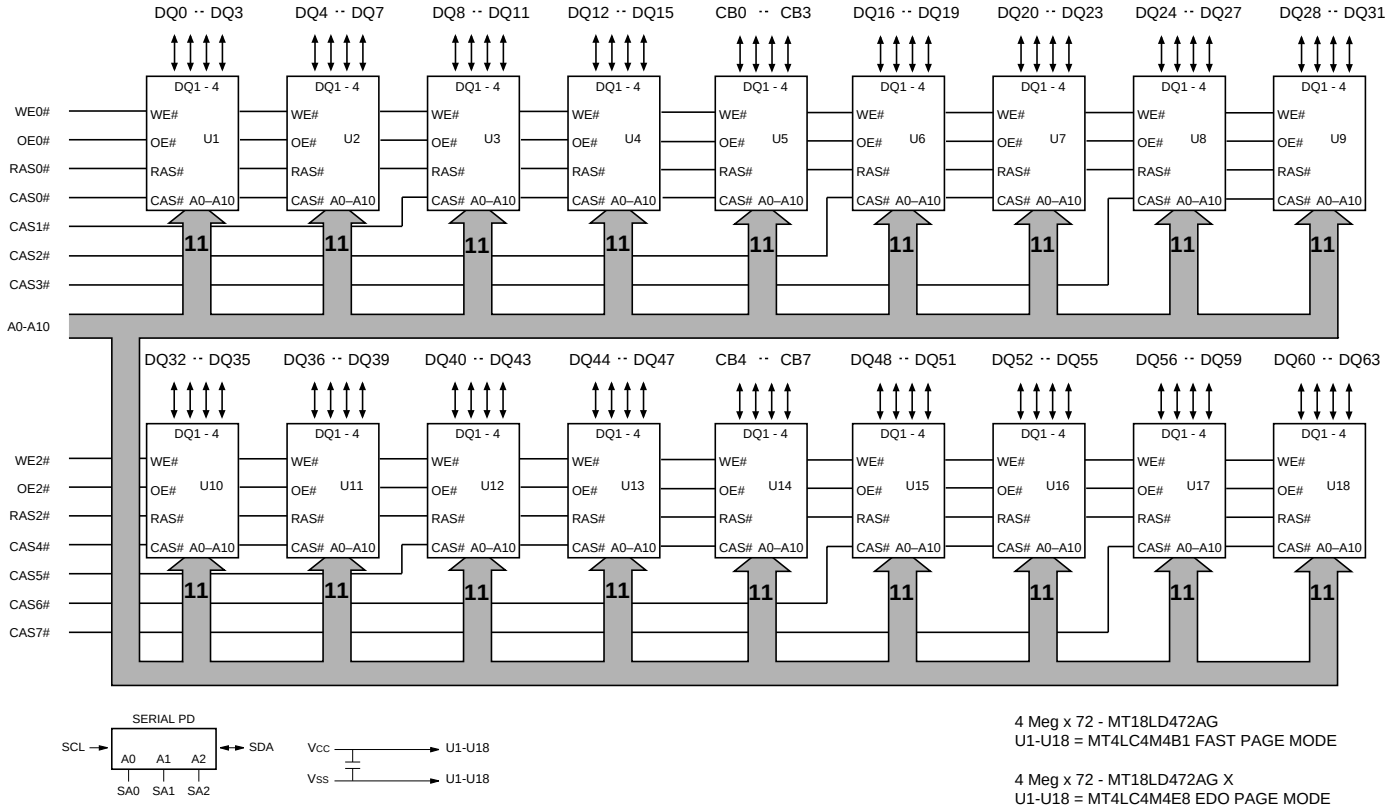
FUNCTIONAL BLOCK DIAGRAM
MT9LD272A(X) (16MB)



2 Meg x 72 - MT9LD272AG
U1-U9 = MT4LC2M8B1 FAST PAGE MODE

2 Meg x 72 - MT9LD272AG X
U1-U9 = MT4LC2M8E7 EDO PAGE MODE

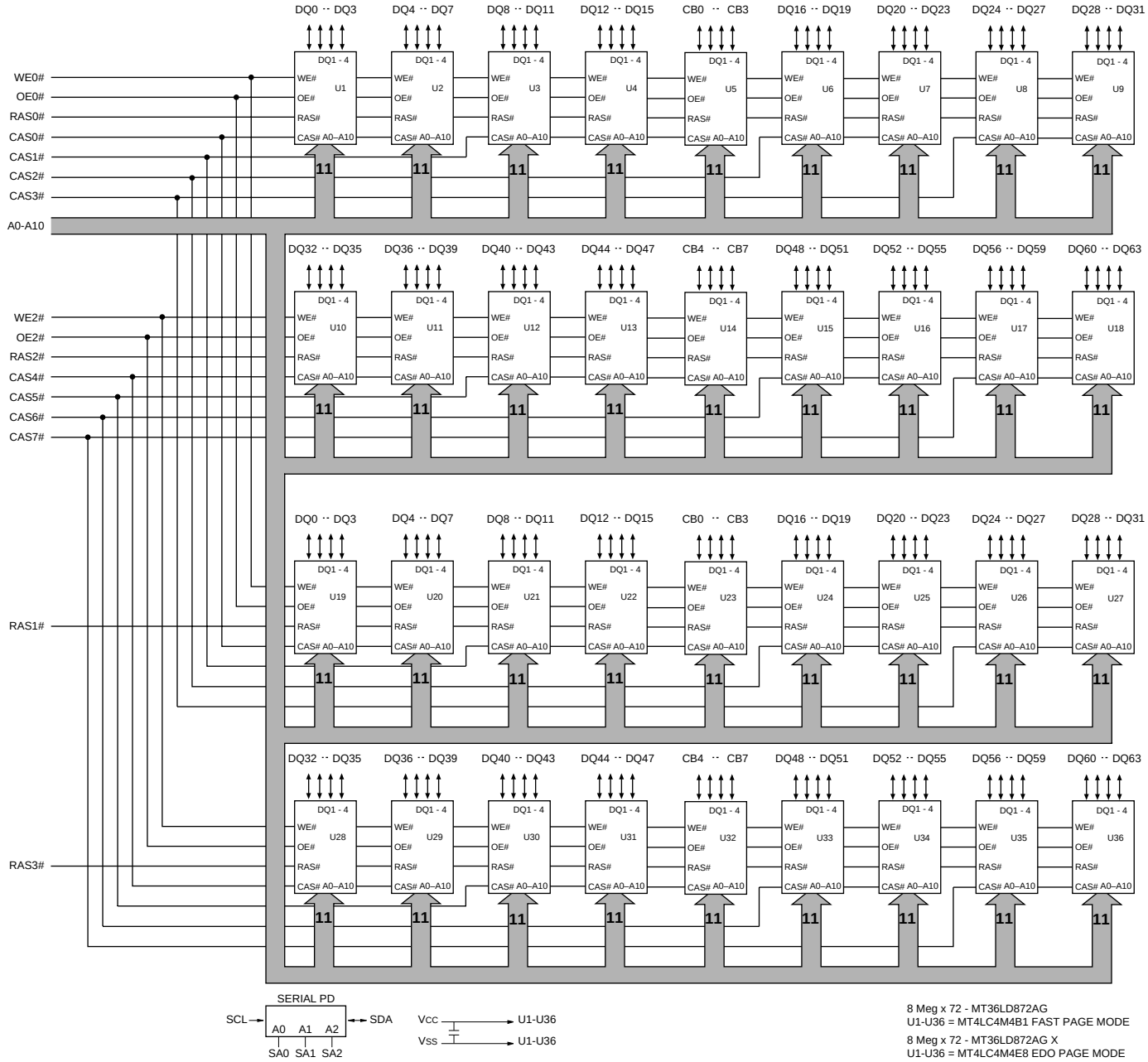
FUNCTIONAL BLOCK DIAGRAM
MT18LD472A(X) (32MB)



4 Meg x 72 - MT18LD472AG
U1-U18 = MT4LC4M4B1 FAST PAGE MODE

4 Meg x 72 - MT18LD472AG X
U1-U18 = MT4LC4M4E8 EDO PAGE MODE

FUNCTIONAL BLOCK DIAGRAM
MT36LD872A(X) (64MB)



8 Meg x 72 - MT36LD872AG
U1-U36 = MT4LC4M4B1 FAST PAGE MODE

8 Meg x 72 - MT36LD872AG X
U1-U36 = MT4LC4M4E8 EDO PAGE MODE

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45, 114, 129	RAS0#-RAS3#	Input	Row-Address Strobe: RAS# is used to clock-in the row-address bits. Two RAS# inputs allow for one x72 bank or two x36 banks.
28, 29, 46, 47, 112, 113, 130, 131	CAS0#-CAS7#	Input	Column-Address Strobe: CAS# is used to clock-in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight CAS# inputs allow byte access control for any memory bank configuration.
27, 48	WE0#, WE2#	Input	Write Enable: WE# is the READ/WRITE control for the DQ pins. If WE# is LOW prior to CAS# going LOW, the access is an EARLY WRITE cycle. If WE# is HIGH while CAS# is LOW, the access is a READ cycle, provided OE# is also LOW. If WE# goes LOW after CAS# goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0#, OE2#	Input	Output Enable: OE# is the input/output control for the DQ pins. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by RAS# and CAS#.
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89,91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
21-22, 52-53, 105-106, 136-137	CB0-CB7	Input/Output	Check Bits.
42, 62, 111, 115, 125-126, 128, 132, 146	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{CC}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V_{SS}	Supply	Ground
82	SDA	Input/Output	Serial Presence-Detect Data. SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
83	SCL	Input	Serial Clock for Presence-Detect. SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs. These pins are used to configure the presence-detect device.

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	**NUMBER OF BYTES USED BY MICRON**									
	128	1	0	0	0	0	0	0	0	80
1	**TOTAL NUMBER OF SPD MEMORY BYTES**									
	256	0	0	0	0	1	0	0	0	08
2	**MEMORY TYPE**									
	FAST PAGE MODE	0	0	0	0	0	0	0	1	01
	EDO PAGE MODE	0	0	0	0	0	0	1	0	02
3	**NUMBER OF ROW ADDRESSES**									
	11	0	0	0	0	1	0	1	1	0B
4	**NUMBER OF COLUMN ADDRESSES**									
	10 (16MB)	0	0	0	0	1	0	1	0	0A
	11 (32MB and 64MB)	0	0	0	0	1	0	1	1	0B
5	**NUMBER OF BANKS**									
	1 (16MB and 32MB)	0	0	0	0	0	0	0	1	01
	2 (64MB)	0	0	0	0	0	0	1	0	02
6	**DATA WIDTH**									
	x72	0	1	0	0	1	0	0	0	48
7	**DATA WIDTH (continued)**									
	NONE	0	0	0	0	0	0	0	0	00
8	**VOLTAGE INTERFACE**									
	LVTTL	0	0	0	0	0	0	0	1	01
9	**RAS# ACCESS TIME (^tRAC)**									
	50ns	0	0	1	1	0	0	1	0	32
	60ns	0	0	1	1	1	1	0	0	3C
10	**CAS# ACCESS TIME (^tCAC)**									
	13ns	0	0	0	0	1	1	0	1	0D
	15ns	0	0	0	0	1	1	1	1	0F
11	**MODULE CONFIGURATION TYPE**									
	ECC	0	0	0	0	0	0	1	0	02
12	**REFRESH RATES**									
	NORMAL (15.625µs)	0	0	0	0	0	0	0	0	00
13	**DRAM WIDTH (PRIMARY DRAM)**									
	x8 (16MB)	0	0	0	0	1	0	0	0	08
	x4 (32MB and 64MB)	0	0	0	0	0	1	0	0	04
14	**ERROR CHECKING DRAM DATA WIDTH**									
	x8 (16MB)	0	0	0	0	1	0	0	0	08
	x4 (32MB and 64MB)	0	0	0	0	0	1	0	0	04

NOTE: 1. “1”/“0”: Serial Data, “driven to HIGH” / “driven to LOW.”

TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	OE#	ADDRESSES		DATA-IN/OUT
						^tR	^tC	DQ0-63, CB0-CB7
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
	Any Cycle (X version)	L	L→H	H	L	n/a	n/a	Data-Out
EDO/FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS#-ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic)..... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	SIZE	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	ALL	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	ALL	2.0	V_{CC} +.3	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	ALL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} +.3V (All other pins not under test = 0V)	CAS0# - CAS7#	I_{I1}	16MB 32MB 64MB	-4 -6 -12	4 6 12	µA	
	A0-A10	I_{I2}	16MB 32MB 64MB	-18 -36 -72	18 36 72	µA	
	WE0#-WE2#, OE0#, OE2#	I_{I3}	16MB 32MB 64MB	-10 -18 -36	10 18 36	µA	
	RAS0#-RAS3#	I_{I4}	16MB 32MB 64MB	-10 -18 -18	10 18 18	µA	
OUTPUT LEAKAGE CURRENT (DQ is disabled; 0V ≤ V_{OUT} ≤ V_{CC} +.3V)	DQ0-DQ63, CB0-CB7	I_{OZ}	16MB 32MB 64MB	-5 -5 -10	5 5 10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	ALL	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}	ALL		0.4	V	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 5, 6) (V_{CC} = +3.3V ±0.3V)

			MAX			
PARAMETER/CONDITION	**SYMBOL**	**SIZE**	**-5***	**-6**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I_{CC1}	16MB 32MB 64MB	9 18 36	9 18 36	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = V_{CC} -0.2V)	I_{CC2}	16MB 32MB 64MB	4.5 9 18	4.5 9 18	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC3}	16MB 32MB 64MB	990 1,980 2,070	900 1,800 1,890	mA	3, 24
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{CC4}	16MB 32MB 64MB	- - -	720 1,440 1,530	mA	3, 24
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{CC5} (X only)	16MB 32MB 64MB	990 1,980 2,070	900 1,800 1,890	mA	3, 24
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{CC6}	16MB 32MB 64MB	990 1,980 2,070	900 1,800 1,890	mA	3, 24
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC7}	16MB 32MB 64MB	990 1,980 2,070	900 1,800 1,890	mA	3, 4

* EDO versions only

CAPACITANCE

		MAX				
PARAMETER	**SYM**	**16MB**	**32MB**	**64MB**	**UNITS**	**NOTES**
Input Capacitance: A0-A10	C_{I1}	51	96	190	pF	2
Input Capacitance: WE0#, WE2#, OE0#, OE2#	C_{I2}	39	67	132	pF	2
Input Capacitance: RAS0# - RAS3#	C_{I3}	39	67	67	pF	2
Input Capacitance: CAS0# - CAS7#	C_{I4}	17	24	41	pF	2
Input Capacitance: SCL, SA0-SA2	C_{I5}	6	6	6	pF	2
Input/Output Capacitance: DQ0-DQ63, CB0-CB7, SDA	C_{IO}	10	10	18	pF	2

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		**-6**			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column address	^tAA		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	45		ns	
Column-address setup time	^tASC	0		ns	
Row-address setup time	^tASR	0		ns	
Column-address to WE# delay time	^tAWD	55		ns	23
Access time from CAS#	^tCAC		15	ns	14
Column-address hold time	^tCAH	10		ns	
CAS# pulse width	^tCAS	15	10,000	ns	
CAS# hold time (CBR Refresh)	^tCHR	15		ns	4
CAS# to output in Low-Z	^tCLZ	3		ns	25
CAS# precharge time	^tCP	10		ns	15
Access time from CAS# precharge	^tCPA		35	ns	
CAS# to RAS# precharge time	^tCRP	5		ns	
CAS# hold time	^tCSH	60		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		ns	4
CAS# to WE# delay time	^tCWD	40		ns	23
Write command to CAS# lead time	^tCWL	15		ns	
Data-in hold time	^tDH	10		ns	22
Data-in setup time	^tDS	0		ns	22
Output disable	^tOD	3	15	ns	
Output enable	^tOE		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	15		ns	21
Output buffer turn-off delay	^tOFF	3	15	ns	19,25,26
OE# setup prior to RAS# during HIDDEN Refresh cycle	^tORD	0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		ns	

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		ns	
Access time from RAS#	^{t}RAC		60	ns	13
RAS# to column-address delay time	^{t}RAD	15		ns	17
Row-address hold time	^{t}RAH	10		ns	
RAS# pulse width	^{t}RAS	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^{t}RASP	60	125,000	ns	
Random READ or WRITE cycle time	^{t}RC	110		ns	
RAS# to CAS# delay time	^{t}RCD	20		ns	16
Read command hold time (referenced to CAS#)	^{t}RCH	0		ns	18
Read command setup time	^{t}RCS	0		ns	
Refresh period (2,048 cycles)	^{t}REF		32	ms	
RAS# precharge time	^{t}RP	40		ns	
RAS# to CAS# precharge time	^{t}RPC	0		ns	
Read command hold time (referenced to RAS#)	^{t}RRH	0		ns	18
RAS# hold time	^{t}RSH	15		ns	
READ WRITE cycle time	^{t}RWC	155		ns	
RAS# to WE# delay time	^{t}RWD	85		ns	23
Write command to RAS# lead time	^{t}RWL	15		ns	
Transition time (rise or fall)	^{t}T	2	50	ns	
Write command hold time	^{t}WCH	10		ns	
Write command hold time (referenced to RAS#)	^{t}WCR	45		ns	
WE# command setup time	^{t}WCS	0		ns	23
Write command pulse width	^{t}WP	10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	10		ns	

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column address	^tAA		25		30	ns	
Column-address setup to CAS# precharge	^tACH	12		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column-address to WE# delay time	^tAWD	42		49		ns	23
Access time from CAS#	^tCAC		13		15	ns	14
Column-address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	4
CAS# to output in Low-Z	^tCLZ	0		0		ns	
Data output hold after CAS# LOW	^tCOH	3		3		ns	
CAS# precharge time	^tCP	8		10		ns	15
Access time from CAS# precharge	^tCPA		28		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	38		45		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	4
CAS# to WE# delay time	^tCWD	28		35		ns	23
Write command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	8		10		ns	22
Data-in setup time	^tDS	0		0		ns	22
Output disable	^tOD	0	12	0	15	ns	
Output enable	^tOE		12		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10		ns	21
OE# HIGH hold time from CAS# HIGH	^tOEHC	5		10		ns	21
OE# HIGH pulse width	^tOEP	5		5		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		ns	
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	19, 26
OE# setup prior to RAS# during HIDDEN Refresh cycle	^tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	47		56		ns	
Access time from RAS#	^tRAC		50		60	ns	13
RAS# to column-address delay time	^tRAD	9		12		ns	17
Row-address hold time	^tRAH	9		10		ns	
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	^tRC	84		104		ns	
RAS# to CAS# delay time	^tRCD	11		14		ns	16
Read command hold time (referenced to CAS#)	^tRCH	0		0		ns	18
Read command setup time	^tRCS	0		0		ns	
Refresh period (2,048 cycles)	^tREF		32		32	ms	
RAS# precharge time	^tRP	30		40		ns	

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
RAS# to CAS# precharge time	^{t}RPC	5		5		ns	
Read command hold time (referenced to RAS#)	^{t}RRH	0		0		ns	18
RAS# hold time	^{t}RSH	13		15		ns	
READ WRITE cycle time	^{t}RWC	116		140		ns	
RAS# to WE# delay time	^{t}RWD	67		79		ns	23
Write command to RAS# lead time	^{t}RWL	13		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
Write command hold time	^{t}WCH	8		10		ns	
Write command hold time (referenced to RAS#)	^{t}WCR	38		45		ns	
WE# command setup time	^{t}WCS	0		0		ns	23
Output disable delay from WE# (CAS# HIGH)	^{t}WHZ	0	12	0	15	ns	
Write command pulse width	^{t}WP	5		5		ns	
WE# pulse to disable at CAS# HIGH	^{t}WPZ	10		10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	8		10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	8		10		ns	

SERIAL PRESENCE-DETECT EEPROM OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	$V_{CC} \times .7$	V_{CC} +.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	$V_{CC} \times .3$	V	
OUTPUT LOW VOLTAGE, I_{OUT} = 3mA	V_{OL}		0.4	V	
INPUT LEAKAGE CURRENT, V_{IN} = GND to V_{CC}	I_{LI}		10	µA	
OUTPUT LEAKAGE CURRENT, V_{OUT} = GND to V_{CC}	I_{LO}		10	µA	
STANDBY CURRENT SCL = SDA = V_{CC} -0.3V, All other inputs = GND or 3.3V +10%	I_{SB}		30	µA	
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I_{CC}		2	mA	

SERIAL PRESENCE-DETECT EEPROM AC ELECTRICAL CHARACTERISTICS

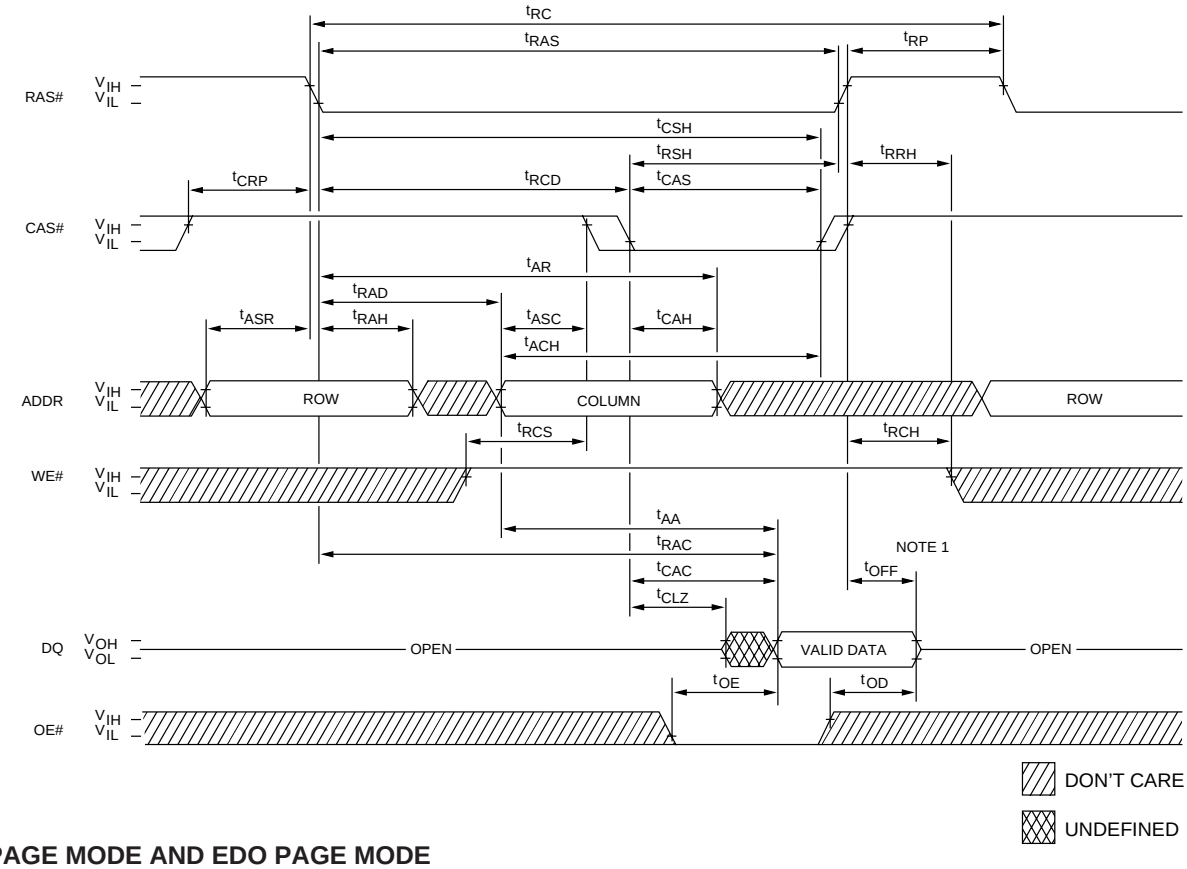
(Notes: 1) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^tBUF	4.7		µs	
Data-out hold time	^tDH	300		ns	
SDA and SCL fall time	^tF		300	ns	
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	4		µs	
Clock HIGH period	^tHIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		100	ns	
Clock LOW period	^tLOW	4.7		µs	
SDA and SCL rise time	^tR		1	µs	
SCL clock frequency	^tSCL		100	KHz	
Data-in setup time	$^tSU:DAT$	250		ns	
Start condition setup time	$^tSU:STA$	4.7		µs	
Stop condition setup time	$^tSU:STO$	4.7		µs	
WRITE cycle time	^tWR		10	ms	28

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3V; f = 1 MHz.
3. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns for FAST PAGE MODE and 2.5ns for EDO PAGE MODE.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2V.
13. Requires that ^{t}AA and ^{t}RAC are not violated.
14. Requires that ^{t}AA and ^{t}CAC are not violated.
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
16. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD (MAX) limit, ^{t}AA and ^{t}CAC must always be met.
17. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
18. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
19. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after ^{t}OEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
22. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}WCS < ^{t}WSC (MIN) and ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
24. Column address changed once each cycle.
25. The 3ns minimum parameter guaranteed by design.
26. For FAST PAGE MODE option, ^{t}OFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the RAS# and CAS# signal to transition HIGH.
27. Applies to both EDO and FAST PAGE MODE modules.
28. The SPD EEPROM WRITE cycle time (^{t}WR) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase / program cycle. During the WRITE cycle, the EEPROM bus interface circuit are disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
29. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.

READ CYCLE [27]



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

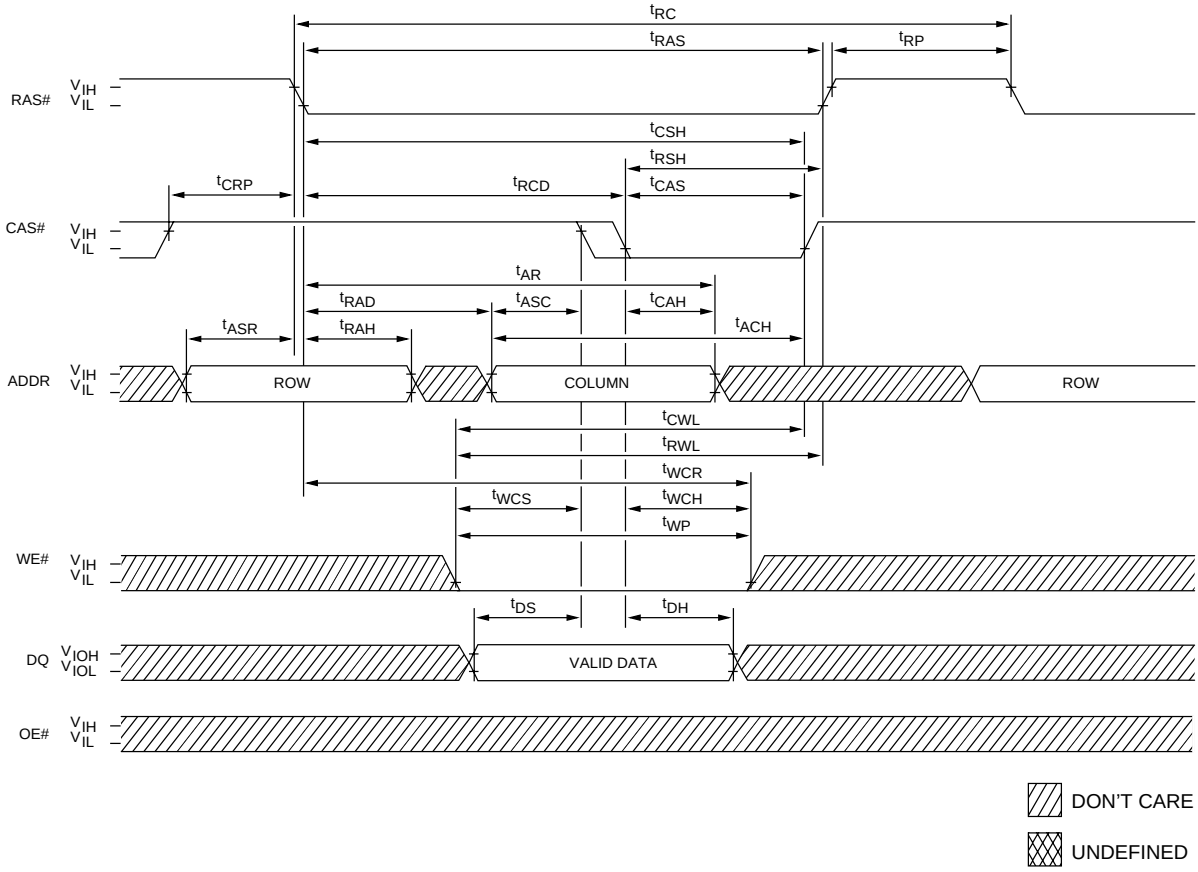
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		25		30	ns
tACH (EDO)	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	—	—	15	10,000	ns
tCLZ (EDO)	0		0		ns
tCLZ (FPM)	—		3		ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	—		60		ns
tOD (EDO)	0	12	0	15	ns
tOD (FPM)	—	—	3	15	ns
tOE		12		15	ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOFF (EDO)	0	12	0	15	ns
tOFF (FPM)	—	—	3	15	ns
tRAC		50		60	ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	—		15		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (EDO)	84		104		ns
tRC (FPM)	—		110		ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	—		20		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

*EDO version only

NOTE: 1. For EDO, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last. For FPM, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs first.

EARLY WRITE CYCLE [27]



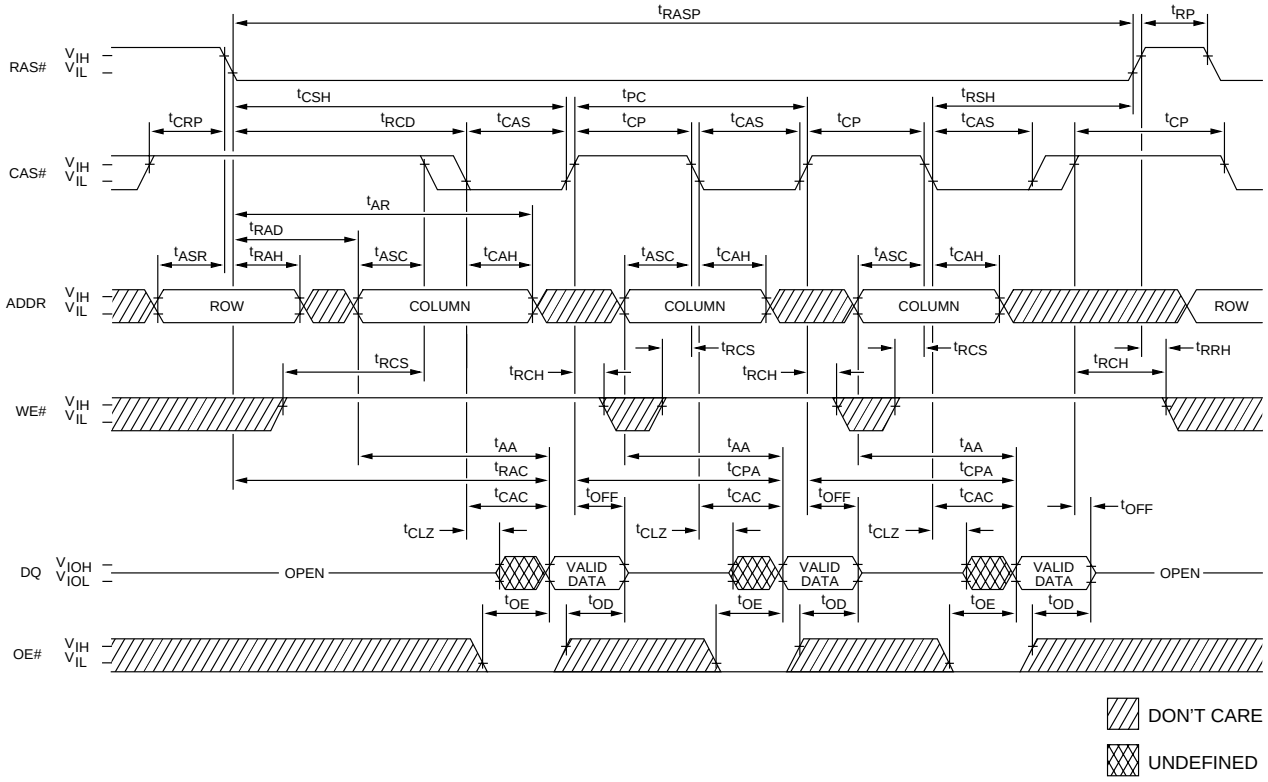
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tACH (EDO)	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS (FPM)	—	—	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCRP	5		5		ns
tCSH (FPM)	—		60		ns
tCSH (EDO)	38		45		ns
tCWL (FPM)	—		15		ns
tCWL (EDO)	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tRAD (FPM)	—		15		ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tRAD (EDO)	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	—		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	—		20		ns
tRCD (EDO)	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP (FPM)	—		10		ns
tWP (EDO)	5		5		ns

*EDO version only

FAST-PAGE-MODE READ CYCLE

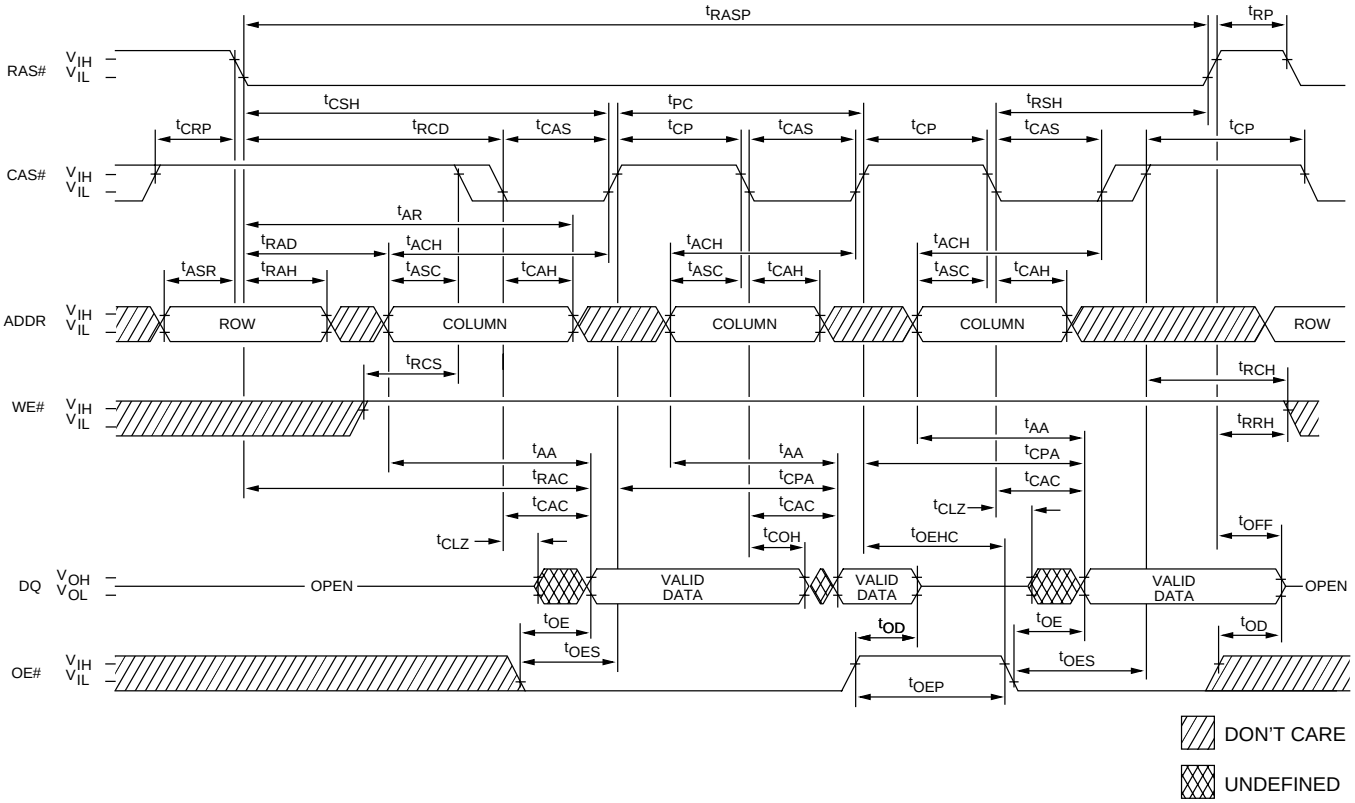


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCPA		35	ns
tCRP	5		ns
tCSH	60		ns
tOD	3	15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOE		15	ns
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

EDO-PAGE-MODE READ CYCLE

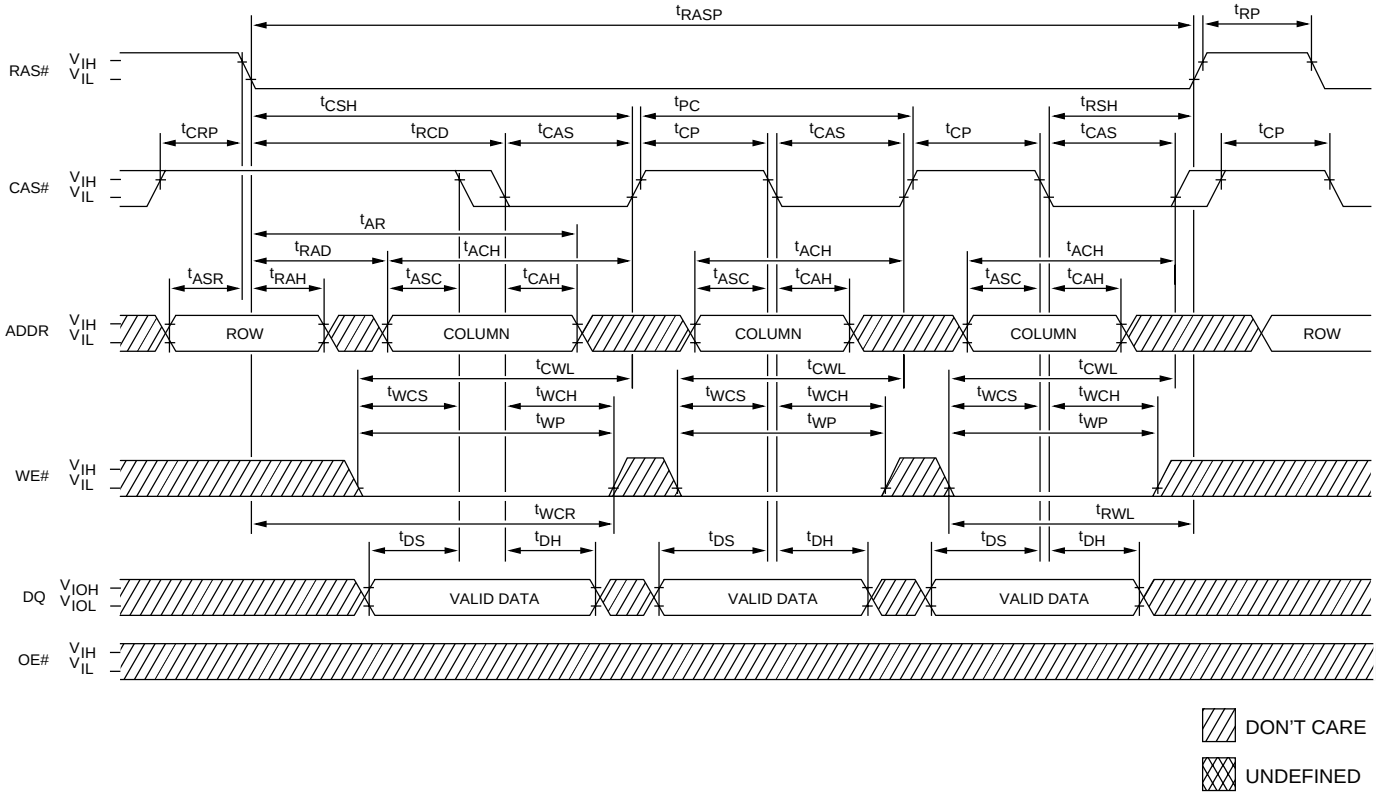


EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOEHC	5		10		ns
tOEP	5		5		ns
tOES	4		5		ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

FAST/EDO-PAGE-MODE EARLY-WRITE CYCLE [27]



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

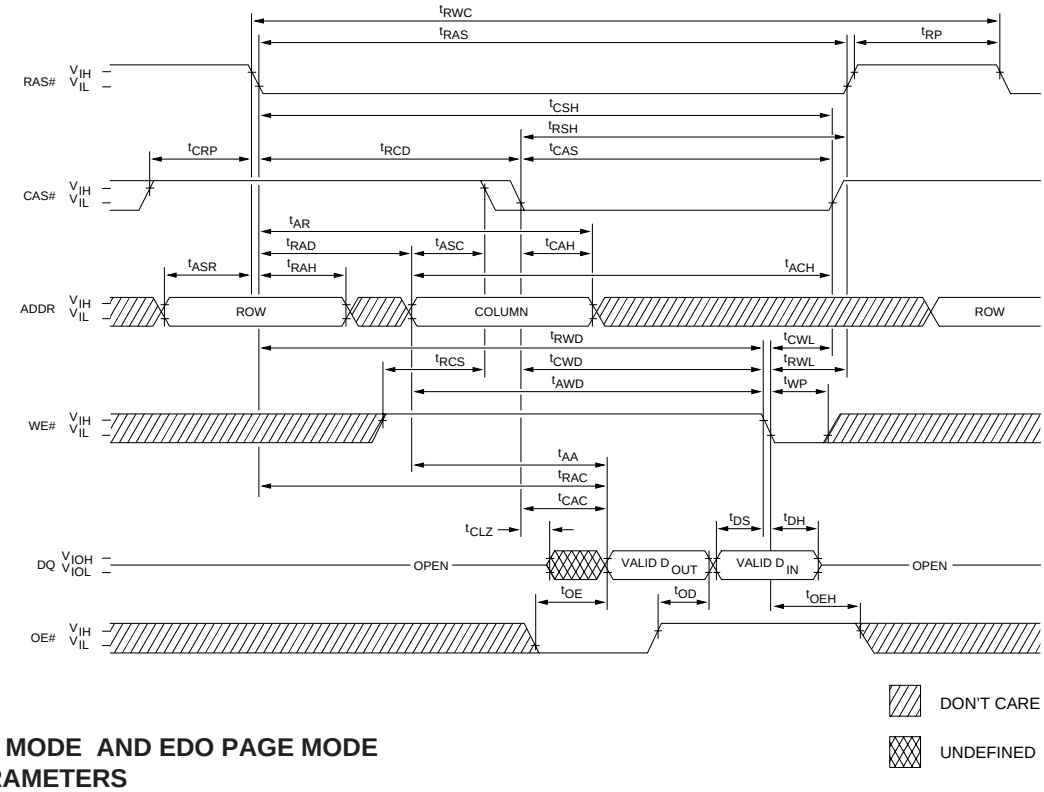
SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tACH (EDO)	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	—	—	15	10,000	ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	—		60		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	—		15		ns
tDH	8		10		ns
tDS	0		0		ns
tPC (EDO)	20		25		ns

SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tPC (FPM)	—		35		ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	—		15		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	—		20		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP (EDO)	5		5		ns
tWP (FPM)	—		10		ns

*EDO version only

READ-WRITE CYCLE [27]

(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

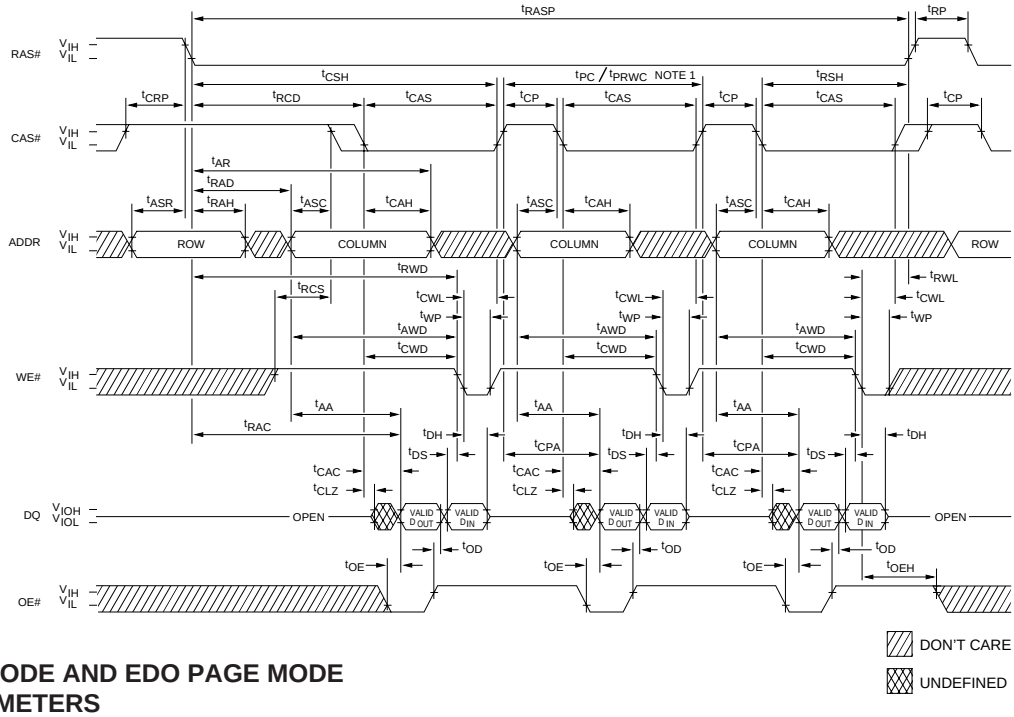
SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH (EDO)	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD (EDO)	42		49		ns
tAWD (FPM)	—		55		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	—	—	15	10,000	ns
tCLZ (EDO)	0		0		ns
tCLZ (FPM)	—		3		ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	—		60		ns
tCWD (EDO)	28		35		ns
tCWD (FPM)	—		40		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	—		15		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tOD (EDO)	0	12	0	15	ns
tOD (FPM)	—	—	3	15	ns
tOE		12		15	ns
tOEH (EDO)	8		10		ns
tOEH (FPM)	—		15		ns
tRAC		50		60	ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	—		15		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	—		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC (EDO)	116		140		ns
tRWC (FPM)	—		155		ns
tRWD (EDO)	67		79		ns
tRWD (FPM)	—		85		ns
tRWL	13		15		ns
tWP (EDO)	5		5		ns
tWP (FPM)	—		10		ns

*EDO version only

FAST/EDO-PAGE-MODE READ-WRITE CYCLE [27]

(LATE WRITE and READ-MODIFY-WRITE cycles)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

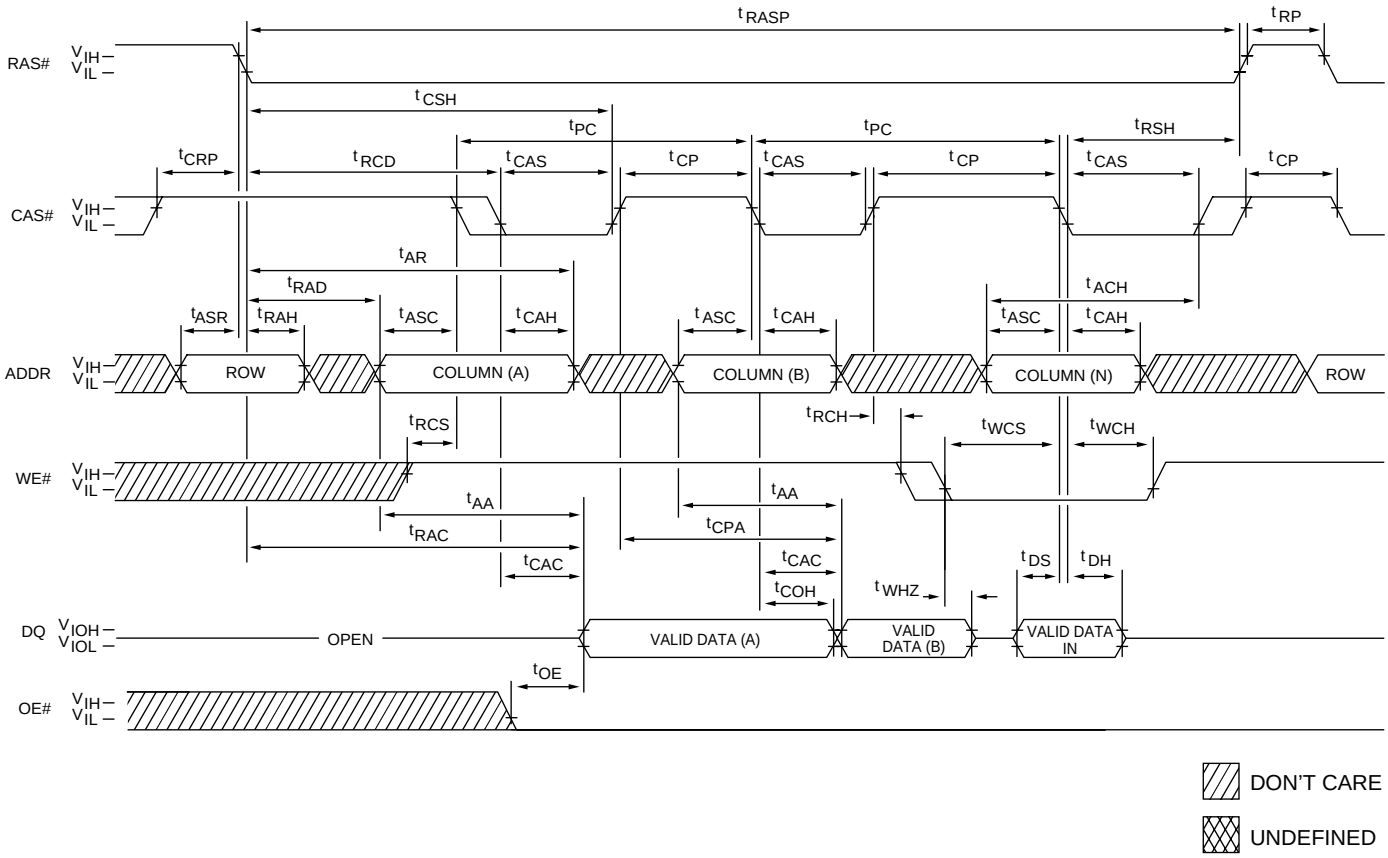
	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD (EDO)	42		49		ns
tAWD (FPM)	—		55		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	—	—	15	10,000	ns
tCLZ (EDO)	0		0		ns
tCLZ (FPM)	—		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	—		60		ns
tCWD (EDO)	28		35		ns
tCWD (FPM)	—		40		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	—		15		ns
tDH	8		10		ns
tDS	0		0		ns
tOD (EDO)	0	12	0	15	ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOD (FPM)	—	—	3	15	ns
tOE		12		15	ns
tOEH (EDO)	8		10		ns
tOEH (FPM)	—		15		ns
tPC (EDO)	20		25		ns
tPC (FPM)	—		35		ns
tPRWC (EDO)	47		56		ns
tPRWC (FPM)	—		85		ns
tRAC		50		60	ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	—		15		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	—		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD (EDO)	67		79		ns
tRWD (FPM)	—		85		ns
tRWL	13		15		ns
tWP (EDO)	5		5		ns
tWP (FPM)	—		10		ns

NOTE: 1. tPC is for LATE WRITE cycles only.

*EDO version only

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

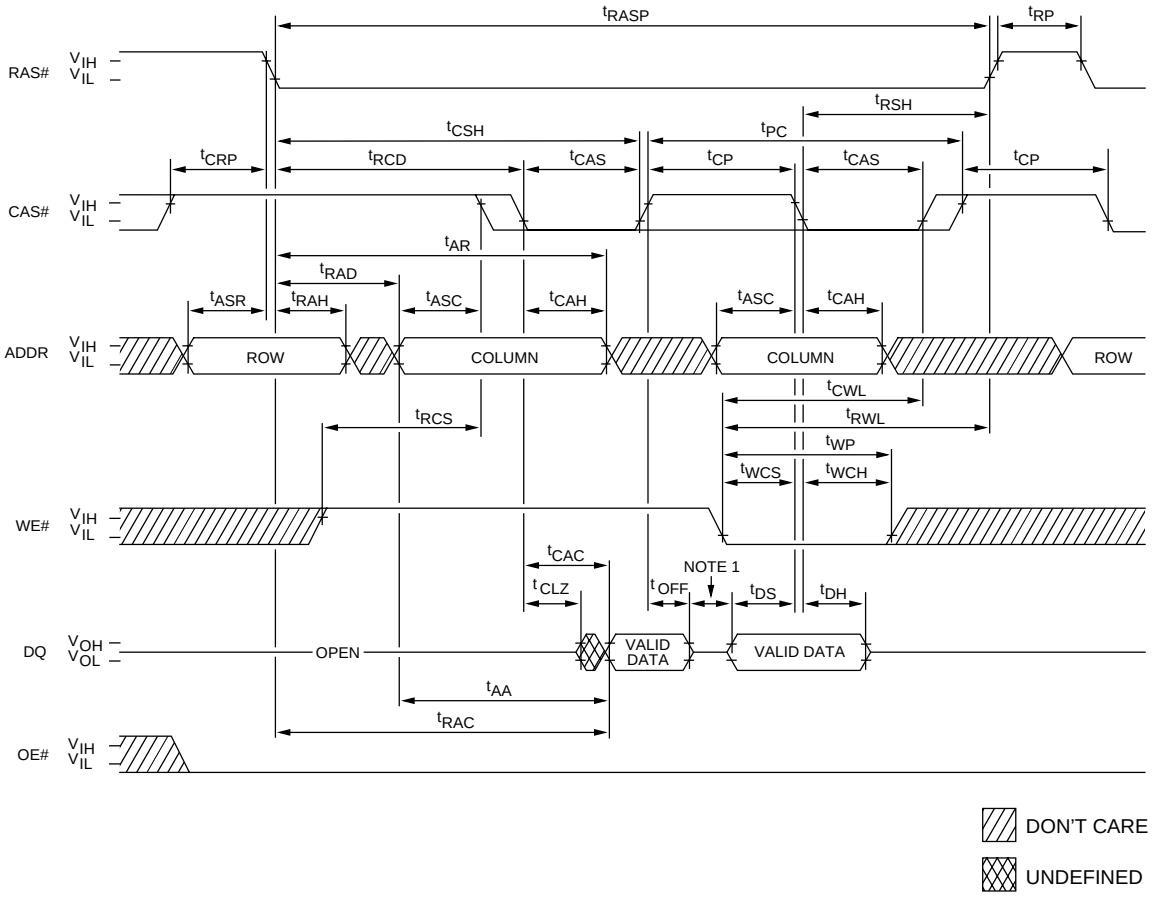


EDO PAGE MODE TIMING PARAMETERS

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns
tDS	0		0		ns

	-5		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ	0	12	0	15	ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



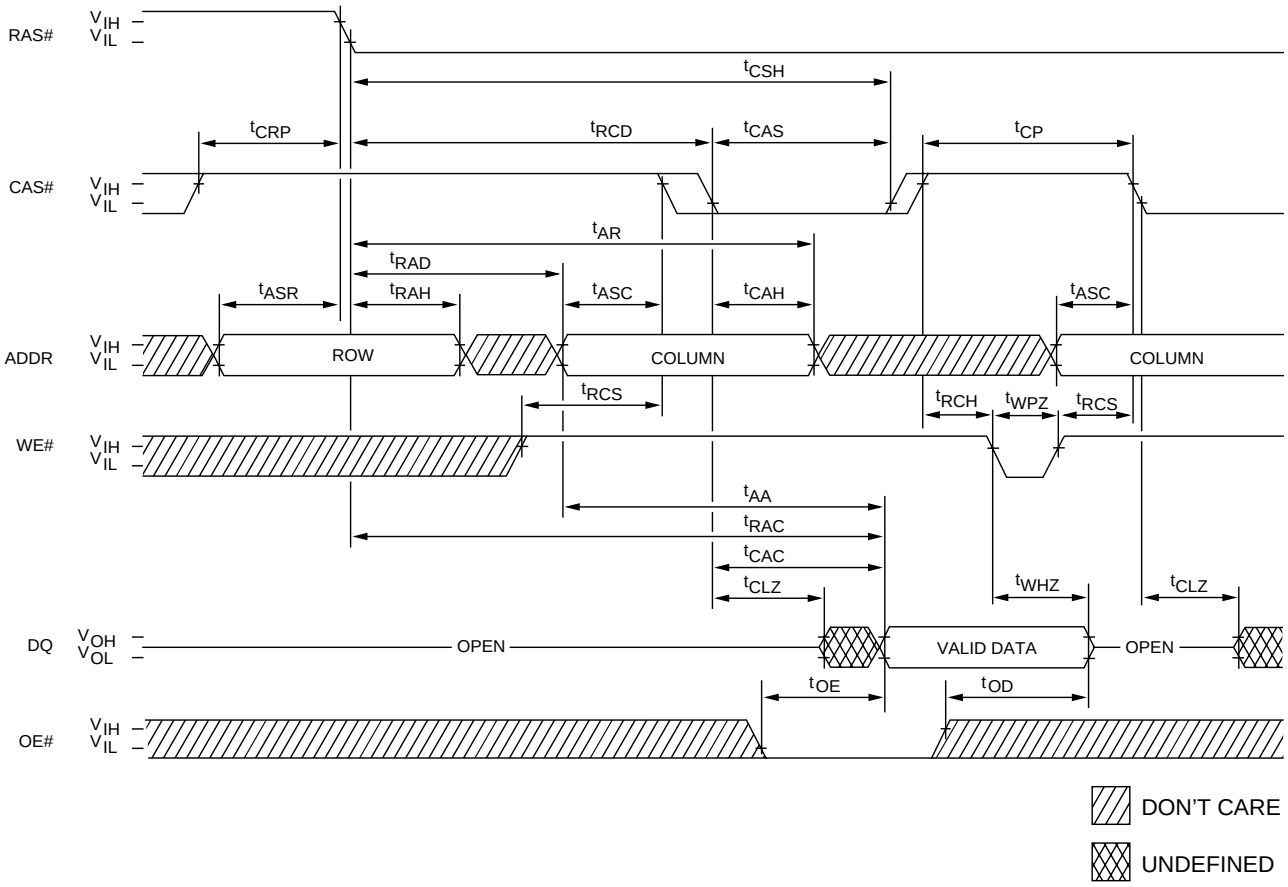
FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCRP	5		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCS	0		ns
tWP	10		ns

NOTE: 1. Do not drive data prior to tristate.

EDO READ CYCLE
(with WE#-controlled disable)

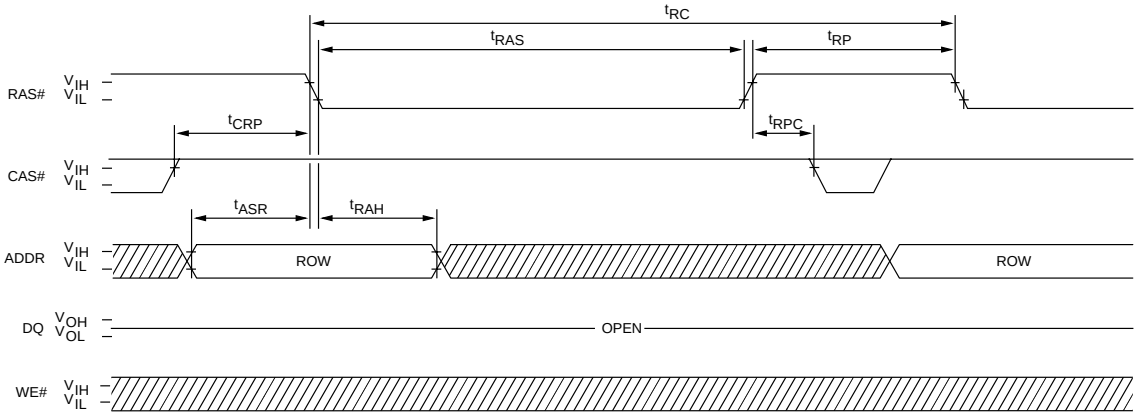


EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns

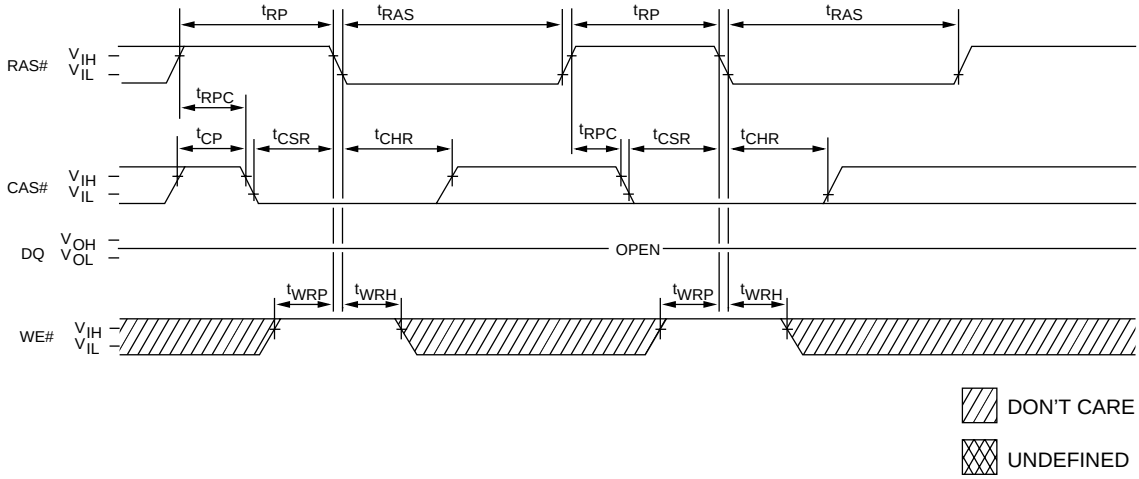
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ	0	12	0	15	ns
tWPZ	10		10		ns

RAS#-ONLY REFRESH CYCLE [27]



CBR REFRESH CYCLE [27]

(Addresses, OE# = DON'T CARE)



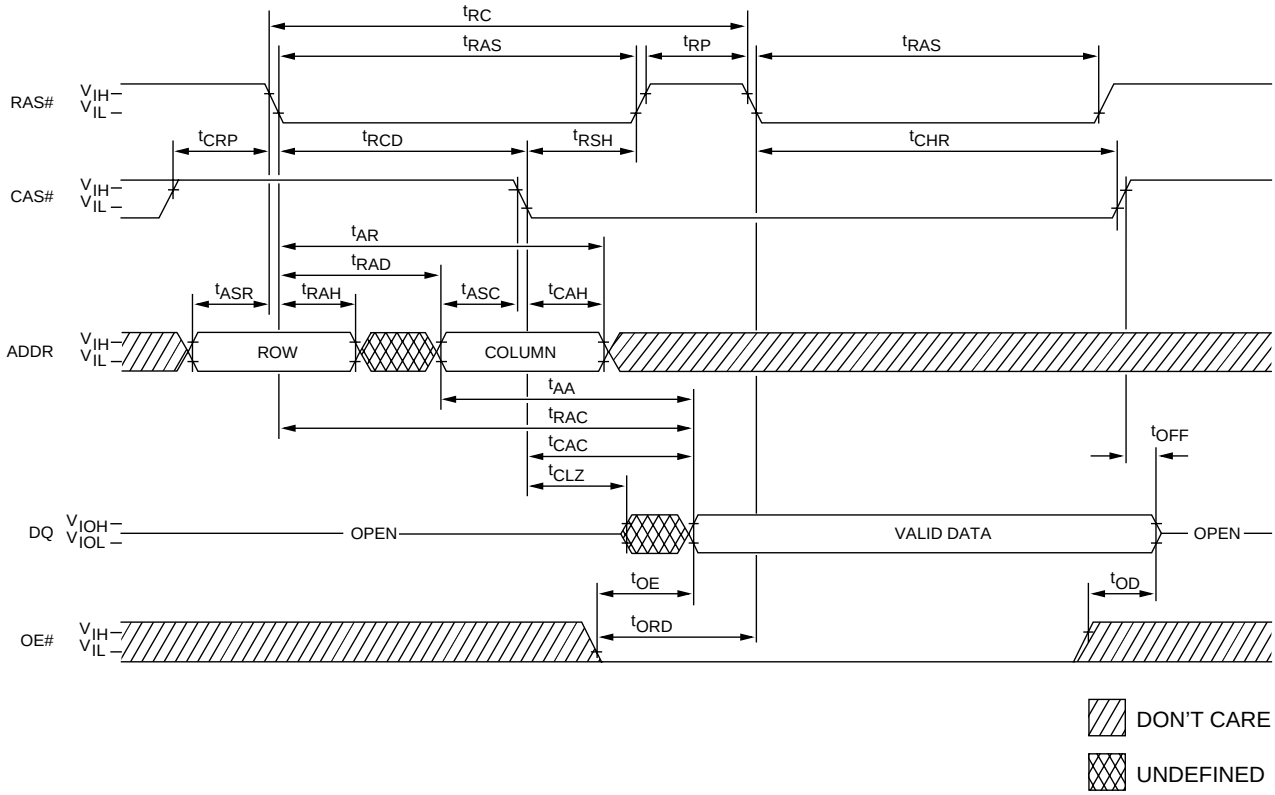
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCHR (FPM)	—		15		ns
tCHR (EDO)	8		10		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns

SYMBOL	-5* MIN	-5* MAX	-6 MIN	-6 MAX	UNITS
tRC (FPM)	—		110		ns
tRC (EDO)	84		104		ns
tRP	30		40		ns
tRPC (FPM)	—		0		ns
tRPC (EDO)	5		5		ns
tWRH	8		10		ns
tWRP	8		10		ns

*EDO version only

HIDDEN REFRESH CYCLE [20, 27]
(WE# = HIGH; OE# = LOW)



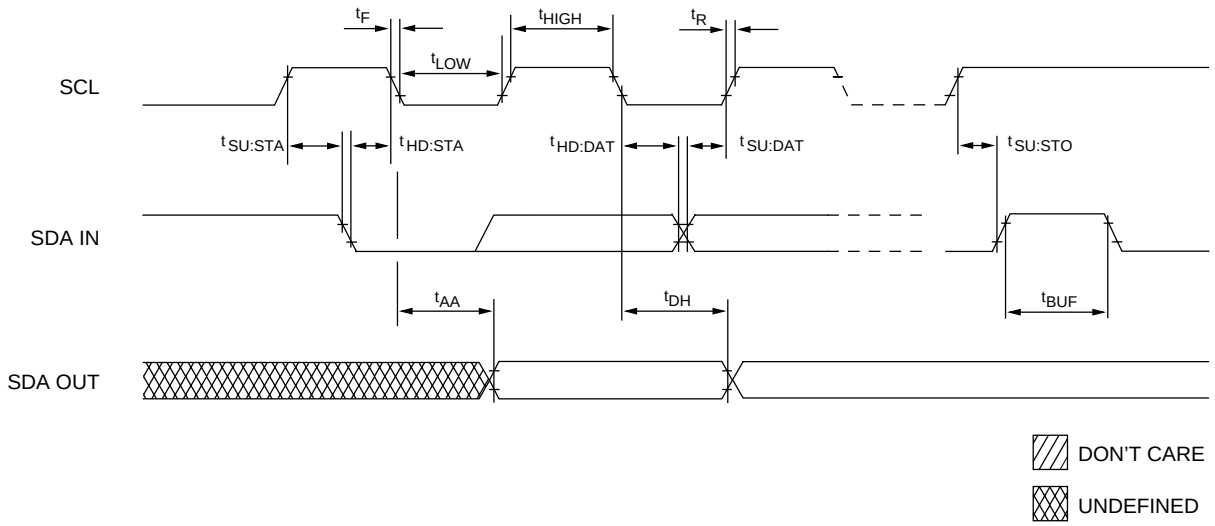
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR (FPM)	—		15		ns
tCHR (EDO)	8		10		ns
tCLZ (FPM)	—		3		ns
tCLZ (EDO)	0		0		ns
tCRP	5		5		ns
tOD (FPM)	—	—	3	15	ns
tOD (EDO)	0	12	0	15	ns
tOE		12		15	ns

	-5*		-6		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tOFF (FPM)	—	—	3	15	ns
tOFF (EDO)	0	12	0	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD (FPM)	—		15		ns
tRAD (EDO)	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	—		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	—		20		ns
tRCD (EDO)	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns

*EDO version only

SPD EEPROM



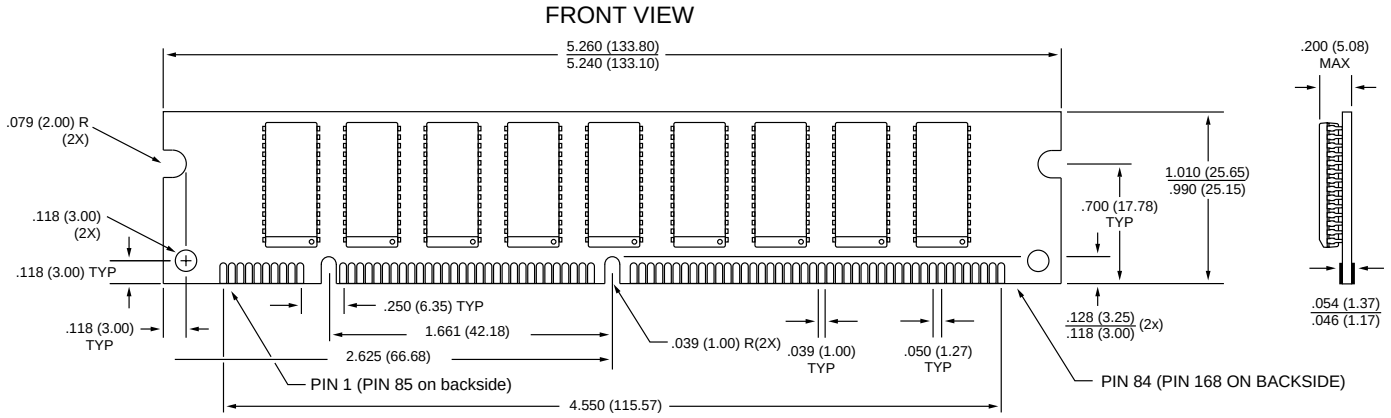
SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYM	MIN	MAX	UNITS
tAA	0.3	3.5	µs
tBUF	4.7		µs
tDH	300		ns
tF		300	ns
tHD:DAT	0		µs
tHD:STA	4		µs
tHIGH	4		µs
tI		100	ns

SYM	MIN	MAX	UNITS
tLOW	4.7		µs
tR		1	µs
tSCL		100	KHz
tSU:DAT	250		ns
tSU:STA	4.7		µs
tSU:STO	4.7		µs
tWR		10	ms

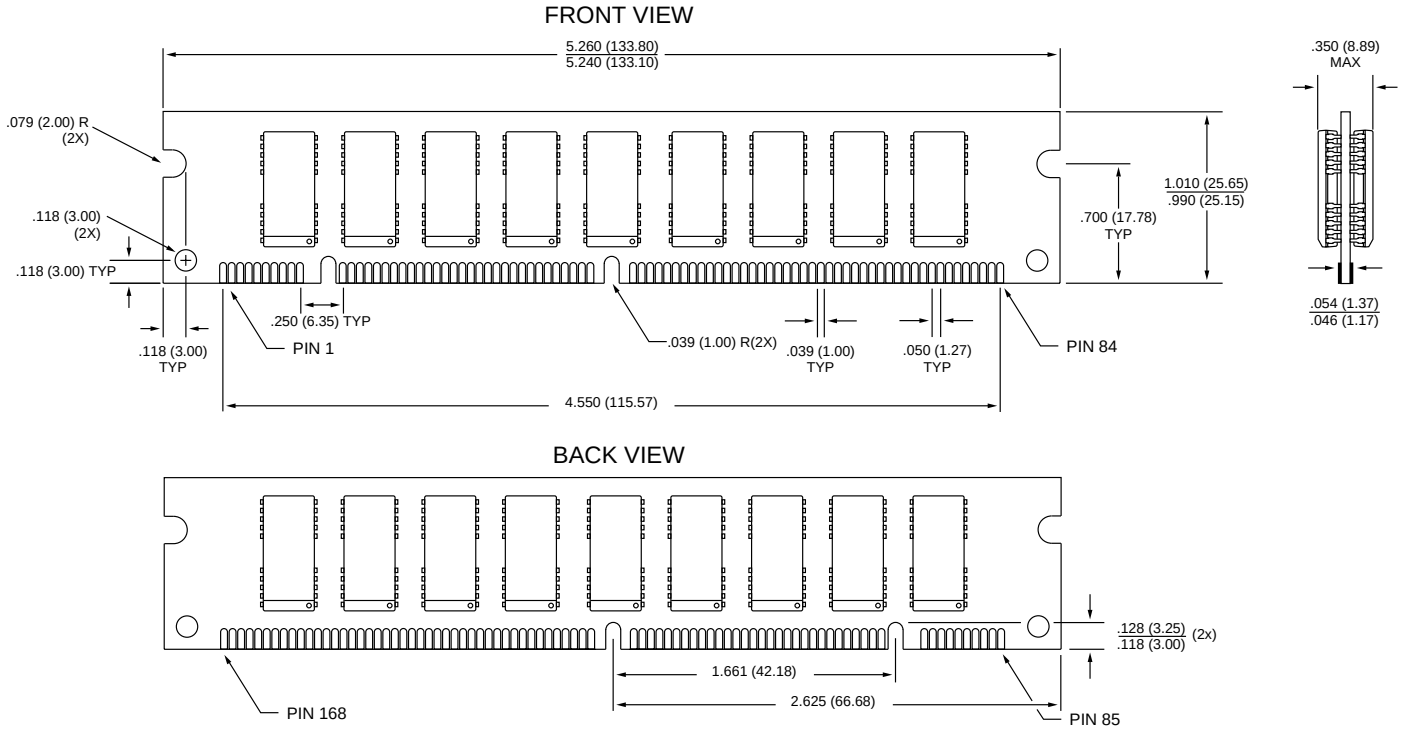
168-PIN DIMM

DE-11



168-PIN DIMM

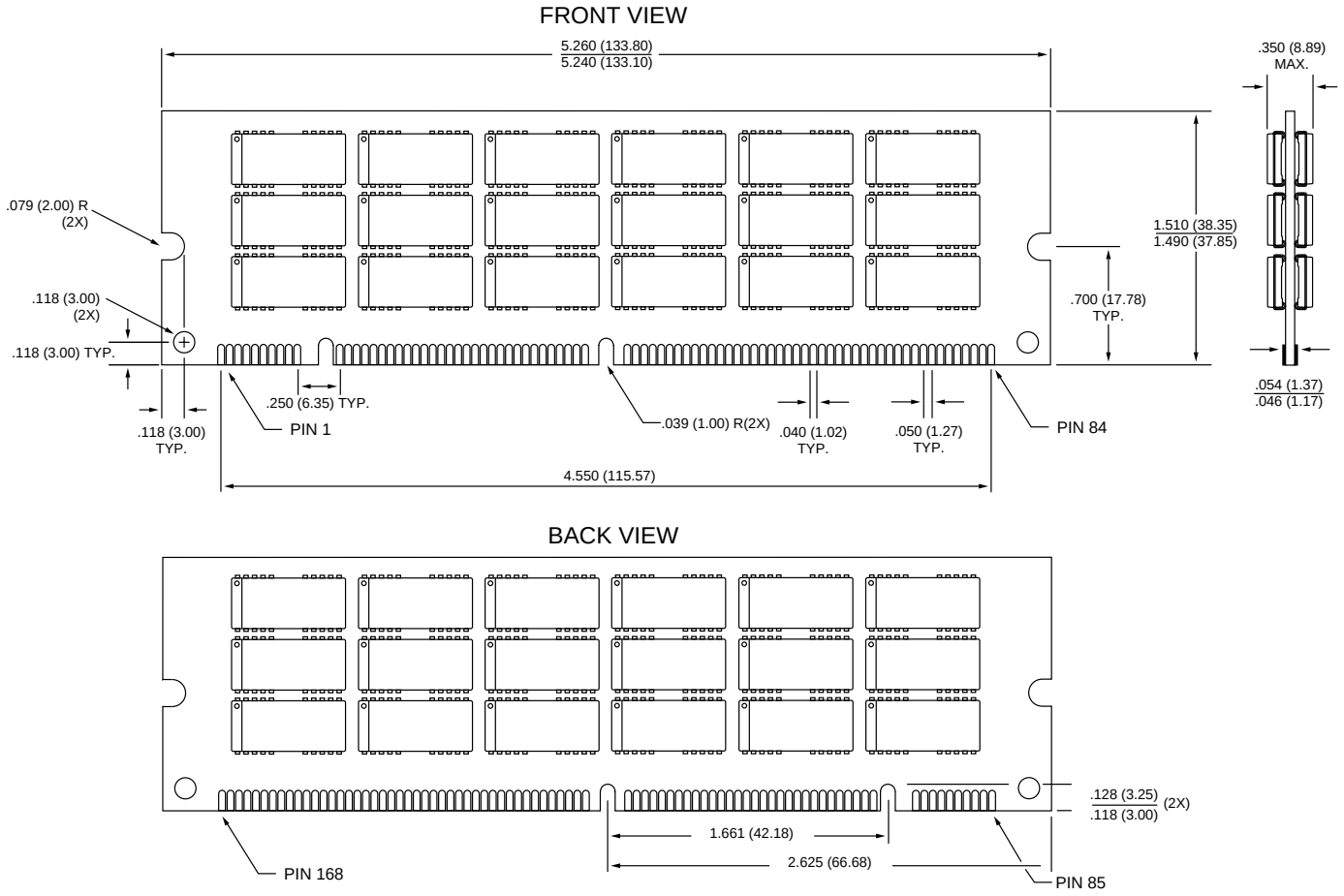
DE-12



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM

DE-24



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Technology that works for you.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900, Micron DataFax: 208-368-5800
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992