G8860
G8860X

032778

S-39 Only

001366

T-1366 GTE

Microcircuits

CMOS DTMF Decoder

Features

- 18 pin DIP package
- Central office quality detection
- Excellent voice talk-off
- Detect times down to 20mS
- Single supply 5V or 8 to 13V operation
- Latched 3 state buffered outputs
- Detects all 16 DTMF combinations
- Uses inexpensive 3.58MHz crystal
- Low power CMOS circuitry
- Adjustable acquisition & release times

Applications

Used in DTMF Receivers For:

- End to end signaling
- Control systems
- PABX
- Central office
- Mobile radio
- Key systems
- Tone to pulse converters

Description

The GTE G8860 and G8860X detects and decodes all 16 DTMF tone pairs. The device accepts the high group and low group square wave signals from a DTMF filter (G8865/G8865X) and provides a 3 state buffered 4 bit binary output. The clock signals are derived from an on chip oscillator requiring a single resistor and low cost TV crystal as external components. The G8860 and G8860X are produced using state-of-the-art CMOS technology and incorporate an on chip regulator, providing low power operation and power supply flexibility. The G8860X differs from the G8860 in that it contains an improved decode algorithm which provides enhanced talk-off performance. The G8860X also features faster and more closely-controlled response time. The G8860X may be used as a direct replacement for the G8860 in existing designs, provided consideration is given to the effect of shorter response time on system performance.

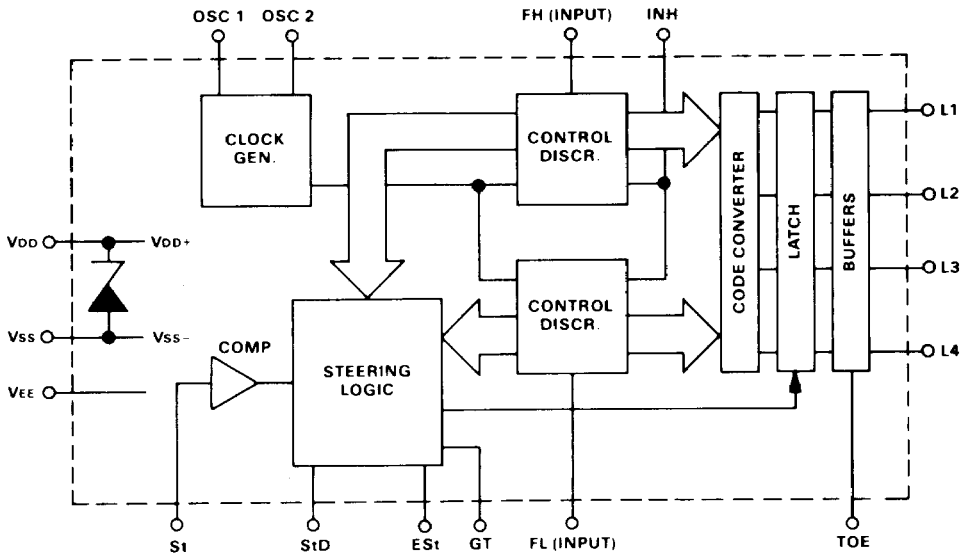
Pin Function

Pin	Description
OSC1	Clock Input
OSC2	Clock Output
IC	Internal Test Run
FH	High Freq. Group Input
L1-L4	Data Outputs

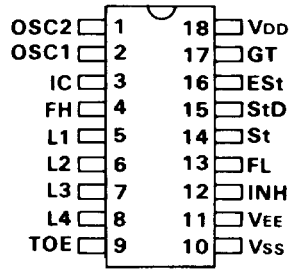
Pin	Description
TOE	Output Enable Input
INH	Inhibit Input
FL	Low Freq. Group Input
St	Steering Input
StD	Delayed Steering Output

Pin	Description
ESt	Early Steering Output
GT	Guard Time Output
VDD	Positive Power Supply
VSS	Internal Logic GND
VEE	Neg. Supply

Block Diagram



Pin Configuration



PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
V_{DD} - V_{EE}	Vdc	15V Max.
V_{DD} - V_{SS} (Low Impedance Supply)	Vdc	5.5V Max.
Voltage on any pin except OSC1 and OSC2	Vdc	V_{EE} -0.3, V_{DD} +0.3
Voltage on OSC1 and OSC2	Vdc	V_{SS} -0.3, V_{DD} +0.3
Current on any pin except V_{DD} and V_{EE}	I_{DD}	10mA Max.
Operating temperature	T_A	-40°C to +85°C
Storage temperature	Ts	-65°C to +150°C
Power dissipation [2]	P	1000 mW Max.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

G8860 DI
PI
x DI
x PI

DC Characteristics: All voltages referenced to V_{EE} unless otherwise noted. V_{DD} (See Note 4), T_A = 25°C, f_c = 3.579545 MHz

Parameter	Symbol	Min	Typ [3]	Max	Unit	Test Conditions
Operating Supply Voltage	V_{DD}	4.75	5	5.25	V	Connections Fig. 2a
(V_{DD} - V_{EE})		8		13	V	Connections Fig. 2b
Internal Logic Ground Voltage	V_{DDSS}	4.75		5.25	V	Connections Fig. 2a
(V_{DD} - V_{SS})		6.0	6.5	7.5	V	I_{dd} = 7mA
Operating Supply Current	I_{DD}		1.3	4	mA	5V
			2.5	5	mA	12V, V_{DD} - V_{SS} = 5.5V
Internal Logic Ground Pin Current	I_{SS}		5.5	6.7	mA	12V, R_{SSEE} = 900 Ω
Operating Power Consumption	P_o		6.5		mW	5V
			66		mW	12V
High Level Input Voltage	V_{IH}	3.5			V	5V
(All Inputs Except OSC1)		8.5			V	12V
Low Level Input Voltage	V_{IL}			1.5	V	5V
(All Inputs Except OSC1)				3.5	V	12V
High Level Input Voltage	V_{IHO}	3.5			V	5V
OSC1		10.5			V	12V
Low Level Input Voltage	V_{ILO}			1.5	V	5V, Ref Vss
OSC1				1.5	V	12V, Ref Vss
Steering Input Threshold	V_{TSI}	2.04	2.27	2.5	V	5V
Voltage		5.4	6.0	6.6	V	12V
Pull Down Sink Current	I_{SI}	10	25	75	μA	5V
(INH)		10	190	400	μA	12V
Pull Up Source Current	I_{SO}	2	7	45	μA	5V + 12V
(TOE)						
Input High Leakage Current	I_{IH}		0.1	1.5	μA	5V or 12V
Input Low Leakage Current	I_{IL}		0.1	1.5	μA	
High Level Output Voltage	V_{OH}	4.9			V	5V
(All Outputs Except OSC2)		11.9			V	12V
Low Level Output Voltage	V_{OL}			0.1	V	5V
(All Outputs Except OSC2)				0.1	V	12V
High Level Output Voltage	V_{OHO}	4.9			V	5V
OSC2		11.9			V	12V

DC Characteristics (Continued)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Low Level Output Voltage OSC2		V_{OL}			0.1	V	5V, Ref Vss
					0.1	V	12V, Ref Vss
Output Drive Current (All Outputs Except OSC2)	P Channel Source	I_{OH}	0.4	0.6		mA	5V, V_{OH} = 4.6V
			0.5	0.8		mA	12V, V_{OH} = 11.5V
	N Channel Sink	I_{OL}	0.8	1.2		mA	5V, V_{OL} = 0.4V
			1.0	1.6		mA	12V, V_{OL} = 0.5V
Output Drive Current OSC2	P Channel Source	I_{OH}	90	120		µA	5V, V_{OH} = 4.6V
			90	120		µA	12V, V_{OH} = 11.5V
	N Channel Sink	I_{OL}	100	160		µA	5V, V_{OL} = 0.5V
			100	160		µA	12V, V_{OL} = 0.5V
Tristate Output Current (High Impedance State)	L1-L4 = H	I_{OZ}		0.035	1.5	µA	5V, Appl V_{OL} = 0V
	L1-L4 = L			0.1	1.5	µA	5V, Appl V_{OH} = 5V
	L1-L4 = H			0.1	1.5	µA	12V, Appl V_{OL} = 0V
	L1-L4 = L			0.3	1.5	µA	12V, Appl V_{OH} = 12V

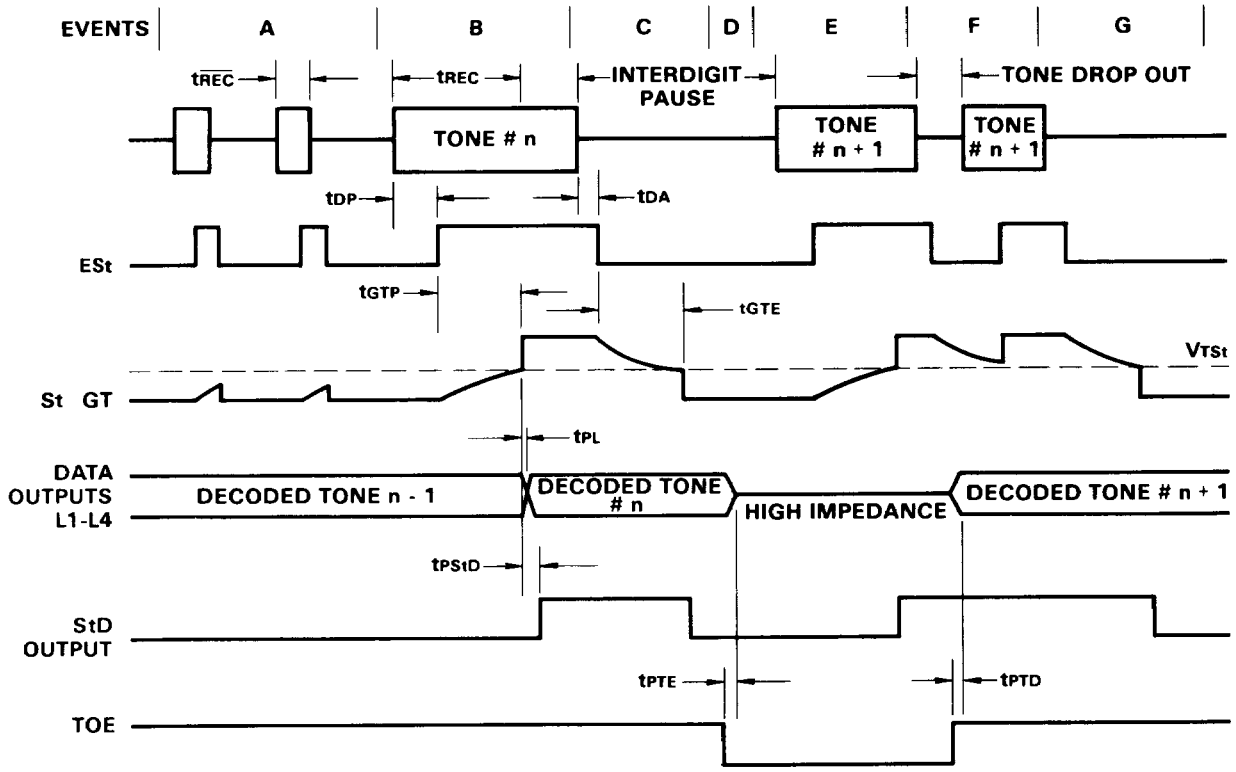
AC Characteristics: V_{DD} = 5V Unless Otherwise Noted, T_A = 25°C, f_c = 3.579545 MHz

Parameter		Symbol	Min	Typ[3]	Max	Unit	Test Conditions	
Tone Frequency Deviation Accept		Δf_A			±2.5	% Nom.		
Tone Frequency Deviation Reject		Δf_R	±3.5			% Nom.		
Tone Present Detection Time (G8860)		t_{DP}	8	10	15	mS		
Tone Absent Detection Time (G8860)		t_{DA}	0.6	4	10	mS		
Tone Present Detection Time (G8860X)		t_{DP}	6		10	mS		
Tone Absent Detection Time (G8860X)		t_{DA}	0		6	mS		
Guard Time		$t_{GT(P\ or\ E)}$	Adjustable Functions of t_{GT}. See Figs. 3 and 4 and Timing Diagram					
Time to Receive = (t_{DP} + t_{GTP})		t_{REC}						
Invalid Tone Duration (f_n of t_{REC})		$t_{\overline{REC}}$						
Interdigit Pause = (t_{DA} + t_{GTA})		t_{ID}						
Acceptable Drop Out (f_n of t_{ID})		t_{DO}						
FL FH Input Transition Time		t_T			1.0	µS	10% - 90% V_{DD}	
Capacitance Any Input		C		5	7.5	pF		
Propagation Delay St to L1-L4		t_{PL}		8	11	µS	5V or 12V	
Propagation Delay St to StD		t_{PStD}		12	14	µS	5V or 12V	
Synch. Delay L1-L4 to StD		t_{QStD}		3.43		µS		
Propagation Delay TOE to L1-L4	Enable	t_{PTE}		300		nS	5V	
				200		nS	12V	
	Disable	t_{PTD}		300		nS	5V	
				200		nS	12V	
Crystal/Clock Frequency		f_c	3.5759	3.5795	3.5831	MHz	OSC1	OSC2
Clock Input (OSC1)	Rise Time	t_{LHCI}			110	nS	10%-90%	Externally
	Fall Time	t_{HLCI}			110	nS	V_{DD} - Vss	Applied
	Duty Cycle	DC_{CI}	40	50	60	%		Clock
Clock Output (OSC2)	Capacitive Load	C_{LO}			30	pF		

Notes:

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Derate 16mW/°C above 75°C. All leads soldered to PC board.
3. All "typical" parametric information is for reference only, not guaranteed and not subject to production testing.
4. 5 V: V_{DD} - V_{EE} = 5V, Vss = V_{EE} connection as Fig. 2a.
   12V: V_{DD} - V_{EE} = 12V, R_{SSEE} = 900 Ω connection as Fig. 2b.
5. Outputs are not loaded unless stated.
6. For input current parameters only V_{IH} - V_{IHO} = V_{DD}, V_{IL} = V_{EE}, V_{ILO} = Vss.

Timing Diagram



EVENTS:

A) Short tone bursts: detected, tone duration is invalid.
B) Tone # n is detected, tone duration is valid, decoded to outputs.
C) End of Tone # n is detected and validated.
D) 3 stage outputs disabled (high impedance).
E) Tone # n + 1 is detected, tone duration is valid, decoded to outputs.
F) Tristate outputs are enabled. Acceptable drop out of Tone # n + 1 does not register at outputs.
G) End of Tone # n + 1 is detected and validated.

Pin Function Table

OSC2	CLOCK OUTPUT	3.58MHz crystal with parallel 5MΩ resistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
OSC1	CLOCK INPUT	
IC	Internal connection for testing only. Must be left open circuit.	
FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter.	
L1 L2 L3 L4	Data Outputs. 3 state buffered. Provides 4 bit binary word corresponding to the tone pair decoded, when enabled by TOE. See Coding Tables.	
TOE	3 state output enable input. Logic high on this input enables outputs L1-L4. Internal pull up.	
V_{SS}	Internal logic ground. For V_{DD}-V_{EE} = 5V V_{SS} connected to V_{EE}. For V_{DD}-V_{EE} > 8V, V_{SS} connected via resistor to V_{EE} see Fig. 2.	
V_{EE}	Negative power supply. External logic ground.	
INH	Inhibit input. Logic high inhibits detection of tones representing characters #, *, A, B, C, D. Internal pull down.	
FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter.	
St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs. Voltage < V_{TSt} on this pin frees the device to accept a new tone pair. See Coding Tables (c) and Functional Description.	
StD	Delayed Steering Output. Flags when a valid tone pair has been received. Presents logic high when output latch updated based on St voltage exceeding VTSt. Returns to logic low when St voltage falls below VTSt.	
ESt	Early Steering Output. Presents a logic high when the digital algorithm detects a recognizable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low.	
GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt. See Coding Tables (c).	
V_{DD}	Positive power supply.	

Functional Description

The GTE G8860 and G8860X are CMOS Digital DTMF detectors and decoders. Used in conjunction with a suitable DTMF filter (GTE G8865) it can detect and decode all 16 Standard DTMF tone pairs (Fig. 1), accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the G8860 must be preceded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sine wave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The High Group and Low Group rectangular waves are applied to the G8860 FH and FL inputs respectively. The G8865 DTMF Filter provides these functions.

Within the G8860 the FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators, Block Diagram — Page 1) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both High Group and Low Group signals have been simultaneously detected a flag ESt (Logic High) is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Timing Diagram) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of "tone absent" before a valid received tone is recognized as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig. 4a) is charged via resistor R from ESt when a DTMF tone pair is detected. After a period t_{GTP} V_C exceeds the St input threshold voltage V_{STt} setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (see Coding Tables) and Timing Diagram.

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents a 4 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs L1 to L4. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_C (Fig. 4a) falling below V_{TSt}.

Increasing the "time to receive" t_{REC} tends to further improve talk off performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal to noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTE} as shown in Fig. 4.

When L1-L4 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The G8860 may be operated from either a 5 volt or 8 to 13 volt supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig. 2. When using the G8860 with the G8865 DTMF Filter it is only necessary to use the G8865 crystal oscillator (see Fig. 3). When using the higher supply voltage range the G8865 OSC2 output should be capacitively coupled to the G8860 OSC1 input as shown in Fig. 3.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves talk off due to the reduced number of detectable tones.

Coding Tables

A. Output Coding

Original Tone Character		TOE	L4	L3	L2	L1
	X	L	Z	Z	Z	Z
DR	1	H	L	L	L	H
	2	H	L	L	H	L
	3	H	L	L	H	H
	4	H	L	H	L	L
	5	H	L	H	L	H
	6	H	L	H	H	L
	7	H	L	H	H	H
	8	H	H	L	L	L
	9	H	H	L	L	H
	0	H	H	L	H	L
D	*	H	H	L	H	H
	#	H	H	H	L	L
	A	H	H	H	L	H
	B	H	H	H	H	L
	C	H	H	H	H	H
	D	H	L	L	L	L

B. Inhibit Function

Detected Character	INH	ESt
None	0	L
X	L	H
DR	H	H
D	H	L

C. Steering

ESt	St	GT	StD(1)
L	L	L	L
H	L	Z	L
L	H	Z	H
H	H	H	H

Notes:
1. Delayed WRT St.
2. For the purpose of these tables consider:
   $V_{St} < V_{TSt}$ LOGIC LOW (L)
   $V_{St} > V_{TSt}$ LOGIC HIGH (H)

H = LOGIC HIGH
L = LOGIC LOW
O = "DON'T CARE" LOGIC HIGH OR LOW
Z = HIGH IMPEDANCE
X = ANY CHARACTER

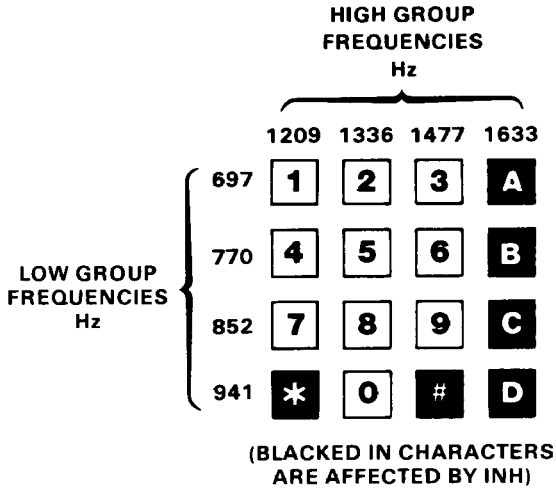


Fig. 1 DTMF Matrix Indicating Character—Tone Pair Correspondence.

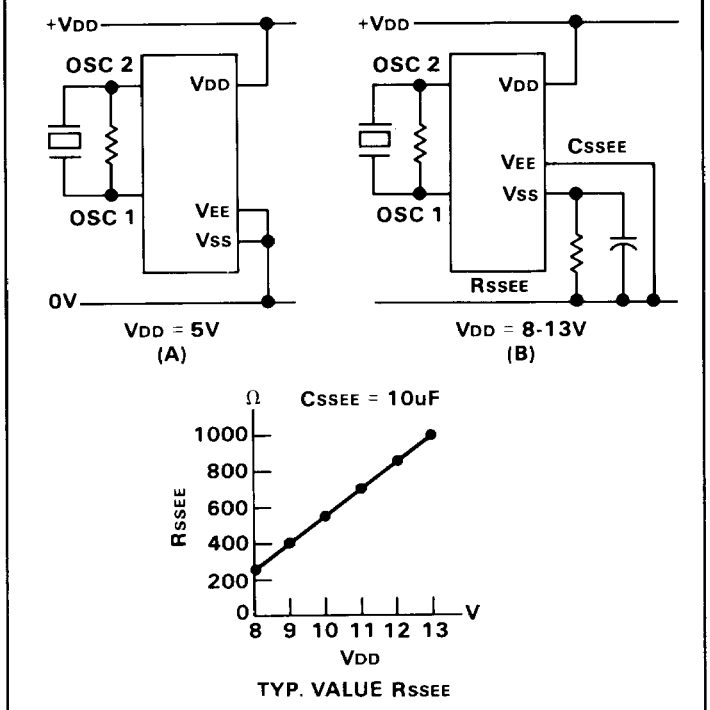
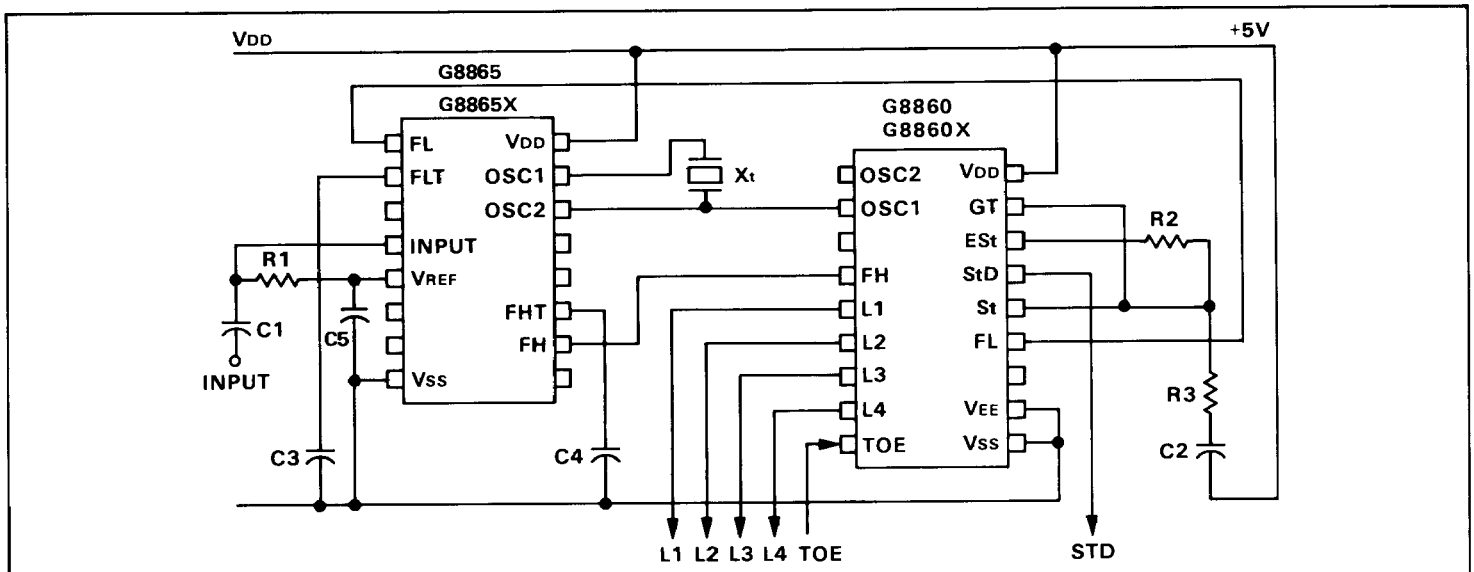
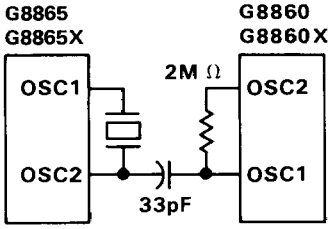


Fig. 2 Power Supply Connection Options





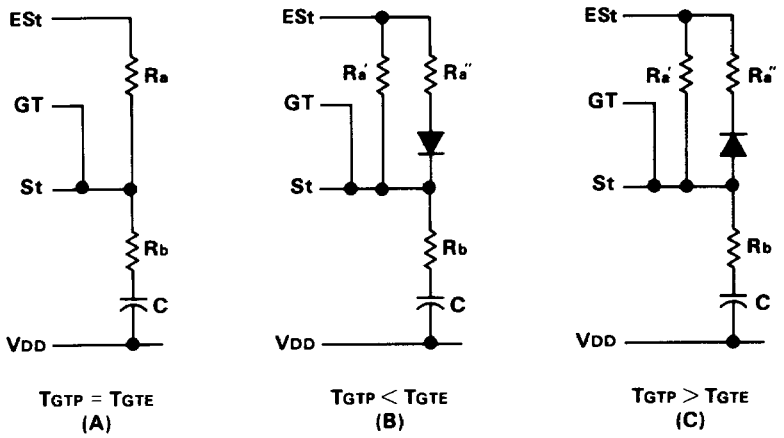
R1 = 2.0M Ω C2 = 0.1 μF
R2 = 300K Ω C3 = C4 = 680pF
R3 = 5K Ω Xt = 3.579MHz
C1 = 10nF
C5 = .3 μF

Note: For operation with VDD - VEE > 5.25V connect with power supply connections as Fig. 2B.

TYPICAL PERFORMANCE

Dynamic Range	30dB
Twist	±10dB
Acc. S/N Ratio	14dB
TREC (G8860)	28 to 35mS
TREC (G8860X)	26 to 30mS
Guard Time	20mS
Max. Invalid Tone Duration	20mS
Min. Interdigit Pause	30mS
Max. Acceptable Dropout	20mS

Fig. 3 Connection Diagram for Single Ended Input Receiver Using the G8865 (5V Operation)



$$T_{GTP} = C(R_a + R_b)\ \text{LOGn}\ \left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{DD} - V_{TSt}}\right)$$

$$T_{GTE} = C(R_a + R_b)\ \text{LOGn}\ \left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{TSt}}\right)$$

FOR V_{OHESt}, V_{OLESt} Symetric About $V_{TSt} = \frac{1}{2} V_{DD}$
WITH $R_b < 0.1\ R_a$ $\quad R_b \geq V_{DD} - V_{EE}\ K\ \Omega$

$$R_b < 0.1\left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$$

A) $T_{GTP} = T_{GTE} \triangleq 0.69\ R_a\ C\left(1 - \frac{R_b}{2\ R_a}\right)$

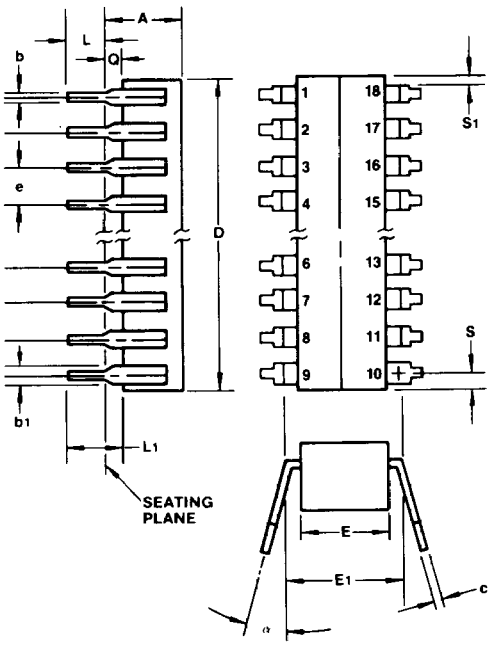
B) T_{GTP} } $\triangleq 0.69\ C\left(\frac{R_a' R_a''}{R_a + R_a''}\right)$
C) T_{GTE} }

B) T_{GTE} }
C) T_{GTE} } $\triangleq 0.69\ R_a'\ C$

Fig. 4 Guard Time Adjustment

Packaging Information

Cerdip Package



SYM-BOL	18-PIN PACKAGE INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	0.200	—	5.08
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	0.960	—	24.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

Ordering Information

Device	Package	Temp. Range
G8860DI	18 Pin Cerdip	-40°C to +85°C
G8860XDI	18 Pin Cerdip	-40°C to +85°C

Sales Offices: Technical or sales assistance may be requested from the GTE Microcircuits area sales office nearest you.

Western
GTE Microcircuits
22691 Lambert Street
Suite 507
El Toro, CA 92630
Tel: 714/855-9901
TWX: 910-595-2752

Central
GTE Microcircuits
3223 N. Frontage Road
Suite 2311
Arlington Heights, IL 60004
Tel: 312/259-1112
TWX: 910-687-0282

Eastern
GTE Microcircuits
380 Town Line Road
Hauppauge, NY 11788
Tel: 516/724-8300
TWX: 510-226-7847

Europe
GTE Microcircuits
Montenstrasse 11
8000 Munich 19
West Germany
Tel: 089/1 78 20 31
Telex: 528452 gtemc d

WARNING:
MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or in conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

Represented in your area by: