8275-B,F,W

DESCRIPTION

The 8275 is a QUAD LATCH circuit designed to provide temporary storage of four bits of information. A common application is as a holding register between a counter and a display driver (such as the 8280 and 8T01.) Separate enable lines to latches 1-2 and 3-4 allow individual control of each pair of latches. Initially, data is transferred on the rising edge of the enable pulse. While the enable is high, output Q follows the data input. When the enable falls, the input data present at fall time is retained at the Q output. Both Q and $\overline{Q}$ are accessible.

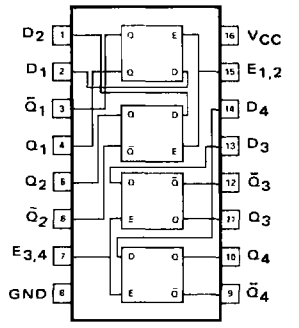
TRUTH TABLE (EACH LATCH)

ENABLE	DATA	Q	$\overline{Q}$
1	1	1	0
1	0	0	1
0	1	*	*
0	0	*	*

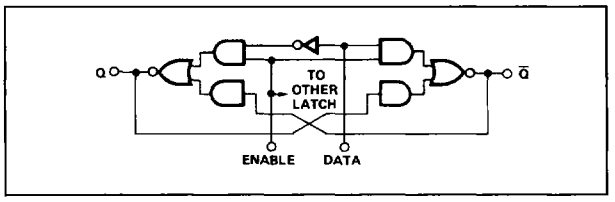
*No change.

PIN CONFIGURATION

B,F,W PACKAGE



LOGIC DIAGRAM



SWITCHING CHARACTERISTICS T_A=25°C, V_{CC}=5V

PARAMETER		FROM INPUT	TO OUTPUT	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{setup}	Setup time[1]							
	Low	D				14	20	ns
	High					12	20	
t_{hold}	Hold time[2]							
	Low	D			0	6		ns
	High				0	15		
Propagation Delay Time								
t_{PLH}	Low-to-high	D	Q			16	30	ns
t_{PHL}	High-to-low					14	25	
t_{PLH}	Low-to-high	D	$\overline{Q}$			24	40	
t_{PHL}	High-to-low					7	15	
t_{PLH}	Low-to-high	E	Q			16	30	
t_{PHL}	High-to-low					12	20	
t_{PLH}	Low-to-high	E	$\overline{Q}$			16	30	
t_{PHL}	High-to-low					12	20	

NOTES:
1. t_{setup} is defined as the time prior to the fall of the clock.
2. t_{hold} is defined as the time after the fall of the clock.

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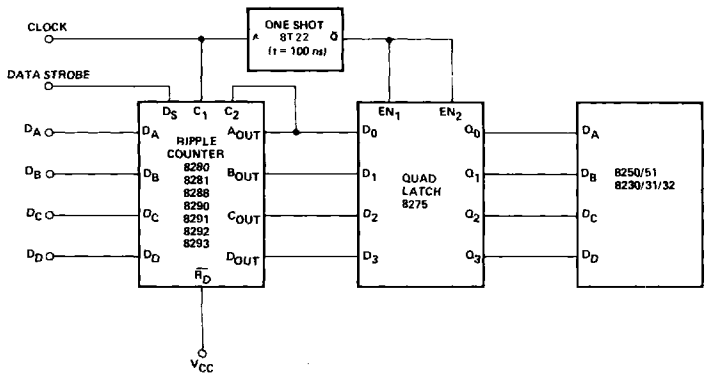
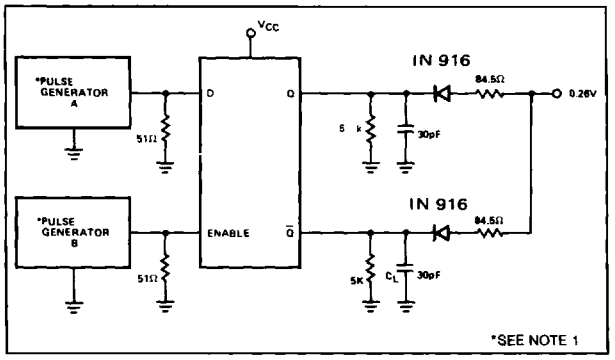
TYPICAL APPLICATION

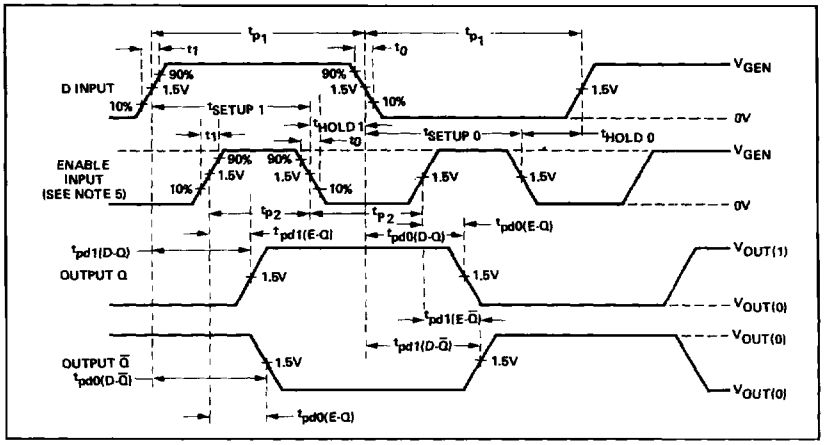
OUTPUT STROBING OF RIPPLE COUNTER TO achieve SYNCHRONOUS OUTPUT CHANGES



AC TEST FIGURE



AC TEST WAVEFORMS



NOTES:

1. The pulse generators have the following characteristics: V_{gen} = 3V. $t_1 = t_0 \leq 10$ns, and $Z_{out} \approx 50\Omega$. For pulse generator A, t_{p1} = 1μs and PRR = 500Hz. For pulse generator B, tp2 = 500ns and Prr = 1MHz. Positions of D-input and enable input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. When measuring $t_{pd}1$ (D-Q), $t_{pd}0$ (D-Q), $t_{pd}0$ (D-$\overline{Q}$), and $t_{pd}1$(D-$\overline{Q}$), enable input must be held at logical 1.

LOGIC