

HN62444BN Series

4M (256K x 16-bit) Mask ROM

DESCRIPTION

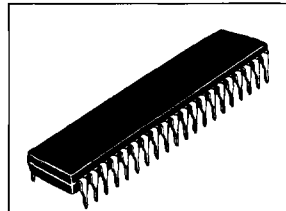
The Hitachi HN62444BN is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16-bit.

The high density and high speed Fast Address Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

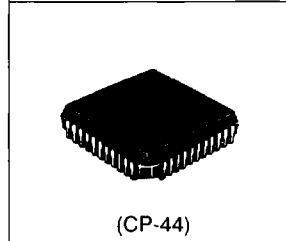
Hitachi's HN62444B is offered with JEDEC-Standard pinouts in 40-pin Plastic DIP and 44-lead PLCC packages.

FEATURES

- Single Power Supply:
 $V_{CC} = 5 V \pm 10\%$
- Normal Access Time:
120 ns (max)
- Fast Address Access Time (A_0, A_1):
70 ns (max)
- Low Power Dissipation:
Active Current: 150 mW (typ)
Standby Current: 5 μ W (typ)
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
JEDEC Standard Word-Wide EPROM Pinout
- Packages:
40-pin Plastic DIP
44-lead PLCC



(DP-40)



(CP-44)

ORDERING INFORMATION

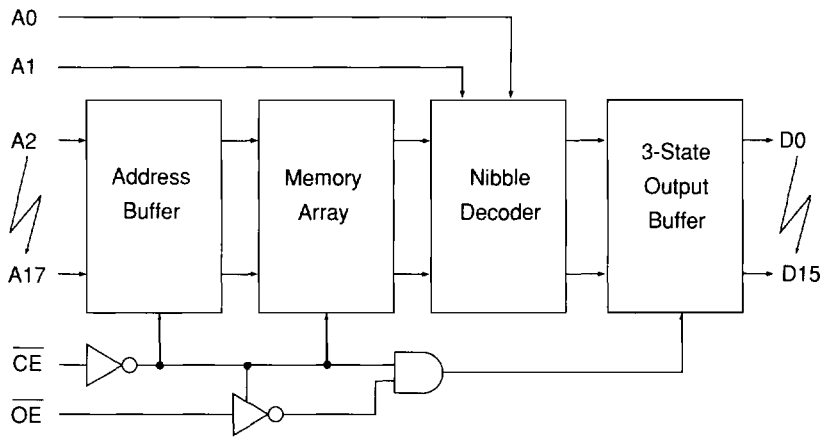
Type No.	Access Time	Package
HN62444BNP	120 ns	40-pin Plastic DIP (DP-40)
HN62444BNCP	120 ns	44-lead PLCC (CP-44)

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■ PIN DESCRIPTION

Pin Name	Function
A ₀ - A ₁₇	Address
D ₀ - D ₁₅	Output
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



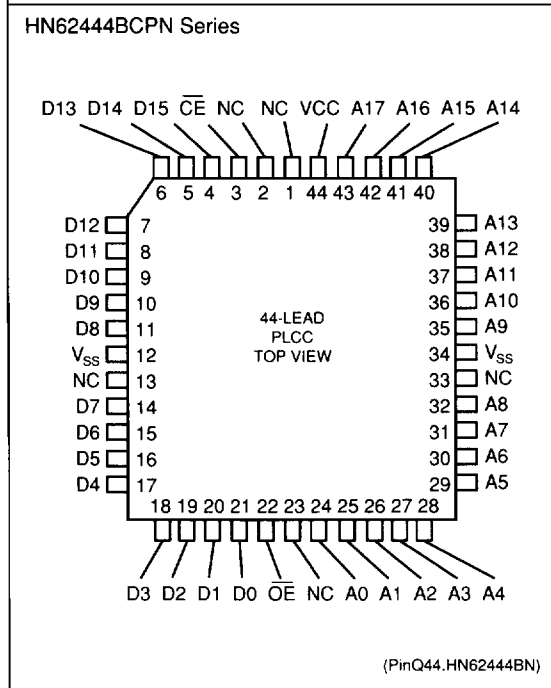
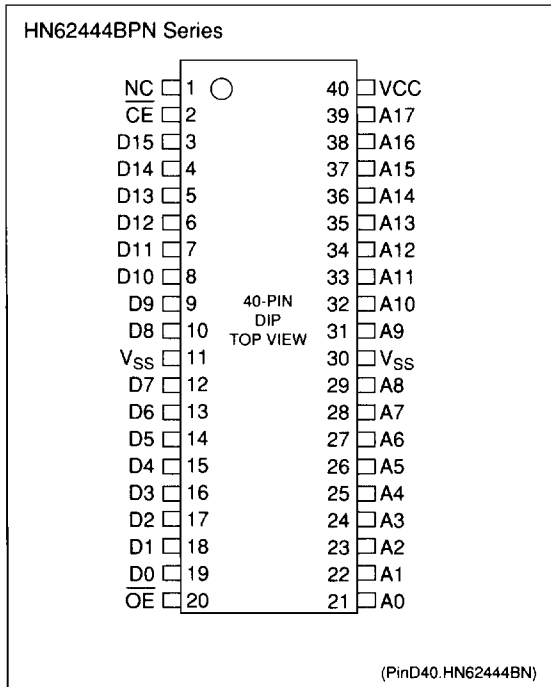
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■ PIN ARRANGEMENT



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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage ¹	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage ¹	V_T	-0.3 to $V_{CC} + 0.3$	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Note: 1. Relative to V_{SS} .

■ CAPACITANCE

($V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = 25^\circ C$, $V_{IN} = 0V$, $f = 1MHz$)

Item	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	-	-	15	pF
Output Capacitance	C_{OUT}	-	-	15	pF

Note: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0$ to $70^\circ C$)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	μA	$V_{IN} = 0$ to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	μA	$\overline{CE} = 2.4$, $V_{OUT} = 0$ to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	120	mA	$V_{CC} = 5.5V$, $I_{DOUT} = 0$ mA, $t_{RC} = \text{min.}$
Standby V_{CC} Current	I_{SB1}	-	-	30	μA	$V_{CC} = 5.5V$, $\overline{CE} \geq V_{CC}$ to $-0.2V$
	I_{SB2}	-	-	3	mA	$V_{CC} = 5.5V$, $\overline{CE} \geq 2.4V$
Input Voltage	V_{IH}	2.4	-	$V_{CC} + 0.3$	V	
	V_{IL}	-0.3	-	0.45	V	
Output Voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -400 \mu A$
	V_{OL}	-	-	0.4	V	$I_{OL} = 2.1$ mA

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■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION
 $(V_{CC} = 5V \pm 5\%, V_{SS} = 0V, T_a = 0 \text{ to } 70^\circ\text{C})$
Test Conditions

- Input pulse levels: 0.45 / 2.4V
- Input rise and fall times: $\leq 10 \text{ ns}$
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

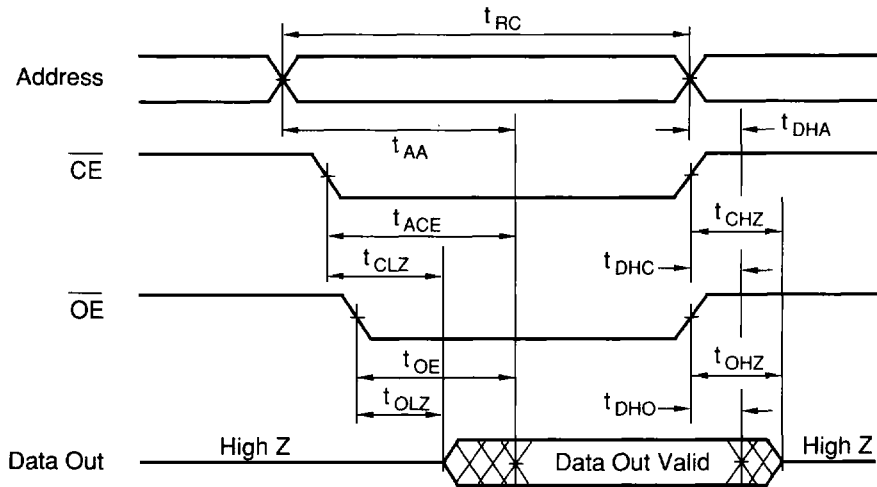
Item	Symbol	HN62444BN-12		Test Unit
		Min.	Max.	
Read Cycle Time	t_{RC}	120	-	ns
Burst Read Cycle Time	t_{BC}	70	-	ns
Address Access Time	t_{AA}	-	120	ns
Burst Address Access Time	t_{BA}	-	70	ns
Chip Enable Access Time	t_{ACE}	-	120	ns
Output Enable Access Time	t_{OE}	-	55	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	ns
Chip Enable to Output in High-Z ¹	t_{CHZ}	-	40	ns
Output Enable to Output in High-Z ¹	t_{OHZ}	-	40	ns
Chip Enable to Output in Low-Z	t_{CLZ}	5	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	5	-	ns

Note: 1. t_{CHZ}, t_{OHZ} are defined as the time at which the output becomes an open circuit and are not referred to output voltage levels.

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■ READ TIMING WAVEFORM

1) Normal Mode:

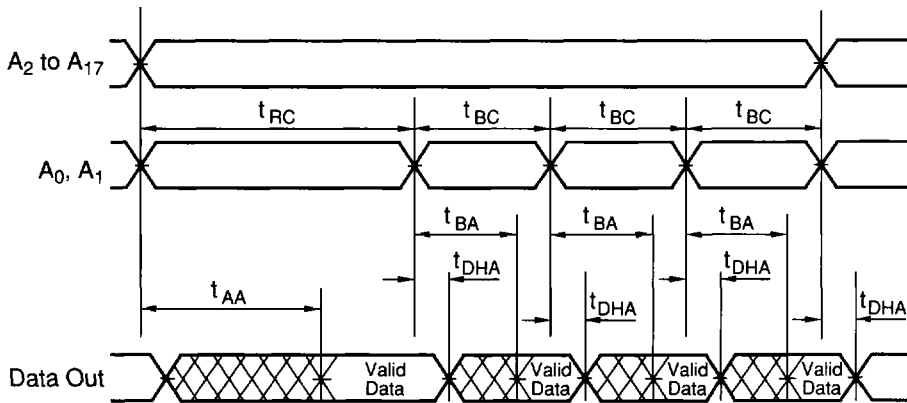


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- Note:
1. t_{DHA} , t_{DHC} , t_{DHO} are determined by the faster time.
 2. t_{AA} , t_{ACE} , t_{OE} are determined by the slower time.
 3. t_{CLZ} , t_{OLZ} are determined by the slower time.

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2) Fast Address Access Mode:



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Note: \overline{CE} and \overline{OE} are enabled.

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