Subscriber Line Interface Circuit (SLIC)

Key Features

- Designed to interface with Broadcom BCM3351 and BCM3352, FlexiVoice™ , cable modem circuit
- Differential Codec interface
- On-chip ringing generation
  - Balanced, up to 81 V_{Peak}
  - Any waveform
  - 5REN ringing load
  - Automatic gain control of ring signal (AGC-R)
  - Short circuit safe
- Low on-hook power consumption in Active State (65 mW @ V_{Bat} = -80 V)
- Automatic current controlled battery switching between on-hook battery (V_{Bat}) and talk battery (V_{TBat})
- Pulse metering and on-hook transmission
- UL-1950 and MTU compliant on-hook line voltage
- 3.3V compatible logic interface

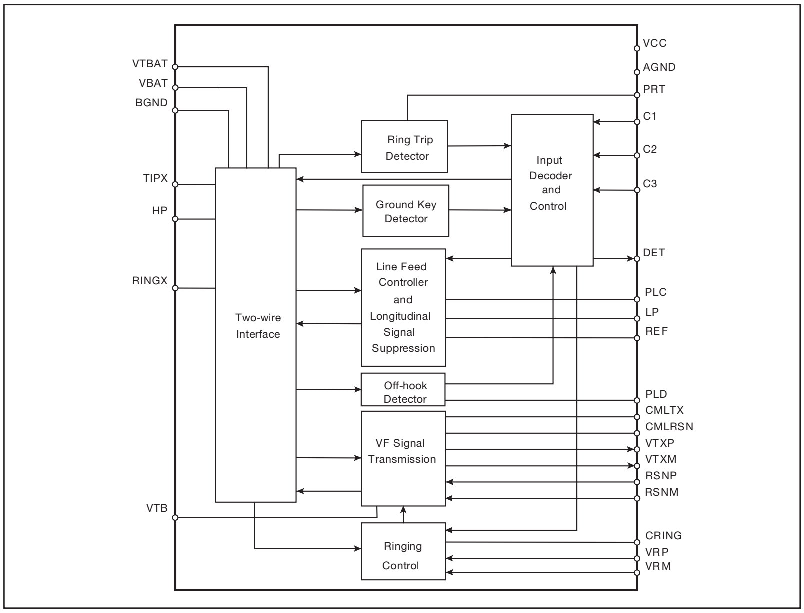


Figure 1. Block diagram.

Description

The ringing FlexiSLIC™ PBL 387 85/1 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit for use in short loop cable modem applications. The PBL 387 85/1 SLIC has been optimized for low power consumption, low total line interface cost and for a high degree of flexibility in various applications.

The PBL 387 85/1 SLIC supplies a balanced, sinewave or trapezoidal ringing signal of up to 81 V_{Peak} (85 V DC supply) to the subscriber line across a load of up to 5REN. The PBL 387 85/1 supplies programmable constant current to the subscriber loop, sourced from the talk battery. The On-Hook line voltage of 43 V to 56 V is derived from the battery. All battery switching is internal to the device and is automatic. To further reduce power consumption the automatic gain control for the ring signal (AGC-R) keeps the level always adjusted to the maximum, that can be sourced from the available battery.

The SLIC incorporates loop current and ring-trip detection functions. The PBL 387 85/1 is compatible with loop start and ground start signalling. Two- to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with Broadcom cable modem circuit BCM3352. The line terminating impedance and balance impedance is programmable and may be complex or real for worldwide compliance. The PBL 387 85/1 includes a differential codec interface. Longitudinal balance specifications and other device characteristics are in compliance with ITU-T requirements.

Tip and ring voltages are UL-1950 compliant; i.e. no two-wire line voltage exceeds 56 V. The PBL 387 85/1 SLIC is packaged in a surface mount 44-pin QSOP package.

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature, Humidity				
Storage temperature range	T_{Stg}	-55	+150	°C
Operating temperature range	T_{Amb}	-40	+110	°C
Operating junction temperature range, Note 1	T_J	-40	+140	°C
Power supply, $-40°C \le T_{Amb} \le +85°C$				
V_{CC} with respect to AGND	V_{CC}	-0.4	6.5	V
V_{TB} with respect to AGND	V_{TB}	V_{Bat}	0.4	V
V_{TBat} with respect to A/BGND	V_{TBat}	V_{Bat}	0.4	V
V_{Bat} with respect to BGND, continuous	V_{Bat}	-85	0.4	V
Power dissipation				
Continuous power dissipation at $T_{Amb} \le +85$ °C	P_D		1.5	W
Peak power dissipation @ $T_{Amb} = +85$ °C, t < 100 ms, $t_{Rep} > 1$ sec.	P_{PD}		4	W
Ground				
Voltage between AGND and BGND	V_G	-5	V_{CC}	V
Digital inputs, outputs (C1, C2, C3, DET)				
Input voltage	V_{ID}	-0.4	V_{CC}	V
Output voltage (DET not active)	V_{OD}	-0.4	3.3	V
Output current (DET)	I_{OD}		30	mA
Ring voltage, input (VRP, VRM)				
Input voltage	V_{RP} ,V_{RM}	-1.1	V_{CC}	V
TIPX and RINGX terminals, $-40°C \le T_{Amb} \le +85°C$, $V_{Bat} = -80$ V				
TIPX or RINGX current	I_{TIPX}, I_{RINGX}	-100	100	mA
TIPX or RINGX voltage, continuous (referenced to AGND)	V_{TA}, V_{RA}	V_{BAT}	2	V
TIPX or RINGX, pulse < 10 ms, $t_{Rep} > 10$ s, Note 2, Note 3	V_{TA}, V_{RA}	V_{BAT} –15	5	V
TIPX or RINGX, pulse < 1 µs, $t_{Rep} > 10$ s, Note 2, Note 3	V_{TA}, V_{RA}	V_{BAT} –20	10	V
TIP or RING, pulse < 250 ns, $t_{Rep} > 10$ s, Note 2 , Note 3	V_{TA}, V_{RA}	V_{BAT} –25	15	V

Notes, Maximum Ratings

1. The circuit includes thermal protection. Operation above max. junction temperature may degrade device reliability.
2. With the diodes D_B and D_{TB} included, see figure 9.
3. R_{F1} and $R_{F2} > 20\ \Omega$ is also required. Pulse is supplied to RING and TIP outside R_{F1} and R_{F2}.
4. The voltage of V_{TB} sets the maximum line length see figure 12. The diode D_{TB} is required see figure 9.

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{Amb}	-40	+85	°C
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{TB} with respect to A/BGND ,Note 4	V_{TB}	-32	-10	V
V_{Bat} with respect to BGND	V_{Bat}	-80		V
V_{CMLTX}	V_{CMLTX}	-0.1	2	V
V_{CMLRSN}	V_{CMLRSN}	-0.1	2	V

Electrical Characteristics

-40 °C ≤ T_{Amb} ≤ +85 °C, V_{CC} = +5 V ±5 %, V_{TBat} = -32 V to -10 V, V_{Bat} = -80 V, -0.1V ≤ V_{CMLTX} ≤ 2 V, V_{CMLRSN}= 0 V, V_R = 0.81 Vpk, R_{LC}= 18.7 kΩ, (I_L = 26.8 mA), Z_L = 600 Ω, R_{LD} = 49.9 kΩ, R_{F1} = R_{F2} = 0 , R_{Ref} = 15.0 kΩ, R_{RT} = 66.5 kΩ, C_{HP} = 33 nF, C_{LP}= 0.47 µF, R_{TP} = R_{TM} = 120 kΩ, R_{RXP} = R_{RXM} = 120 kΩ.
Current definition: current is positive if flowing into a pin unless stated otherwise. Active state includes active normal state unless otherwise specified.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}		Active state				
Off-Hook, I_{LDC} ≥ 10 mA	2	1% THD, Note 1	1.0			V_{Peak}
On-Hook, I_{LDC} ≤ 5 mA			1.0			V_{Peak}
Metering, I_{LDC} ≥ 10 mA		Z_{LM} = 200 Ω, f = 16 kHz		0.7		V_{Peak}
Input impedance, Z_{TRX}		Note 2		Z_T/200		Ω
Longitudinal impedance, Z_{LOT}, Z_{LOR}		0 < f < 100 Hz		20	35	Ω/wire
Longitudinal current limit, I_{LOT}, I_{LOR}		active state	12			mA_{rms} /wire
Longitudinal to metallic balance, B_{LM}		IEEE standard 455-1985, ZTRX = 736 Ω				
		0.2 kHz < f < 1.0 kHz	53	70		dB
		1.0 kHz < f < 3.4 kHz	53	70		dB
Longitudinal to metallic balance, B_{LME}	3	active state				
$B_{LME} = 20 \times \text{Log}\left\lvert\frac{E_{LO}}{V_{TR}}\right\rvert$		0.2 kHz ≤ f ≤ 1.0 kHz	53	70		dB
		1.0 kHz < f < 3.4 kHz	53	70		dB
Longitudinal to four-wire balance, B_{LFE}	3	active state				
$B_{LFE} = 20 \times \text{Log}\left\lvert\frac{E_{LO}}{V_{TX}}\right\rvert$		0.2 kHz ≤ f ≤ 1.0 kHz	53	70		dB
		1.0 kHz < f < 3.4 kHz	53	70		dB
Metallic to longitudinal balance, B_{MLE}	4	active state				
$B_{MLE} = 20 \times \text{Log}\left\lvert\frac{V_{TR}}{V_{LO}}\right\rvert$, $E_{RX} = 0$		0.2 kHz < f < 3.4 kHz	40	58		dB

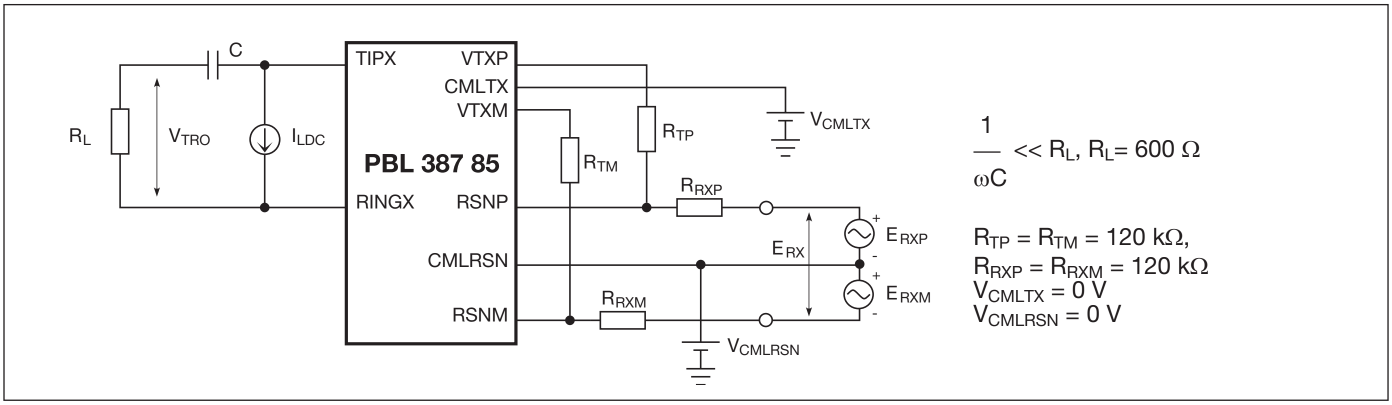


Figure 2. Overload level, V_{TRO}, two-wire port.

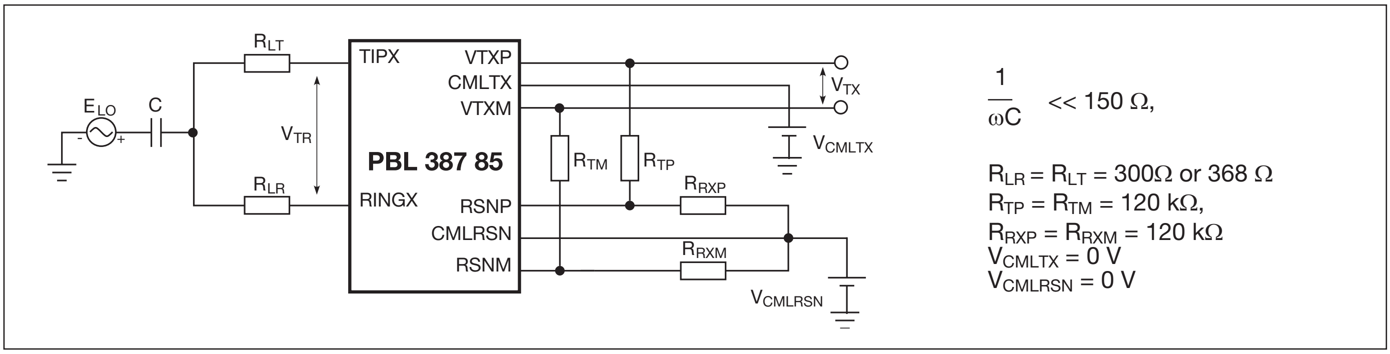
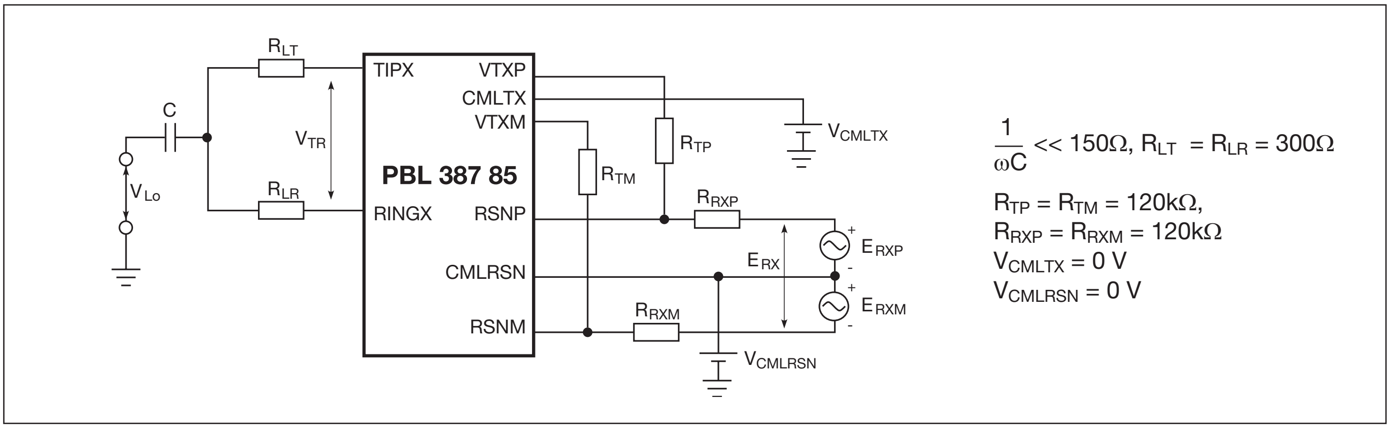


Figure 3. Longitudinal to metallic, B_{LME}, and Longitudinal to four-wire, B_{LFE}, balance.

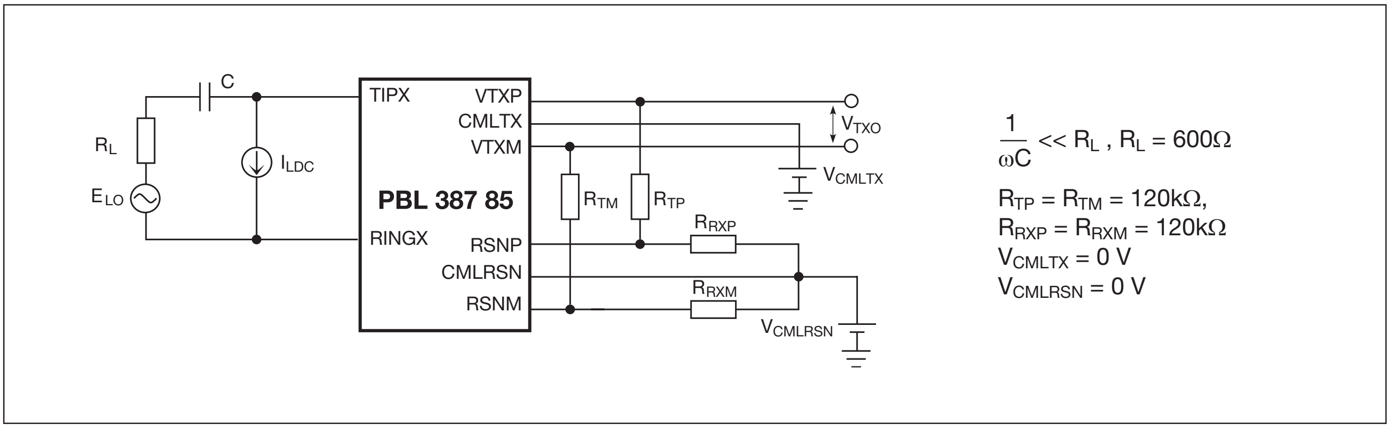
Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to longitudinal balance, B_{FLE} $B_{FLE} = 20 \times \text{Log}\left\|\frac{E_{RX}}{V_{Lo}}\right\|$	4	active state 0.2 kHz < f < 3.4 kHz	40	58		dB
Two-wire return loss, r $r = 20 \times \text{Log}\frac{\|Z_{TRX} + Z_L\|}{\|Z_{TRX} - Z_L\|}$		0.2 kHz < f < 0.5 kHz 0.5 kHz < f < 1.0 kHz 1.0 kHz < f < 3.4 kHz, Note 3	25 27 23			dB dB dB
TIPX idle voltage, V_{TI}		active normal, $I_L = 0$		- 0.9		V
RINGX idle voltage, V_{RI}		active normal, $I_L = 0$		- 51		V
Open loop voltage, $\|V_{TR\ Open}\|$		active, $I_L = 0$	43	50	56	V
Four-wire transmit port (differential outputs VTXP and VTXM)						
Overload level, V_{TXPO}, V_{TXMO} Off-hook, $I_L \geq$ 10mA On-hook, $I_L \leq$ 5mA	5	 Load impedance > 20 kΩ, Differential load impedance > 40 kΩ, 1% THD, Note 4	 0.5 0.5			 V_{Peak} V_{Peak}
Output offset voltage, ΔV_{TXP}, ΔV_{TXM}, from nominal V_{CMLTX}			-60		60	mV
Differential output offset voltage, $\Delta V_{TXP} + \Delta V_{TXM}$			-120		120	mV
Nominal output dc voltage, V_{TXPdc}, V_{TXMdc}		Note 5.		V_{CMLTX}		V
Transmit common mode control voltage, V_{CMLTX}		Note 5.	-0.1		2	V
Output impedance, z_{TXP}, z_{TXM}		0.2 kHz < f < 3.4 kHz		5	20	Ω
Differential output impedance, $z_{TXP} + z_{TXM}$		0.2 kHz < f < 3.4 kHz		10	40	Ω
CMLTX to VTX suppression		f = 1 kHZ		70		dB
CMLTX to VTX suppression		f = 500 kHZ		40		dB



$\frac{1}{\omega C} << 150\Omega$, $R_{LT} = R_{LR} = 300\Omega$

$R_{TP} = R_{TM} = 120k\Omega$,
$R_{RXP} = R_{RXM} = 120k\Omega$
$V_{CMLTX} = 0$ V
$V_{CMLRSN} = 0$ V

Figure 4. Metallic to longitudinal, B_{MLE} and four-wire to longitudinal balance, B_{FLE}.

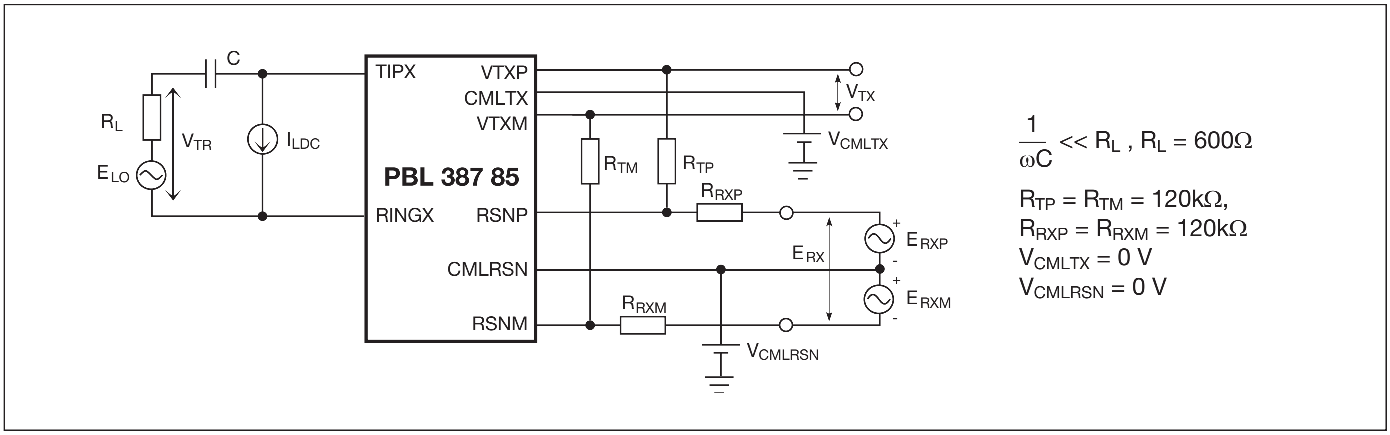


$\frac{1}{\omega C} << R_L$, $R_L = 600\Omega$

$R_{TP} = R_{TM} = 120k\Omega$,
$R_{RXP} = R_{RXM} = 120k\Omega$
$V_{CMLTX} = 0$ V
$V_{CMLRSN} = 0$ V

Figure 5. Overload level, V_{TXO}, four-wire transmit port.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire receive port (receive summing node = RSN; differential inputs RSNP and RSNM)						
RSNP, RSNM dc offset voltage, V_{RSNMdc}, V_{RSNPdc} from nominal V_{CMLRSN}		I_{RSN} = 0 mA	-25		25	mV
Differential RSNP, RSNM dc voltage, ΔV_{RSNP-M}		I_{RSN} = 0 mA	-50		50	mV
Receive common mode control voltage, V_{CMLRSN}		Note 6.	-0.1		2	V
RSNP, RSNM impedance		0.2 kHz < f < 3.4 kHz		10	50	Ω
Differential RSNP, RSNM impedance		0.2 kHz < f < 3.4 kHz		20	100	Ω
RSNP current, I_{RSNP}, to metallic loop current ,I_L, gain, α_{RSNP}		0.3 kHz < f < 3.4 kHz		400		ratio
RSNM current, I_{RSNM}, to metallic loop current ,I_L, gain, α_{RSNM}		0.3 kHz < f < 3.4 kHz		400		ratio
Differential RSN current, $(I_{RSNP} – I_{RSNM})/2$, to metallic loop current(I_L) gain, α_{RSNPM}		0.3 kHz < f < 3.4 kHz		800		ratio
CMLRSN to VTX suppression		f = 1 kHz		63		dB
CMLRSN to VTX suppression		f = 500 kHz		34		dB
Frequency response						
Two-wire to four-wire, g_{2-4}	6	relative to 0 dBm, 1.0 kHz. E_{RX} = 0 V 0.3 kHz < f < 3.4 kHz f = 8.0 kHz, 12 kHz, 16 kHz	 -0.15 -0.5	 -0.1	 0.15 0.1	 dB dB
Four-wire to two-wire, g_{4-2}	6	relative to 0 dBm, 1.0 kHz. E_{LO} = 0 V 0.3 kHz < f < 3.4 kHz f = 8 kHz, 12 kHz, 16 kHz	 -0.15 -1.0 -1.0	 -0.2 -0.3	 0.15 0 0	 dB dB dB
Four-wire to four-wire, g_{4-4}	6	relative to 0 dBm, 1.0 kHz. E_{LO} = 0 V 0.3 kHz < f < 3.4 kHz	 -0.15		 0.15	 dB
Insertion loss						
Two-wire to four-wire, G_{2-4} $G_{2-4} = 20 \times \text{Log} \left\lvert \frac{V_{TX}}{V_{TR}} \right\rvert ,E_{RX} = 0$	6	0 dBm, 1.0 kHz, Note 7	-6.22	-6.02	-5.82	dB
Four-wire to two-wire, G_{4-2} $G_{4-2} = 20 \times \text{Log} \left\lvert \frac{V_{TR}}{E_{RX}} \right\rvert ,E_{LO} = 0$	6	0 dBm, 1.0 kHz, Notes 7, 8	-0.2		0.2	dB



$\frac{1}{\omega C} << R_L$, $R_L = 600\Omega$

$R_{TP} = R_{TM} = 120k\Omega$,
$R_{RXP} = R_{RXM} = 120k\Omega$
$V_{CMLTX} = 0$ V
$V_{CMLRSN} = 0$ V

Figure 6. Frequency response, insertion loss, gain tracking.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Gain tracking						
Two-wire to four-wire $R_{LDC} \leq 2k\Omega$	6	Ref. -10 dBm, 1.0 kHz, Note 9				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Four-wire to two-wire $R_{LDC} \leq 2k\Omega$	6	Ref. -10 dBm, 1.0 kHz, Note 9				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Noise						
Idle channel noise at two-wire port (TIPX-RINGX)		C-message weighting		7	12	dBrnC
		Psophometrical weighting		-83	-78	dBmp
		Note 10				
Harmonic distortion						
Two-wire to four-wire	6	0 dBm, 1.0 kHz test signal			-50	dB
Four-wire to two-wire		0.3 kHz < f < 3.4 kHz			-50	dB
Battery feed characteristics						
Constant loop current, I_{LConst}		$R_{LC} = \frac{500}{I_{LProg}} - \frac{10.4\times\ln(32\times I_{LProg})}{I_{LProg}}$ $18 < I_{LProg} < 30$ mA	$0.95\times I_{LProg}$	I_{LProg}	$1.05\times I_{LProg}$	mA
Loop current detector						
Programmable threshold, I_{LTh}		$I_{LTh} = \frac{500}{R_{LD}}$, $I_{LTh} > 10$ mA	$0.9\times I_{LTh}$	I_{LTh}	$1.1\times I_{LTh}$	mA
Ringing						
V_{RP}/V_{RM} input impedance			50			MΩ
Input bias current V_{RP}/V_{RM}				7		nA
Common mode voltage V_{RP}/V_{RM}			-0.1		2	V
Common mode suppression V_{RP}/V_{RM}				45		dB
V_R input voltage ($V_{RP} - V_{RM}$)				0.81		V_{Peak}
Ring injection suppression		Active state, $R_L = 600\ \Omega$		100		dB
Differential ringing gain		V_R to two-wire, Note 11		94		ratio
Ringing voltage total distortion		$R_L = 1.4\ k\Omega - 40\ k\Omega$, 25 Hz, Note 11		0.4	2	%
Voltage offset TIPX and RINGX		$\lvert V_{BAT}\rvert/2 + 0.65$, Note 11	-3	0	3	V
Common mode voltage TIPX and RINGX		$\lvert V_{BAT}\rvert/2 + 0.65$	-0.4	0	0.4	V
Ring-trip detector						
Ring-trip current threshold, I_{LRTh}		Note 12	$0.92\times I_{LRTh}$	I_{LRTh}	$1.08\times I_{LRTh}$	mA
Loop voltage measurement						
Frequency		$f = \frac{10^6}{\lvert V_{TR}\rvert + 1}$		f		Hz
Ground fault detector						
Ground fault detector threshold			11	15	19	mA
Digital inputs (C1, C2, C3)						
Input low voltage, V_{IL}			0		0.5	V
Input high voltage, V_{IH}			2.5		V_{CC}	V
Input low current, $\lvert I_{IL}\rvert$		$V_{IL} = 0.5$ V	-200			µA
Input high current, $\lvert I_{IH}\rvert$		$V_{IH} = 2.5$ V	-100			µA

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Detector output (DET)						
Output low voltage, V_{OL}		I_{OL} = 1 mA		0.1	0.6	V
Output high voltage, V_{OH}			3.1	3.3	3.5	V
Internal pull-up resistor to V_{CC}				10		kΩ
Internal pull-down resistor to GND				20		kΩ
Power dissipation (V_{Bat} -80 V, V_{TBat} = -24 V note 13)						
P_1		Open circuit state		16		mW
P_2		Active state Longitudinal current = 0 mA, I_L = 0 mA		65		mW
P_3		Active state, R_L = 300 Ω (Off-hook)		0.50		W
P_4		Active state, R_L = 600 Ω (Off-hook)		0.29		W
P_5		Ringing state, R_L = 7 kΩ (ac load ≈ 1 REN) Sine wave, 20 Hz, max. amplitude		0.36		W
Power supply currents (V_{Bat} = -80 V)						
V_{CC} current, I_{CC}		Open circuit state		1.4		mA
V_{TBat} current, I_{TBat}		Open circuit state		0		mA
V_{TB} current, I_{TB}		Open circuit state		-0.13		mA
V_{Bat} current, I_{Bat}		Open circuit state		-0.07		mA
V_{CC} current, I_{CC}		Active state, On-hook		2.4		mA
V_{TBat} current, I_{TBat}		Active state, On-hook		0		mA
V_{TB} current, I_{TB}		Active state, On-hook		-0.2		mA
V_{Bat} current, I_{Bat}		Active state, On-hook		-0.6		mA
V_{CC} current, I_{CC}		Ringing state, On-hook, No ring signal		7.1		mA
V_{TBat} current, I_{TBat}		Ringing state, On-hook, No ring signal		0		mA
V_{TB} current, I_{TB}		Ringing state, On-hook, No ring signal		-1		mA
V_{Bat} current, I_{Bat}		Ringing state, On-hook, No ring signal		-2.7		mA
Power supply rejection ratios						
V_{CC} to 2-wire port		Active State f = 1 kHz, V_n = 100 mV	30	45		dB
V_{CC} to 4-wire port		Active State f = 1 kHz, V_n = 100 mV	36	51		dB
V_{TB} to 2-wire port		Active State f = 1 kHz, V_n = 100 mV	28.5	60		dB
V_{TB} to 4-wire port		Active State f = 1 kHz, V_n = 100 mV	34.5	66		dB
V_{Bat} to 2-wire port		Active State f = 1 kHz, V_n = 100 mV	40	60		dB
V_{Bat} to 4-wire port		Active State f = 1 kHz, V_n = 100 mV	46	66		dB
Temperature guard						
Junction threshold temperature, T_{JG}				155		°C
Thermal Resistance						
Junction to pin, Θ_{JP}				22		°C/W
Junction to ambient, Θ_{JA}				42.8		°C/W

Notes, Electrical characteristics

1. The overload level is automatically expanded to needed signal level, maximum 1.7 V_{Peak} when the signal level is > 1.0 V_{Peak} , and is specified at the two-wire port with the signal source at the four-wire receive port. For more information see section Adaptive overhead voltage.
2. The two-wire impedance is programmable by selection of external component values according to:
   $Z_{TRX} = Z_T/(|G_{2\text{-}4S} \times \alpha_{RSN}|)$

   where:

   Z_{TRX} = impedance between the TIPX and RINGX terminals

   $Z_T = Z_{TP} = Z_{TM}$ = programming network between the VTXP and RSNP, VTXM and RSNM terminals

   $G_{2\text{-}4S}$ = transmit gain, nominally = 0.5

   $\alpha_{RSN} = \alpha_{RSNP} = \alpha_{RSNM}$ =
   = receive current gain, nominally 400 (current defined as positive flowing into the receive summing node, RSNP, and when flowing from ring to tip)
   See section Transmission.
3. Higher return loss values can be achieved by adding a reactive component to Z_{TP}, Z_{TM} ,the two-wire terminating impedance programming resistances, e.g. by dividing Z_{TP}, Z_{TM}, into two equal halves and connecting capacitors from the common points to ground.
4. The overload level is automatically expanded as needed up to 1.25 V_{Peak} (using the AOV function) when the signal level >0.5 V_{Peak} and is specified at the four-wire transmit port, (V_{TXP}, V_{TXM}) with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2\text{-}4S} = 0.5$.
5. The output dc voltage, V_{TXPdc}, V_{TXMdc}, is set by the voltage applied to pin CMLTX, V_{CMLTX}.
6. The dc voltage on pins RSNM and RSNP is set by the voltage applied to pin CMLRSN, V_{CMLRSN}
7. Secondary protection resistors R_{F1} and R_{F2} impact the insertion loss (refer to section Transmission). The specified insertion loss is for $R_{F1} = R_{F2} = 40\Omega$.
8. The specified insertion loss tolerance does not include errors caused by external components.
9. The level is specified at the four-wire receive port (E_{RXP}, E_{RXM}, figure 6) and referenced to a 600 Ω impedance level.
10. The two-wire idle noise is specified with the four-wire receive port grounded ($E_{RXP} = E_{RXM} = 0$, figure 6). The four-wire idle noise at VTXP, VTXM is the two-wire value reduced by 6 dB and is specified with the two-wire port terminated in 600 Ω (R_L). The VTXP, VTXM noise specification is referenced to a 600 Ω impedance level.
11. PBL 387 85 contains an Automatic Gain Control Ringing (AGC-R) unit. This unit controls the Gain in the ringing loop to keep an undistorted ringing signal due to variation in V_{BAT}, V_{RP}/V_{RM} input signal amplitude and Voltage offset. For more information see section Ringing further on.
12. See section Calculation of the ring-trip threshold for information about this.
13. The V_{TBAT} voltage is optimized for $R_L = 600\ \Omega$, $I_L = 26.8$ mA, no metering signal, $R_F = 40$ and the current controlled battery switch. See section Optimizing V_{TB} for further information.

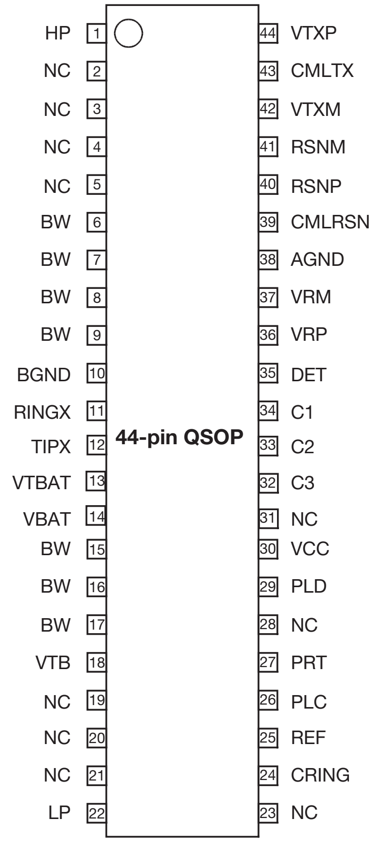


Figure 8. Pin configuration 44L-QSOP, top view.

Pin Description

Pin	Symbol	Description
1	HP	**H**igh **P**ass AC/DC separation capacitor C_{HP} connects between this pin and TIPX.
2	NC	**N**o **C**onnect. Must be left open.
3	NC	**N**o **C**onnect. Must be left open.
4	NC	**N**o **C**onnect. Must be left open.
5	NC	**N**o **C**onnect. Must be left open.
6	BW	**B**at**w**ing (refer to Note, Pin Description)
7	BW	**B**at**w**ing (refer to Note, Pin Description)
8	BW	**B**at**w**ing (refer to Note, Pin Description)
9	BW	**B**at**w**ing (refer to Note, Pin Description)
10	BGND	**B**attery **G**rou**nd**. Shall be tied together with AGND.
11	RINGX	The RINGX pin connects to the ring lead of the two-wire interface via over voltage protection components (and optional test access switch).
12	TIPX	The TIPX pin connects to the tip lead of the two-wire interface via over voltage protection components (and optional test access switch).
13	VTBAT	**T**alk **Bat**tery. The dc loop current is supplied to TIPX and RINGX from this battery voltage. Negative with respect to BGND.
14	VBAT	On-hook Ringing Battery supply voltage. Negative with respect to BGND.
15	BW	**B**at**w**ing (refer to Note, Pin Description)
16	BW	**B**at**w**ing (refer to Note, Pin Description)
17	BW	**B**at**w**ing (refer to Note, Pin Description)
18	VTB	Internal SLIC bias voltage. Connected to the talk battery supply. Refer to the application diagram in figure 9. May be connected to any voltage between V_{BAT} and –10 V.

19	NC	**N**o **C**onnect. Must be left open.
20	NC	**N**o **C**onnect. Must be left open.
21	NC	**N**o **C**onnect. Must be left open.
22	LP	**L**ow **P**ass saturation guard filter capacitor C_{LP} connects between this pin and VTBAT to filter out noise and improve PSRR.
23	NC	**N**o **C**onnect. Must be left open.
24	CRING	The capacitor C_{RING} connects between this pin and AGND. Required for the ring signal generation.
25	REF	A 15 kΩ resistor connected between this pin and AGND sets an internal SLIC reference current. The value must not be changed.
26	PLC	**P**rogrammable **L**ine **C**urrent. The constant current DC feed is programmed by a resistor connected from this pin to AGND.
27	PRT	**P**rogrammable **R**ing-**t**rip Resistor RRT connected between this pin and AGND. Sets the ring-trip threshold. The capacitor C_{RT} together with resistor R_{RT} filters the ring-trip detector.
28	NC	**N**o **C**onnect. Must be left open.
29	PLD	**P**rogrammable **L**oop **D**etector threshold. The loop detection threshold is programmed by a resistor, R_{LD}, connected between this pin and AGND.
30	VCC	+5 V power supply.
31	NC	**N**o **C**onnect. Must be left open.
32	C3	C1, C2, C3 are digital inputs, which control the SLIC operating states. Refer to table 1 for details.
33	C2	
34	C1	
35	DET	**Det**ector output. Active low when indicating loop or ring-trip detection, active high when indicating ground key detection.
36	VRP	Low **v**oltage **r**ingsignal input (**p**lus).
37	VRM	Low **v**oltage **r**ingsignal input (**m**inus).
38	AGND	**A**nalog **G**rou**nd**, shall be tied together with BGND.
39	CMLRSN	**C**ommon **M**ode **L**evel **R**eceive **S**umming **N**ode. External reference voltage, which sets the dc bias for RSNM and RSNP.
40	RSNP	**R**eceive **S**umming **N**ode **P**lus. 400 times the current flowing out of this pin equals the metallic (transversal) current flowing from RINGX to TIPX. Programming networks for two-wire impedance and receive gain connect to the receive summing node.
41	RSNM	**R**eceive **S**umming **N**ode **M**inus. 400 times the current flowing into this pin equals the metallic (transversal) current flowing from RINGX to TIPX. Programming networks for two-wire impedance and receive gain connect to the receive summing node.
42	VTXM	**T**ransmit vf output, **m**inus. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced at VTXM with a gain of -0.25. The two-wire impedance programming network connects between VTXM and RSNM. The ac voltage at VTXM is at opposite phase compared to the ac signal at VTXP.
43	CMLTX	**C**ommon **M**ode **L**evel **T**ransmit. External voltage source (e.g. BCM 3352), which sets the dc bias level for VTXP and VTXM.
44	VTXP	**T**ransmit vf output, **p**lus. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced at VTXP with a gain of 0.25. The two-wire impedance programming network connects between VTXP and RSNP. The ac voltage at VTXP is at opposite phase compared to the ac signal at VTXM.

Note: A batwing is a package pin, which provides a low thermal resistance path to the silicon chip via the lead frame. By soldering the batwing pins to PCB copper foil the device can be efficiently cooled. Note that batwing pins are at the same voltage as the VBAT pin (substrate voltage).

SLIC Operating States

State	C3	C2	C1	SLIC Operating State	Active detector (DET response)
0	0	0	0	TIPX & RINGX open circuit	No active detector (DET is set high)
1	0	0	1	Ringing	Ring-trip detector (DET active low)
2	0	1	0	Active	Loop current detector (DET active low)
3	0	1	1	Active	Loop voltage measurement (DET pulse train)
4	1	0	0	Not applicable	—
5	1	0	1	Active	Ground key detector and loop ground fault detector (DET active high)
6	1	1	0	Not applicable	—
7	1	1	1	Not applicable	—

Table 1. SLIC operating states.

Functional Description and Applications Information

Introduction

The application diagram, figure 9, shows the PBL 387 85/1 SLIC in a cable modem application with the Broadcom BCM 3352 circuit. Due to the low 3.3 V BCM 3352 supply voltage it is necessary to utilize a differential interface to transmit the voice signal between the PBL 387 85/1 SLIC and the BCM 3352 with sufficient dynamic range and amplitude. Additionally the differential interface helps in suppressing common mode noise that is generated within the BCM 3352 circuit. The low voltage ring signal, which is generated by the BCM 3352, is also connected to the SLIC via a differential interface.

The codec function resides within the BCM 3352 circuit. Hybrid balance filter, transmit and receive gain can be set via software control within the BCM 3352. Ringing frequency and amplitude is also controlled by the BCM 3352. The BCM 3352 can adjust the low voltage ringing signal into the SLIC VRP and VRM pins such that the two-wire ringing voltage will include a dc bias.

The CML output of the BCM3352 connects to CMLTX and sets the common mode dc level of the VTXP and VTXM.

R_{F1}, R_{F2} and the clamp “OVP” make up the overvoltage protection network.

C_{TC} and C_{RC} clamp fast transients that may bypass the OVP clamp and also filter high frequency interference (RFI filter).

C_{HP} and C_{LP} are coupling capacitors within two SLIC feedback loops that control SLIC battery feed and SLIC voice frequency transmission.

C_{TB}, C_B are power supply bypass capacitors.

D_{TB} is a diode that is part of the battery switching function.

D_B prevents reverse currents from the VB supply rail during application of negative over voltages.

D_{BB} is normally reverse biased, but conducts supply VTB to the VBAT terminal in case the voltage VB should fail.

R_{TP} and R_{TM} set the two-wire impedance. Complex termination impedance can be achieved by replacing R_{TM} and R_{TP} with complex networks.

R_1, R_2, R_3 set the “base” transmit gain. The BCM 3352 codec provides further software transmit gain control.

R_{RXM} and R_{RXP} set the “base” receive gain. The BCM 3352 codec provides further software receive gain control.

R_4 and C_4 filter the common mode level, CML, reference voltage that connects to CMLTX.

C_1, C_2, C_3, C_5, C_6, C_7 provide filtering for the BCM3352 transmit and receive differential inputs and outputs.

C_8 and C_9 provide filtering/integration for the BCM3352 differential pulse width modulated low voltage ringing signal output.

R_{LD} sets the loop current detector threshold.

R_{LC} sets the constant dc loop current.

R_{REF} sets a SLIC reference current (must be 15.0 kΩ, 1% as specified).

R_{RT} sets the ring-trip detector current threshold.

C_{RT} filters the ring-trip detector.

C_{RING} is used for the high voltage ringing signal generation.

V_{TB} is the talk battery supply, i.e. the negative supply voltage that sources the loop current.

V_B is the ringing battery, i.e. the negative supply voltage that is used to power the SLIC while ringing the line. This battery is also used to provide the On-Hook voltage.

Design support tools

The following design support tools are available for the PBL 387 85/1:

- Test board, TB 216
- Pspice model of PBL 387 85/1

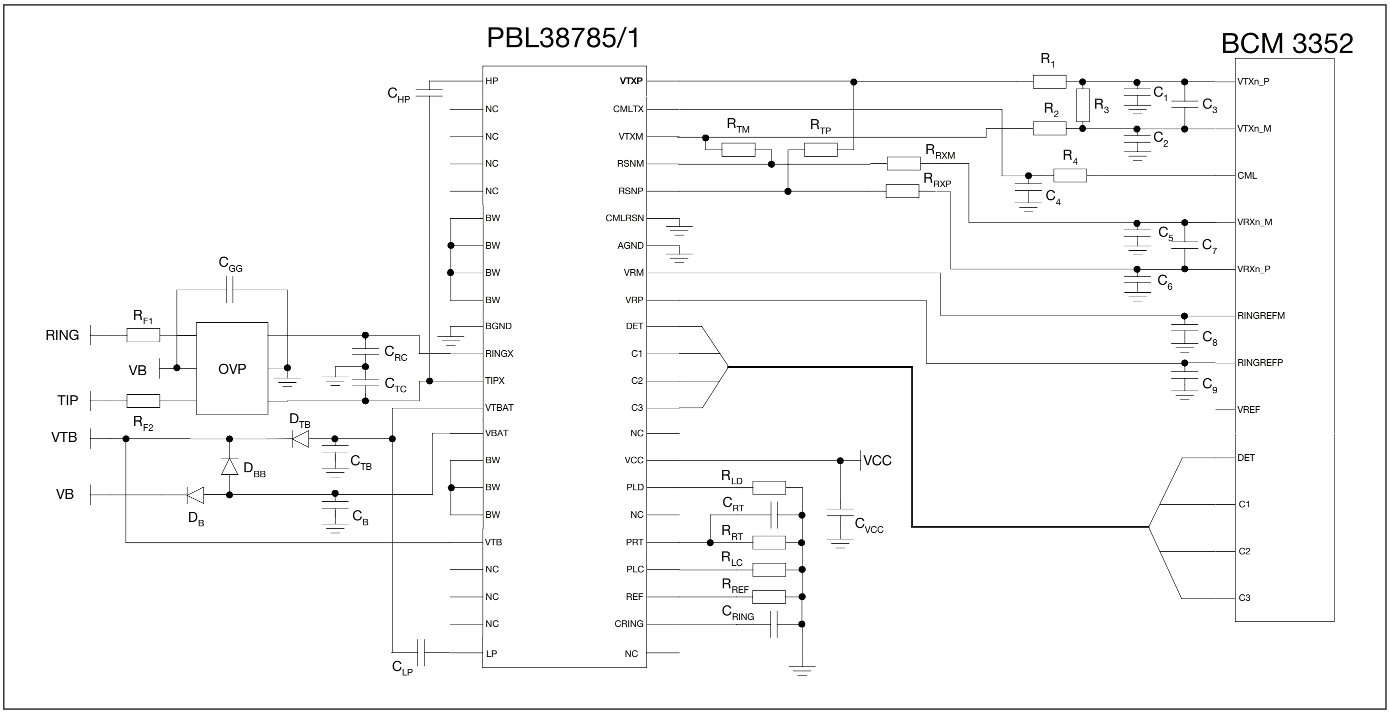


Figure 9. Single channel subscriber line interface with PBL 387 85/1 and Broadcom BCM3352 cable modem circuit.

PBL 387 85/1 components

RESISTORS :

(values according to IEC-63 E96 series)

R_{LD} = 49.9 kΩ 1% 1/10 W

R_{LC} = 18.7 kΩ 1% 1/10 W

R_{RT} = 61.9 kΩ 1% 1/10 W @ V_{BAT} = 80 V

R_{REF} = 15 kΩ 1% 1/10 W

$R_{TM} = R_{TP}$ = 105 kΩ 1% 1/10 W (for 600 Ω two-wire impedance with the R_{F1} and R_{F2} included.)

$R_{RXM} = R_{RXP}$ = 105 kΩ 1% 1/10 W (The gain is set to 1)

$R_{F1} = R_{F2}$ = Line protection resistor, 40Ω 1% match, e.g. by Bourns TBD

CAPACITORS:

(values according to IEC-63 E6 series)

C_{TB} = 150 nF 100 V 20%

C_{B} = 100 nF 100 V 20%

C_{VCC} = 100 nF 10 V 20%

C_{HP} = 33 nF 100 V 20%

C_{LP} = 470 nF 100 V 20%

C_{GG} = 220 nF 100 V 20%

C_{RING} = 470 nF 10 V 20 %

C_{RT} = 10 nF 10 V 20 %

OPTIONAL CAPACITORS:

C_{TC} = 1.0 nF 100 V 20%

C_{RC} = 1.0 nF 100 V 20%

DIODES:

$D_B = D_{TB} = D_{BB}$ =TBD

BCM 3352 components

RESISTORS:

(values according to IEC-63 E96 series)

R_1 = 20 kΩ 1% 1/10 W

R_2 = 20 kΩ 1% 1/10 W

R_3 = DNP kΩ 1% 1/10 W

R_4 = 10 kΩ 1% 1/10 W

CAPACITORS:

(values according to IEC-63 E6 series)

C_1 = 150 pF 10 V 10%

C_2 = 150 pF 10 V 10%

C_3 = 150 pF 10 V 10%

C_4 = 100 nF 10 V 10%

C_5 = 3.3 nF 10 V 10%

C_6 = 3.3 nF 10 V 10%

C_7 = 3.3 nF 10 V 10%

C_8 = 68 nF 10 V 10%

C_9 = 68 nF 10 V 10%

OVP:

Secondary protection clamp (e.g. Bourns/Power Innovations TISP PBL3 or TISP 6NTP2A ,which serves two lines).
The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferably to a ground plane.

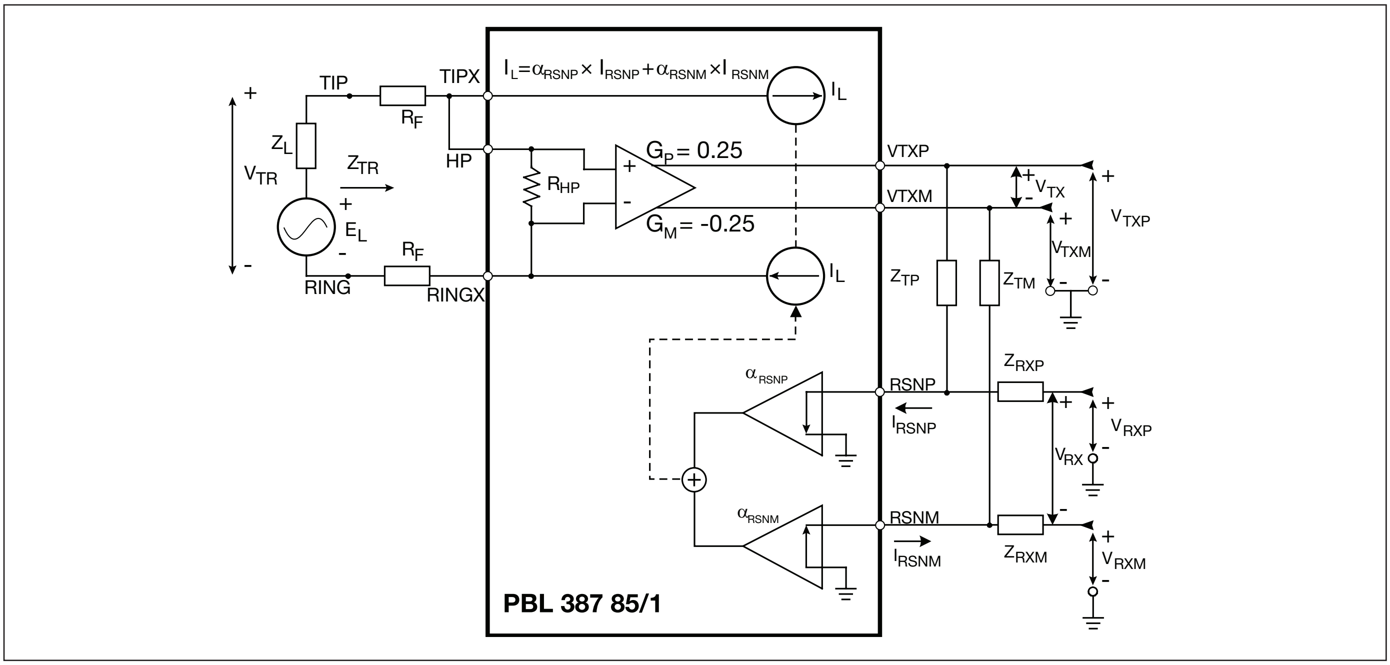


Figure 10. Simplified AC model of PBL 387 85/1.

Transmission

General

A simplified ac model of the transmission circuit is shown in figure 10. Circuit analysis yields:

$$V_{TR} = \frac{V_{TXP} - V_{TXM}}{G_{2\text{-}4S}} + I_L \times 2RF \tag{1}$$

$$I_L = \alpha_{RSNP} \times \left(\frac{V_{TXP}}{Z_{TP}} + \frac{V_{RXP}}{Z_{RXP}}\right) - \alpha_{RSNM} \times \left(\frac{V_{TXM}}{Z_{TM}} + \frac{V_{RXM}}{Z_{RXM}}\right) \tag{2a}$$

Assuming

$\alpha_{RSNP} = \alpha_{RSNM} = \alpha_{RSN}$
$Z_{TP} = Z_{TM} = Z_T$
$Z_{RXP} = Z_{RXM} = Z_{RX}$

Equation 2a reduces to:

$$\frac{I_L}{\alpha_{RSN}} = \frac{V_{TXP} - V_{TXM}}{Z_T} + \frac{V_{RXP} - V_{RXM}}{Z_{RX}} \tag{2b}$$

$$V_{TR} = E_L - I_L \times Z_L \tag{3}$$

where:

V_{TX}	is the non-ground referenced ac metallic voltage between the V_{TXP} and V_{TXM} terminals.
V_{TXP}/V_{TXM}	analog output from the SLIC 4-wire output. P is the positive and M is the negative balanced input signal.
V_{TR}	is the ac metallic voltage between tip and ring.
E_L	is the line open circuit ac metallic voltage.
I_L	is the ac metallic current.
R_F	is a line over voltage protection resistor.
$G_{2\text{-}4S}$	is the SLIC two-wire to four-wire gain (transmit direction) with a nominal value of 0.5.
G_P/G_M	are the SLIC two-wire to four-wire gain (transmit direction) for positive (P) and negative (M) outputs respectively. $\lvert G_P \rvert + \lvert G_M \rvert = \lvert G_{2\text{-}4S} \rvert$
Z_L	is the total line impedance
Z_{RX}	controls four- to two-wire gain.
Z_{RXP}/Z_{RXM}	control four- to two-wire gain.
Z_T	determines the SLIC TIPX to RINGX ac impedance for signals at voice frequencies.
Z_{TP}/Z_{TM}	determine the SLIC TIPX to RINGX ac impedance for signals at voice frequencies.
V_{RX}	is the non-ground referenced ac metallic voltage between the V_{RXP} and V_{RXM} terminals.
V_{RXP}/V_{RXM}	analog speech input signal from CODEC/filter or signal generator. P is the positive and M is the negative balanced input signal.
α_{RSN}	is the receive summing node current to metallic loop current gain. $\alpha_{RSN} = 400$
$\alpha_{RSNP}/\alpha_{RSNM}$	are the receive summing nodes current to metallic loop current gain. $\alpha_{RSNP} = \alpha_{RSNM} = 400$
R_{HP}	internal resistor, approx. 400 kΩ

Two-Wire Impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the line protection resistors R_F , let $V_{RXP} = V_{RXM} = 0$.

From (1) and (2):

$$Z_{TR} = \frac{Z_T}{\alpha_{RSN} \times G_{2\text{-}4S}} + 2RF \tag{4}$$

Thus with Z_{TR}, $G_{2\text{-}4S}$, α_{RSN} and R_F known:

$$Z_T = \alpha_{RSN} \times G_{2\text{-}4S} \times (Z_{TR} - 2R_F) \tag{5}$$

Two-Wire to Four-Wire Gain

From (1) and (2) with $V_{RXP} = V_{RXM} = 0$:

$$G_{2-4} = \frac{V_{TXP} - V_{TXM}}{V_{TR}} = \frac{Z_T / \alpha_{RSN}}{\dfrac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F} \qquad (6)$$

Four-Wire to Two-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4-2} = \frac{V_{TR}}{V_{RXP} - V_{RXM}} = -\frac{Z_T}{Z_{RX}} \times \frac{Z_L}{\dfrac{Z_T}{\alpha_{RSN}} + G_{2-4S} \times (Z_L + 2R_F)} \qquad (7)$$

For applications where

$$\frac{Z_T}{\alpha_{RSN} \times G_{2-4S}} + 2R_F = Z_L$$

the expression for G_{4-2} simplifies to:

$$G_{4-2} = -\frac{Z_T}{Z_{RX}} \times \frac{1}{2 \times G_{2-4S}} \qquad (8)$$

Four-Wire to Four-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4-4} = \frac{V_{TXP} - V_{TXM}}{V_{RXP} - V_{RXM}} = -\frac{Z_T}{Z_{RX}} \times \frac{G_{2-4S} \times (Z_L + 2R_F)}{\dfrac{Z_T}{\alpha_{RSN}} + G_{2-4S} \times (Z_L + 2R_F)} \qquad (9)$$

By using

$V_{TXP} - V_{TXM} = V_{TX}$ (10)

$V_{RXP} - V_{RXM} = V_{RX}$ (11)

Equation 1 becomes

$$V_{TR} = \frac{V_{TX}}{G_{2-4S}} + I_L \times 2_{RF} \qquad (12)$$

Equation 2 becomes

$$\frac{I_L}{\alpha_{RSN}} = \frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} \qquad (13)$$

And equation 3 id.

$V_{TR} = E_L - I_L \times Z_L$ (14)

Longitudinal impedance

A feedback loop within the SLIC counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range.

The SLIC longitudinal impedance per wire, Z_{LoT} and Z_{LoR}, appears as typically 20 Ω to longitudinal disturbances. It should be noted that longitudinal currents may exceed the dc loop current without disturbing the vf transmission.

Capacitors C_{TC} and C_{RC} (Optional)

The primary function of the capacitors C_{TC} and C_{RC} is as a part of the overvoltage protection network. The overvoltage protection clamp may not respond quickly enough to very fast transients and therefore damaging voltages may reach the SLIC pins TIPX and RINGX. C_{TC} and C_{RC} will protect the SLIC by shorting such fast transients to ground.

C_{TC} and C_{RC} may be utilized for RFI filtering when needed. C_{TC} and C_{RC} form RFI filters in conjunction with suitable series impedances (i.e. resistances, inductances). Resistors R_{F1} and R_{F2} may be sufficient, but series inductances can be added to form a second order filter. Current-compensated inductors (common mode chokes) are suitable since they impose little metallic impedance but high longitudinal impedance, therefore having minimum influence on two-wire transmission. Recommended values for C_{TC} and C_{RC} are 1 nF or less. Lower values implies less influence on the return loss and less degradation of the longitudinal balance caused by missmathing between C_{TC} and C_{RC}. On the other hand with lower values of C_{TC} and C_{RC} will decrease the attenuation of longitudinal induced radio frequencies. The influence of these capacitors on the two-wire terminating impedance must be considered when selecting a value for $C_{TC} = C_{RC}$. C_{TC} and C_{RC} contribute to a metallic impedance of $1/(\pi \times f \times C_{TC}) = 1/(\pi \times f \times C_{RC})$, a TIPX to ground impedance of $1/(2 \times \pi \times f \times C_{TC})$ and a RINGX to ground impedance of $1/(2 \times \pi \times f \times C_{RC})$.

Ac - dc separation capacitor, C_{HP}

The high pass filter capacitor connected between terminals HP and TIPX provides the separation of the ac and dc signals, such that only ac signals are forwarded to the VTXP and VTXM terminals. C_{HP} positions the low end frequency response break point of the ac feedback loop in the SLIC. The C_{HP} value of 33 nF will position the low end frequency response 3 dB break point of the ac loop at 12 Hz (f_{3dB}) according to $f_{3dB} = 1/(2 \times \pi \times R_{HP} \times C_{HP})$ where $R_{HP} = 400$ kΩ.

Capacitor C_{LP}

The capacitor C_{LP}, which connects between the terminals LP and VTBAT, positions the high end frequency break point of the low pass filter in the dc feedback loop (battery feed controlling loop) of the SLIC. Both C_{LP} and C_{HP} influence the two-wire impedance at low frequencies (primarily below the vf band) by adding an impedance in parallel with the programmed two-wire impedance (set by R_{TM} and R_{TP} and/or the Z-filter in the codec). The SLIC SPICE model includes the effects of C_{LP} and C_{HP} on the vf transmission. The C_{LP} value of 470 nF will position the high end frequency response 3 dB break point of the ac loop at 0.3 Hz (f_{3dB}).

Adaptive overhead voltage, AOV

The Adaptive Overhead Voltage feature minimizes the SLIC power dissipation by permitting the TIPX and RINGX dc voltages to operate very close to the supply rails. When the

SLIC detects a condition where the ac signal on TIPX/RINGX is approaching the supply rail and therefore would become distorted, the SLIC adjusts the overhead voltage, such that the TIPX/RINGX dc bias is moved away from the rails and thereby yielding enough peak signal swing for the ac signal. High level signal conditions such as when voice and metering signals are transmitted simultaneously are therefore automatically accommodated for the duration of the high level signal condition. This AOV system provides the designer with a flexible solution for different system requirements and possible future changes regarding voice, metering and other signal levels. There is no dc overhead level that must be set to a fixed value on account of worst case predicted peak ac signal value. Overhead voltage is defined asthe voltage between TIPX and RINGX or RINGX and VTB (depending on selected state or used battery). The PBL387 85/1 will behave as a SLIC with fixed overhead voltage for signals in the 0-20 kHz range and with an amplitude less than $1V_{Peak}$. For signal amplitudes between $1V_{Peak}$ and $1.25\ V_{Peak}$ the adaptive overhead function will expand the overhead voltage making it possible for the signal to propagate through the SLIC without distortion. The expansion of the overhead occurs instantaneously. When the signal amplitude decreases, the overhead returns to its initial value with a time constant of approximately one second.

During operation the influence of the adaptive overhead function will not effect the SLIC performance in the constant current region of operation. If, however, the SLIC is in the off-hook, constant voltage region of operation, then the influence of the adaptive headroom will be apparent as a slight decrease in line voltage (and hence line current) as the SLIC adjusts to accommodate the larger signal (e.g. voice + metering).

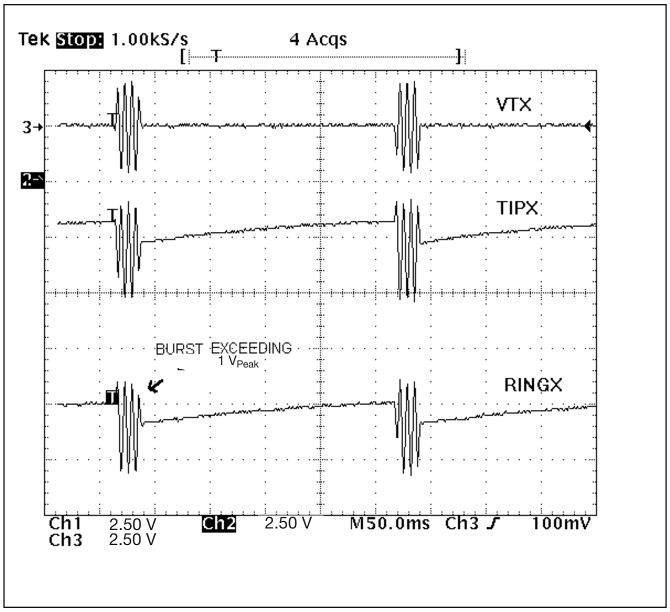


Figure 11. The AOV function. (Observe that burst is undersampled)

Metering Applications

Subscriber Pulse Metering (SPM), also known as Advice-of-Charge signaling (AOC), is used in several European countries to provide the subscriber with an accurate indication of the cost of a call in progress. Pulses of an out-of-speechband signal are sent at the same time as the speech signal down the telephone line, the rate of the pulses indicating the cost of the call - faster pulse rates indicate a more expensive call. An electronic meter at the subscriber counts the pulses as they arrive and indicates the call cost on a digital display. This meter is normally wired in parallel with the telephone circuit and also provides filtering of the signal so that the subscriber at the telephone does not hear it.

There are two frequencies used for SPM signaling: 12kHz and 16kHz. The frequency used depends on the national requirements. The frequency of the SPM signal must be quite accurate, ±0.5% is typical. Furthermore the signal must be sinusoidal with <5% total harmonic distortion. Pulse metering signals can be applied to the two-wire line via the PBL 387 85/1 SLIC by connecting the pulse-metering source through coupling capacitors and resistors to the RSNP and RSNM node. The capacitors in series isolates the RSN inputs from any dc voltage that may be superimposed on the metering signal. The signal level of metering has to be included when optimizing talk battery V_{TB}. It is possible to mix speech and metering up to $1.7\ V_{Peak}$ using the AOV function.

Battery Feed and Automatic Battery Switching

To reduce short loop power dissipation a second lower battery voltage, Off-hook or Talk battery, must be connected to the device via an external diode at terminal VTBAT. The SLIC automatically switches between the two battery supply voltages without need for external control. The silent battery switching to VBAT occurs when the line current is below 5.5 mA. This means that the current in On-hook, VBAT, battery is limited to 6 mA in the Active state. The On-hook voltage is derived from VBAT with the range of -43 V to -56 V at the TIPX and RINGX wires @ $V_{Bat} \geq -48$ V.

Constant current feed region (figure 12, curve segment A-B-C)

For TIPX to RINGX voltages $V_{TR} < |V_{TB}| - 5.7\ V$

where

V_{TR} = the tip to ring dc voltage
V_{TB} = the talk battery voltage
5.7 V = the voltage drop from $|V_{TB}|$ to the line voltage at point C in the graph of figure 12, calculated according to:

$$0.7\ V + 3.7\ V + (27\ mA \times 2 \times 25\ \Omega) \approx 5.7\ V$$

The PBL 387 85/1 emulates constant current loop feed. The constant current value is adjustable between 18 mA and 30 mA by setting a value for resistor R_{LC}:

$$R_{LC} = \frac{500}{I_{LProg}} - \frac{10.4 \times \ln(32 \times I_{LProg})}{I_{LProg}}$$

which may be approximated by

$$R_{LC} \approx \frac{500}{I_{LProg}}$$

where

I_{LProg}	desired constant current in A
R_{LC}	programming resistance in Ω
ln( )	natural logarithm

Resistive feed region (figure 12, curve segment C-D-E)

For $V_{TR} > |V_{TB}|$ -5.7 V the PBL 387 85/1 emulates resistive loop feed with feed resistance equal to 2x25 Ω. The slope of the resistive feed region is made steep to extend the constant current region as close to the talk battery voltage (V_{TBat}) as possible.

On-hook region (figure 12, curve segment E-G-H-J)

For loop currents I_L < 5.5 mA the PBL 387 85/1 automatically switches to feed loop current from the ring battery, V_{Bat}.
The switch from talk battery, V_{TBat}, to ring battery, V_{Bat}, occurs without hysteresis at point E in figure 12. For loop currents I_L within the on-hook range $0 \text{ mA} < I_L < 5.0\text{mA}$ (curve segment G-H-J) the line voltage remains nearly constant. This feature maintains a high on-hook voltage in the presence of dc line leakage currents or when a subscriber device consumes some current from the battery feed, e.g. to power displays. The On-hook voltage tracks the V_{BAT} voltage up to $|54.5|$ V, $V_{TROpen} = |V_{Bat}| - 4.5$ V. For V_{BAT} higher than $|54.5|$ V the On-hook voltage is limited to $|50|$ V typical.
In the presence of leakage currents $I_{LLk} < 5$ mA during on-hook: (Figure 12, curve segment G-H-J)
$V_{TROn\text{-}hook} = V_{TROpen} - I_{LLk} \times R_{Feed}$ where $R_{Feed} = 2\times25\ \Omega$

Optimizing V_{TB}

To optimize V_{TB} with actual load on the line:
$V_{TB} = (R_{LMax} + R_{FEED} + 2R_F) \times I_{Lprog} + V_F + 3.7$
where:

R_{Lmax}	is the maximum loop length including On-hook phone load
R_{Feed}	2×25 Ω
R_F	is the resistance of one fuse resistor.
I_{LProg}	is the programmed line current
V_F	is the forward voltage of D_{TB} Normal value is 0.7 V

Example: $R_{Lmax} = 600\ \Omega$, $R_F = 40\ \Omega$, $I_{LProg} = 26.8$ mA
This will give a V_{TB} of 24 V.

A: $I_L (@V_{TR}=0) = I_{Lconst} = I_{LProg}$

$$R_{LC} = \frac{500}{I_{LProg}} - \frac{10.4 \times \ln(32 \times I_{LProg})}{I_{LProg}}$$

B,C: $I_L = I_{Lconst}$, $V_{TR}(@C) = V_{App} - R_{FEED} \times I_{LProg}$

D: $R_{FEED} = 2\times25\ \Omega$

E: $I_L \approx 5.5$ mA , $V_{TR} = V_{App} - R_{FEED} \times 5.5$ mA

F: $V_{App} (@I_L = 0) = V_{TB} - V_F^* - 3.7$ V
* V_F is the forward voltage drop across diode D_{TB}

G: $I_L \approx 5$ mA

H: $R_{FEED} = 2 \times 25\ \Omega$

J: The On-hook voltage tracks the V_{BAT} voltage up to $|54.5|$ V, $V_{TROpen} = |V_{Bat}| - 4.5$ V. For $V_{BAT} > |54.5|$ V, $V_{TROpen} = 50$ V.

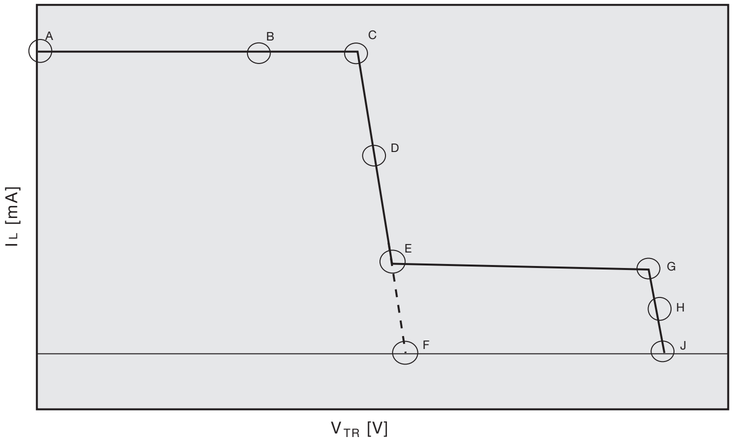


Figure 12. Battery feed characteristics.

Ringing Voltage

When designing PBL 38780/1 the object was to design a robust ringing SLIC that supports balanced ringing and that handles the high power dissipation and the different fault conditions that may occur when ringing. For power handling see section Power control.
Figure 13 shows a high level schematic of the ring loop. The ring loop in the PBL 38780/1 is designed as a voltage amplifier. An internal feedback loop from the two-wire to the input sets a predetermined voltage gain. The voltage gain is adjusted to 94 by the AGC-R when ringing. The power amplifiers are of the current feed type that makes it possible to provide a reliable control of the ringing current. This arrangement makes it possible to add a control device, including an Automatic Gain Control unit, that provides protecting functions, such as:

Automatic Gain Control-Ringing, AGC-R: If the amplifiers that supply Tip and Ring are forced to saturation due to i.e. variations of the VBAT voltage or the VR input signal level, the AGC-R will decrease the output signal. The shape of the output signal is kept undistorted. This function guarantees a low output impedance, approximately 2×20 Ω, and also allows variations in the input signal and the V_{Bat} voltage.

Current limit: At off-hook or in fault conditions, i.e. Tip and Ring are shorted, the control device will limit the ringing current to approximately 10 mA above the programmed ring-trip threshold.

Foreign voltage protection: The control device will detect if Tip and/or Ring are shorted to e.g. ground. The output voltage will be shut off to keep the power down. The detector output will be high.

Temperature management: If the chip temperature exceeds 155 °C the control device will reduce the output voltage until the chip temperature equals 155 °C, and increase it again when the temperature drops. The detector output, DET, is forced to a logic low level when the temperature guard is active.

The VRP and VRM pins are the input pins to the high impedance differential input. The voltage V_R is the non ground reference voltage between the VRP and VRM pins. It operates at a common mode level from GND to 2 V. The differential input handles any waveform, e.g. sinusoidal, trapezoid or square-wave shaped signals, since the SLIC acts like a linear amplifier. When using square-wave input signal it has to be filtered with a RC filter of R = 200 kΩ connected to ground

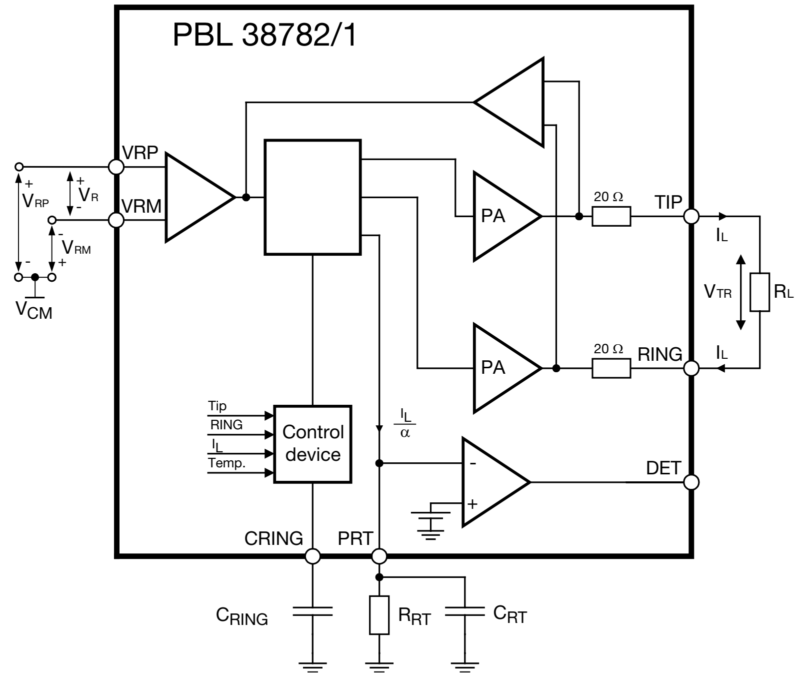


Figure 13. Ring loop schematic.

and C = 10 nF in series. A DC-offset can be obtained by adding a DC part to the input signal. The capacitor C_{RING} forms a low pass filter that is an essential part of the control device. The control device is used to control e.g. the applied output voltage, the ringing current or the chip temperature. The resistor R_{RT} is a programming resistor that sets the ring-trip detector threshold. The current through the resistor is a rectified version of the line current divided by a factor α. The capacitor C_{RT} filters the ring-trip detection device. The PRT-pin is connected to the negative input of an OP-amplifier. The positive input is connected to a reference voltage. The output of the OP-amp comparator is connected to the detector output DET. When the voltage over the resistor R_{RT} exceeds the reference voltage the detector output changes state.

The ring injection will be described in more detail with reference to figures 14 and 15. Figure 14 shows a ring sequence with an off-hook at time t1. The first diagram shows the voltages applied to the differential input, VRP and VRM, together with the voltages at TIPX and RINGX pins. The voltage of the TIP wire follows the voltage of the VRP pin.
The second diagram shows the rectified current, I_L/α, through the resistor R_{RT}. The dotted line represents the programmed ring-trip threshold, I_{LTH}/α.
The third diagram shows the voltage on the detector output. Before the time t1, the telephone is supposed to be on-hook. The signal to VRP and VRM is supplied symmetrically around the common mode voltage, V_{CM}.
The ring voltage is applied symmetrically around a fixed voltage, $V_{Bat}/2$, to the load. As long as the telephone is on-hook the rectified current, I_L/α, will not exceed I_{LTH}/α. The DET output will be high. The control device will make sure that the voltage over the load is as high as possible without saturating the power amplifiers. When the telephone goes off-hook, at time t1, the impedance of the load will decrease. The line current will increase and the control device will reduce the line current to a maximum of approximately 10 mA above the programmed ring-trip threshold, I_{LTH}. When the rectified current, I_L/α, exceeds or equals to I_{LTH}/α, the detector output, DET, will change to a logic low level, i.e. an off-hook. The voltage of the load will be reduced as a result of the control device limiting the line current. The figure 15 illustrates ringing with a DC offset. This method is useful when trying to extend the ring-trip capability. When programming the ring-trip threshold there must be some margin so that no false ring-trip occurs when ringing at high REN.
In on-hook the DC voltage will not have any affect on the load since there is no DC path, but when the telephone goes off-hook there will be a DC path and the extra voltage will give a high ring current. This arrangement makes it possible to set a higher ring-trip threshold value and thereby give a larger margin between the ring current in on-hook, with low RENs, and the ring current in off-hook. To keep the same amplitude on the AC signal, as when ringing without DC offset, the battery has to be increased by the same value as the programmed DC offset. The signal to the VRP-pin is supplied with a positive DC offset to the common mode voltage, V_{CM}. The signal to the VRM-pin is supplied around the common mode voltage. The signal on the Tip-wire will be applied with a positive DC offset to the fixed voltage $V_{BAT}/2$. The signal on the Ring-wire will be applied with a negative DC offset.

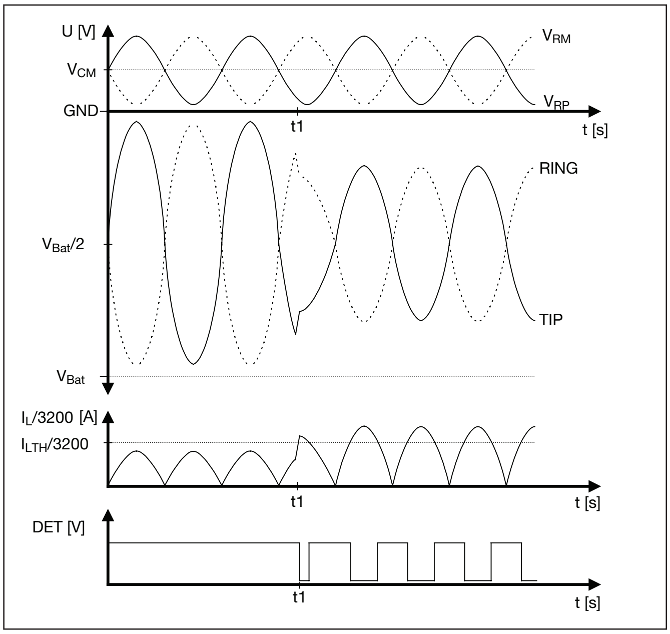


Figure 14. Off-hook during ringing.

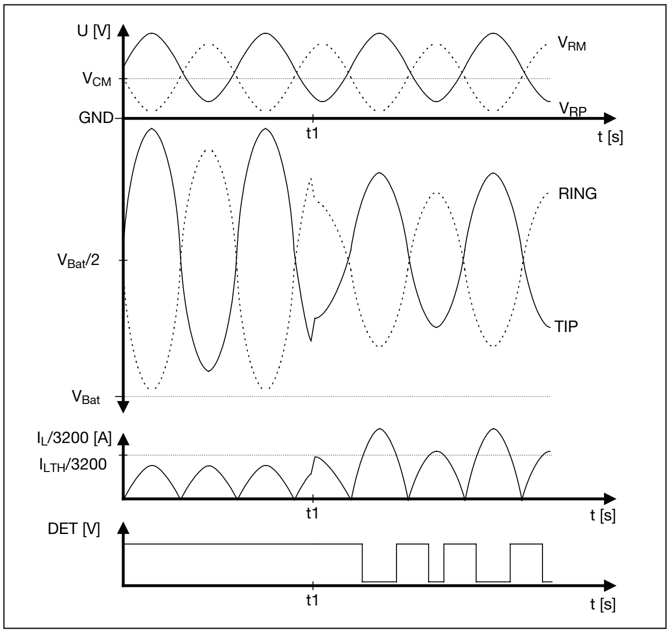


Figure 15. Off-hook during Ringing with an applied DC offset.

Calculation of the input signal

The VRP and VRM inputs have to be connected to a signal generator or via impedance to ground in all states. The following equations are valid for ringing loads between 0.25 and 5 REN. The optimal signals at VRP and VRM pins are calculated as follows:

$$VR_{PK} = \frac{|V_{Bat}| - 3.5}{94.4} \tag{17}$$

Where:

VR_{PK}	is the peak value of the AC-signal between the VRP and VRM pins.
V_{Bat}	is the voltage of the VBAT pin.

Example: $V_{Bat} = 80V$

This will give: $VR_{PK} = 0.81\ V_{PK}$
With DC-offset:

$$VR_{DC} = \frac{VR_{DCT-R}}{109.6} \tag{18}$$

$$VR_{PK+DC} = \frac{|V_{Bat}| - 3.5}{94.4} - VR_{DC} \tag{19}$$

Where:

VR_{DC}	is the DC voltage difference between the VRP and VRM pins.
VR_{DCT-R}	is the DC voltage difference between the TIP and RING wires.
VR_{PK+DC}	is the peak value of the AC-signal to be superimposed to the DC-voltage VR_{DC}.

Example: $V_{Bat} = -80\ V$, $VR_{DCT-R} = 10\ V$
This will give: $VR_{DC} = 0.091\ V$ and $VR_{PK+DC} = 0.718\ V_{PK}$

The tip wire follows the VRP pin. Setting VRP to a higher voltage potential than V_{RM} will make Tip go to a higher voltage potential than Ring. The common mode level of the VRP and VRM pins can be set to GND and up to 2V. If a differential signal generator is not available: Connect the VRM pin to GND. Apply a signal to the VRP pin referred to GND.
If the signal generator has a different common mode level than GND: Connect the VRM pin to GND and a resistor of 200 kΩ from the VRP pin to GND and a capacitor of 0.47 μF from the VRP pin to the signal generator

Calculation of the ring-trip threshold

The ring-trip threshold is calculated according to the equation:

$$R_{RT} = 3750 \times \frac{Z_{Bellmin} + 40 + 2 \times R_F + R_{Lmin}}{|V_{Bat}| \times \alpha_{Max} - 3.5} \tag{20}$$

With DC-offset:

$$R_{RT} = 3750 \times \frac{Z_{Bellmin} + 40 + 2 \times R_F + R_{Lmin}}{|V_{Bat}| \times \alpha_{Max} - 3.5 - VR_{DCT-R}} \tag{21}$$

Where:

40	is the resistance of the SLICs internal resistors connected in series with output amplifiers see figure 13.
R_{RT}	is the resistor value of the resistor connected between the PRT-pin and GND.
V_{Bat}	is the voltage of the VBAT pin.
α_{Max}	is the variation of the battery. 2% will give an α=1.02.
$Z_{Bellmin}$	is the minimum resistance of the bell in on-hook. Typical 1400 Ω for 5 REN.
R_F	is the resistance of one fuse resistor.
R_{Lmin}	is the resistance of the minimum loop length.
VR_{DCT-R}	is the DC voltage difference between the Tip and Ring wire.

Example: $V_{Bat} = -80\ V$, $Z_{BellMin} = 1300\ \Omega$, $\alpha_{Max} = 0\%$,
$R_F = 40\ \Omega$, $VR_{DCT-R} = 0$, $R_{Lmin} = 0\ \Omega$,
This will give: $R_{RT} = 69.6\ k\Omega$ and a Ring-trip current threshold,

$I_{LRth} = 57.5\ mA$

$$I_{LRth} = \frac{4000}{R_{RT}} \tag{22}$$

Power Dissipation Considerations

Thermal design considerations

The thermal resistance, Θ_{Ja}, of the PBL387 85/1 in a 44-pin QSOP package is 42.8 °C/W. The junction to ambient thermal resistance value, Θ_{Ja}, is extracted using the SEMI standard G38-0996 and is representative of the natural airflow as seen in an application with a multilayer board. In this device the thermal resistance is lowered by using batwing pins, i.e. pins that are thermally and electrically shorted to the die. This also means that the potential of the batwing pins are the same as the substrate potential, i.e. the V_{Bat} potential. To reduce the thermal resistance in critical applications these batwing pins must be used. Typical demanding applications involves high ring voltages, high DC-offset, high REN numbers, high line currents together with high talk battery and used in high ambient temperatures. In these type of applications the batwing pins shall be soldered to a large metal layer using thermal conducting vias, i.e. small vias that will be filled with solder during the soldering process. The metal layer shall be of the order of 1sq inch and most effective is to use an outer layer, which can be cooled by convection. The PBL387 85/1 has a thermal shutdown protection at a typical temperature, T_{JG} of 155 °C, see Analog temperature guard.

There are three situations where high power dissipation occurs.

1. Ringing power dissipation on-hook
2. Ringing power dissipation off-hook
3. Off-hook power dissipation

1. Ringing power dissipation on-hook

The power dissipation can be calculated by the following formula:

$$P_{RNG} = P_R \times \frac{t_R}{t_R + t_A} + P_A \times \frac{t_A}{t_R + t_A}$$

where:

P_{RNG}	Average power during ringing.
P_R	Power in Ring state.
P_A	Power in Active state P2 in the specification typical around 65 mW
t_R	Time in Ring state
t_A	Time in Active state

Ringing is normally applied with a defined ring cadence with burst and silent intervals where the SLIC is switched between the ring and active state. Typically the time t_A is four times the time t_R. In some applications the time for the ringing and silent periods are equal, and the SLIC will dissipate more power.

The power dissipation in the SLIC for the burst can be calculated using:

$P_R = P_S - P_{Out} =$

For a sinusodial shaped ring signal:

$$= \frac{2}{\pi} \times V_{BAT} \times \frac{V_{Ring}}{Z_{Loop}} - \frac{V_{Ring}^2 \times \cos\Theta_L}{2Z_{Loop}} + P_{RingBias}$$

where:

P_s	Supply power
P_{Out}	Output power
V_{BAT}	potential at pin
V_{Ring}	peak to peak voltage between tip and ring during ringing
$P_{RingBias}$	power dissipation in ring state without load, typical value 0.3 W
Z_{Loop}	total line impedance, including fuse and the telephone impedance (in this case the on-hook resistance)

Z_{Loop} can be calculated using:

$$Z_{Loop} = \sqrt{(R_{Line} + R_{Bell} + 2R_F)^2 + \left(\frac{1}{2\pi \times f_{Ring} \times C_{Bell}}\right)^2}$$

where:

R_{Line}	line resistance, typical 0-500 Ω.
R_{Bell}	total bell resistance
R_F	fuse and protection resistance, typical 40 Ω.
f_{Ring}	ring frequency
C_{Bell}	total bell capacitance

$$\Theta_L = -\alpha \tan\left(\frac{1/(2\pi \times f_{Ring} \times C_{Bell})}{R_{CU} + R_{Bell} + 2R_F}\right)$$

Example:

Calculate the SLIC power dissipation and junction temperature when $V_{Bat} = -80$ V, 5REN, line resistance = 0 Ω, protection resistance = 2×40 Ω and ring cadence is 1:1. Ambient temperature is 85 °C.

Typical values in North America can be for 5 REN:

$R_{Bell} = 1386\ \Omega$, $C_{Bell} = 40\ \mu F$, $f_{Ring} = 20$ Hz.

$$Z_{Loop} = \sqrt{(0 + 1386 + 2\times40)^2 + \left(\frac{1}{2\pi\times20\times40\times10^{-6}}\right)^2} = 1479\ \Omega$$

$V_{Ring} = V_{BAT} - 3.5 = 76.5$ V

The phase shift is very small so $\cos(\Theta_L)$ is very near one and the formula above is simplified to:

$$P_R = \frac{2}{\pi} \times V_{Bat} \times \frac{V_{Ring}}{Z_{Loop}} - \frac{V_{Ring}^2}{2Z_{Loop}} + P_{RingBias} =$$

$$= \frac{2}{\pi} \times 80 \times \frac{76.5}{1479} - \frac{76.5}{2958} + 0.3 = 0.96 \text{ W}$$

$$P_{RNG} = 0.96 \times \frac{1}{1+1} + 0.065 \times \frac{1}{1+1} = 0.51 \text{ W}$$

The $\Theta_{ja} = 42.8$ °C/W and ambient temperature = 85 °C.

$T_j = 0.51 \times 42.8 + 85 = 106.8$ °C

which is less then the thermal protection at 155 °C.

2. Ringing power dissipation off-hook

Using the same formula as above and 300 Ω as the off-hook load the result will indicate several Watts of power dissipation. In that case the SLIC will limit the current to approx. 10mA above the programmed ring-trip threshold, see section Calculation of the ring-trip threshold. If the system do not force the SLIC in to Active state the temperature guard will be activated and the detector output, DET, will stay low.

3. Off-hook power dissipation

The maximum off-hook power dissipation is dependent on the V_{TB} voltage, the line current I_L and the loop resistance R_{Loop}. The power dissipation in the SLIC can be calculated using:

$P_{Off\text{-}hook} = P_S - P_{Out} = V_{TB} \times I_L + P_q - I_L^2 \times R_{Loop}$

P_S	Supply power
P_{Out}	Output power
I_L	programmed line current
P_q	quiescent power, approx 65mW
R_{Loop}	the total line resistance, including fuse and the telephone impedance, in this case the off-hook resistance

Example:
Calculate the SLIC power dissipation and junction temperature when V_{TB} = -24 V, Programmed line current 27 mA, Off-hook resistance = 200 Ω , line resistance = 0 Ω, protection resistance = 2x40 Ω. Ambient temperature is 85°C.

$P_{Off\text{-}hook} = 24 \times 0.027 + 0.065 - (0.027)^2 \times (200+0+2 \times 40) = 0.51$ W

The junction temperature is calculated like the previous example.

Loop Monitoring Functions

The loop current, ground key and ring-trip detectors report their status through a common output, DET. The particular detector to be connected to the detector pin, DET, is selected via the three bit control interface C1, C2 and C3. Please refer to section Control Inputs for a description of the control interface.

Detector Output (DET)

The PBL 387 85/1 SLIC incorporates a detector output driver, DET, designed as an open collector (npn), an internal 10 kΩ pull-up resistor to VCC and an internal pull-down resistor of 20 kΩ to AGND. The logic high level is 3.3V to interface to the Broadcom chip.

Loop Current Detector

The loop current detector indicates that the telephone is off-hook and that dc current is flowing in the loop by setting the output pin DET to a logic low level when selected. The loop current detector threshold value, I_{LTh}, where the loop current detector changes state, is programmable with the R_{LD} resistor. R_{LD} connects between pin PLD and ground and is calculated according to:

$$R_{LD} = \frac{500}{I_{LTh}}$$

The loop current detector is internally filtered and is not influenced by the ac signal at the two-wire side. In the Tip Open Circuit state the DET output changes to logic low state when the RINGX current exceeds I_{LTh}.

Loop Ground Fault Detector

The loop fault ground detector circuit senses the difference between TIPX and RINGX currents. When triggerd the output pin DET is set to a logic high level. The detector is triggered when the difference exceeds the internally set and fixed current threshold.

Loop voltage measurement

The loop voltage, V_{TR} (V), is presented at the DET output as a pulse train with a repetition frequency, f_V (Hz), which is inversely proportional to the voltage according to:

$$f_V = \frac{10^6}{(|V_{TR}| + 1)}$$

The loop voltage measurement commences when commanding the SLIC into the loop voltage measurement state from any other state (refer to Table 1, SLIC operating states). Loop diagnostic purposes and setting line card gain are two examples of uses for the loop voltage information.

Control Inputs

The PBL 387 85/1 SLIC has three digital control inputs, C1, C2 and C3. A decoder in the SLIC interprets the control input condition and determing the commanded operating state. C1, C2 and C3 are internal pull-up inputs. The logic inputs are compatible with a 3.3V logic interface.

Open circuit state (C3, C2, C1 = 0,0,0)

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum and no detectors are active. DET output is set high.

Ringing state (C3, C2, C1 = 0,0,1)

The low voltage ringing signal, which is connected to VRP and VRM, is amplified and appears at TIPX and RINGX as a balanced high voltage ring signal. The ring-trip detector monitors hook status and sets the DET output low when off-hook line status is detected.

Active state (C3, C2, C1 = 0,1,0)

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. The loop current detector is activated. The loop current detector indicates off-hook with a logic low level present at the detector output.

Active state, loop voltage measurement
(C3, C2, C1 = 0,1,1)

A frequency inversely proportional to the line voltage will appear at the DET output when the PBL 387 85/1 is set to the active, loop voltage measurement state.

Active state, Loop Ground Fault Detector
(C3, C2, C1 = 1,0,1)

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. Senses it TIPX or RINGX wires are connected to ground and indicates it on DET.

Overtemperature and Overvoltage Protection

Analog temperature guard

The varying environmental conditions in which SLICs operate in conjunction with fault conditions may lead to the chip maximum temperature limitation being exceeded. The PBL 387 85/1 SLIC reduces the dc line current and the longitudinal current when the chip temperature reaches approximately 155°C and increases the line current again automatically when the chip temperature drops. Due to the linear nature of the chip temperature regulation (e.g. dc loop current partially reduced) a talk path may still be functional while the temperature guard is active. The detector output, DET, is forced to a logic low level while the temperature guard is active.

Overvoltage protection - general

PBL 387 85/1 must be protected against foreign voltages on the telephone line. Overvoltages can result from lightning, ac power contact, induction and other causes. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum continuous and transient voltages that the SLIC TIPX and RINGX terminals can withstand. Overvoltage protection consists of primary protection located outside of the line card (e.g. gas tubes in a main distribution frame) and secondary protection (series line resistors and solid state clamping devices such as diodes and thyristors) located on the linecard printed circuit board.

Secondary protection

The circuit shown in figure 9 utilizes series resistors (R_{F1}, R_{F2}) together with a programmable overvoltage protector (OVP, e. g. Power Innovations TISP PBL3 or TISP6NTP2AD) as secondary protection.

The TISP PBL3 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to the negative supply voltage (i.e. the battery voltage, V_{BAT}). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized. Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor, C_{GG}, is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. C_{GG} should be placed close to the overvoltage protection device. Without the capacitor even the low inductance in the track to the V_{BAT} supply will limit the current and delay the activation of the thyristor clamp.

The line protection resistors R_{F1} and R_{F2} serve the dual purposes of being non- destructing energy dissipators when transients are clamped and of being fuses when the line is exposed to a power cross. If longitudinal balance requirements permit, PTC resistors may be used for R_{F1} and R_{F2}. Note, however, that it is important to use fixed resistors in series with PTCs since PTCs are capacitive. Fast transients will therefore experience much less PTC impedance than do slower transients. Relying only on PTCs as the current limiting element could therefore result in excessive fast transient current through the clamp, with possible clamp current overload and resulting inability to protect the SLIC. A value of approximately 40 Ω for each of R_{F1} and R_{F2} limits the peak overvoltage transient current to a value that is compatible with the clamping device (OVP block in figure 9.) capability. Higher resistance values for R_{F1} and R_{F2} than 40 Ω will require more stringent matching of the R_{F1} and R_{F2} resistors and will also have a much greater impact on terminating impedance, gains and dc loop resistance. Lower resistance values for R_{F1} and R_{F2} than 40 Ω will result in peak clamp currents that may exceed the capability of standard clamping devices.

Power-up Sequence

No special power-up sequence is necessary except that ground has to be present before all other power supply voltages. The digital inputs C1, C2 and C3 are internal pull-up terminals.

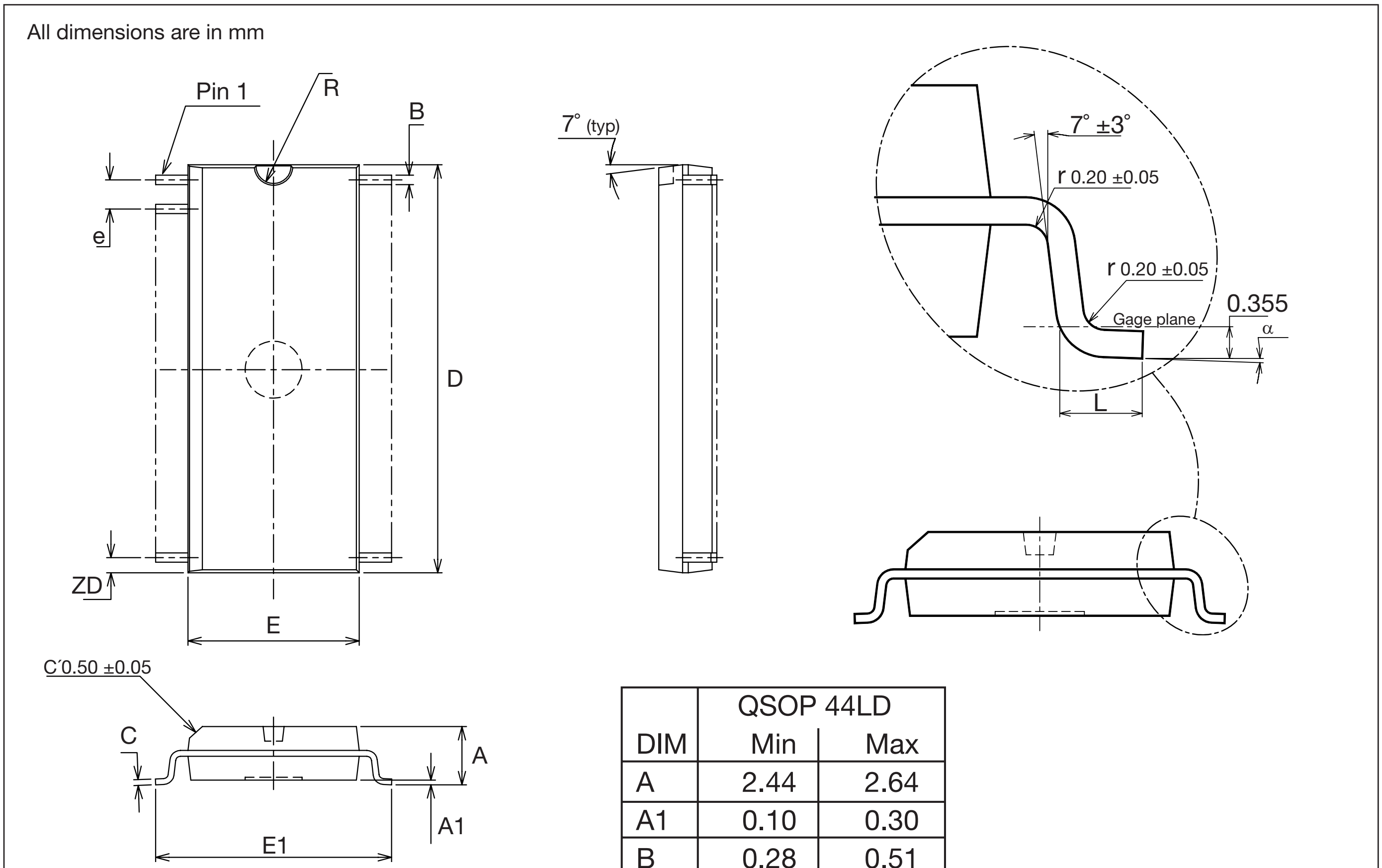
Printed Circuit Board Layout

Care in Printed Circuit Board (PCB) layout is essential for proper function. The components connecting to the RSNP and RSNM inputs should be placed in close proximity to those pins, such that no interference is injected into the receive summing nodes (RSN). Ground plane surrounding the RSNP and RSNM pins is advisable.

Analog ground (AGND) should be connected to battery ground (BGND) near the SLIC package. R_{LC} and R_{REF} should be connected to AGND with short leads. Pin LP and HP are sensitive to leakage currents. The C_{LP} connection between pins LP and VTBAT should be as short as possible. C_B and C_{TB} must be connected near the pins VBAT and VTBAT with short vias to ground. The batwing pins are internally connected to VBAT and used for transferring the heat from the chip to the printed circuit board. It is therefore advisable to implement a PCB layout that facilitates heat conduction away from the batwing pins.

Mechanical drawing

All dimensions are in mm



	QSOP 44LD	
DIM	Min	Max
A	2.44	2.64
A1	0.10	0.30
B	0.28	0.51
C	0.23	0.32
D	17.73	17.93
E	7.40	7.60
E1	10.11	10.51
L	0.40	1.27
R	0.63	0.89
Q	0°	8°
e	0.80 Ref	
ZD	0.51	

Figure 16. Mechanical drawing.

Ordering Information

Package	Temp. Range	Part No.
44-pin QSOP Tape & Reel	-40° - +85 °C	PBL 387 85/1QSA

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