M5M29FB/T800FP,VP,RV-80

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

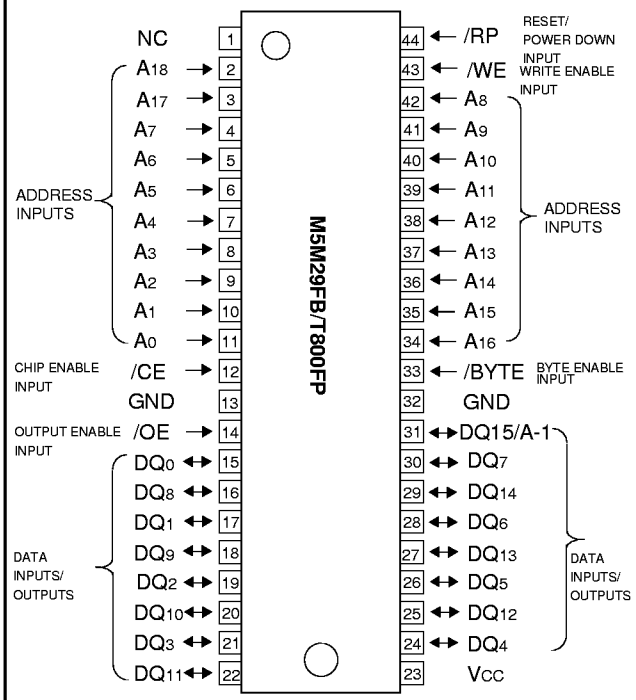
DESCRIPTION

The MITSUBISHI M5M29FB/T800FP, VP, RV are 3.3V-only high speed 8,388,608-bit CMOS boot block Flash Memories suitable for mobile and personal computing, and communication products. The M5M29FB/T800FP, VP, RV are fabricated by CMOS technology for the peripheral circuits and DINOR(Divided bit line NOR) architecture for the memory cells, and are available in 44pin SOP or 48pin TSOP(I).

FEATURES

- Organization ..... 524,288 word x 16bit
  ..... 1,048,576 word x 8 bit
- Supply voltage ..... VCC = 2.7V to 3.6V
- Access time ..... 80ns (Max) at 3.0V
  ..... 100/120ns (Max) at 2.7V
- Power Dissipation
  - Read ..... 108 mW (Max.)
  - Program/Erase ..... 144 mW (Max.)
  - Standby ..... 0.72 mW (Max.)
  - Deep power down mode ..... 0.33μW (typ.)
- Auto program
  - Program Time ..... 7.5ms (typ.)
  - Program Unit 128word
- Auto Erase
  - Erase time ..... 50 ms (typ.)
  - Erase Unit
    - Boot Block ..... 8Kword / 16Kbyte x 1
    - Parameter Block ..... 4Kword / 8Kbyte x 2
    - Main Block ..... 16Kword / 32Kbyte x 1
      ..... 32Kword / 64Kbyte x 15
- Program/Erase cycles ..... 100K cycles
- Boot Block
  - M5M29FB800 ..... Bottom Boot
  - M5M29FT800 ..... Top Boot
- Other Functions
  - Software Command Control
  - Selective Block Lock
  - Erase Suspend/Resume
  - Program Suspend/Resume
  - Status Register Read
  - Sleep
- Package
  - 48-Lead, 12mmx 20mm TSOP (type-I)
  - 44-Lead SOP
- Operation Temperature
  - 0 to 70°C for Read/Erase/Program

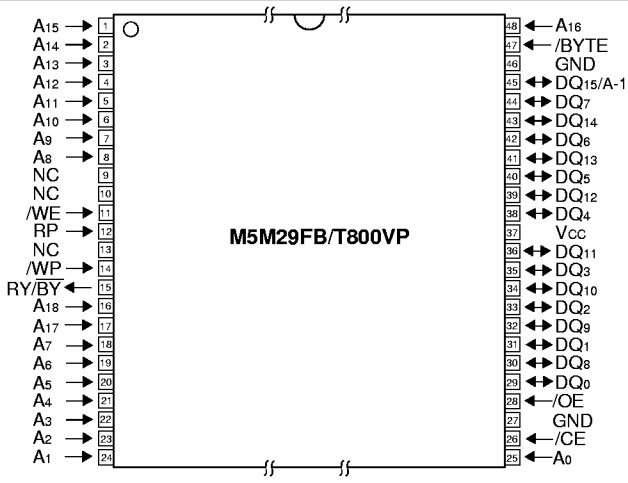
PIN CONFIGURATION (TOP VIEW)



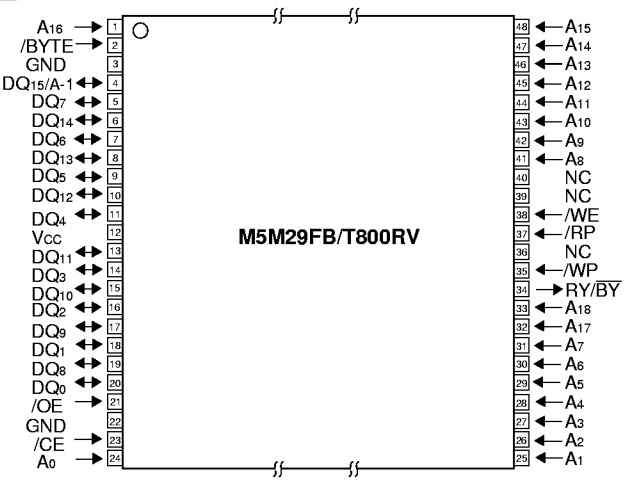
Outline 600mil 44-pin SOP
(FP: 44P2A-A)

APPLICATION

Code Storage PC BIOS
Digital Cellular Phone/Telecommunication



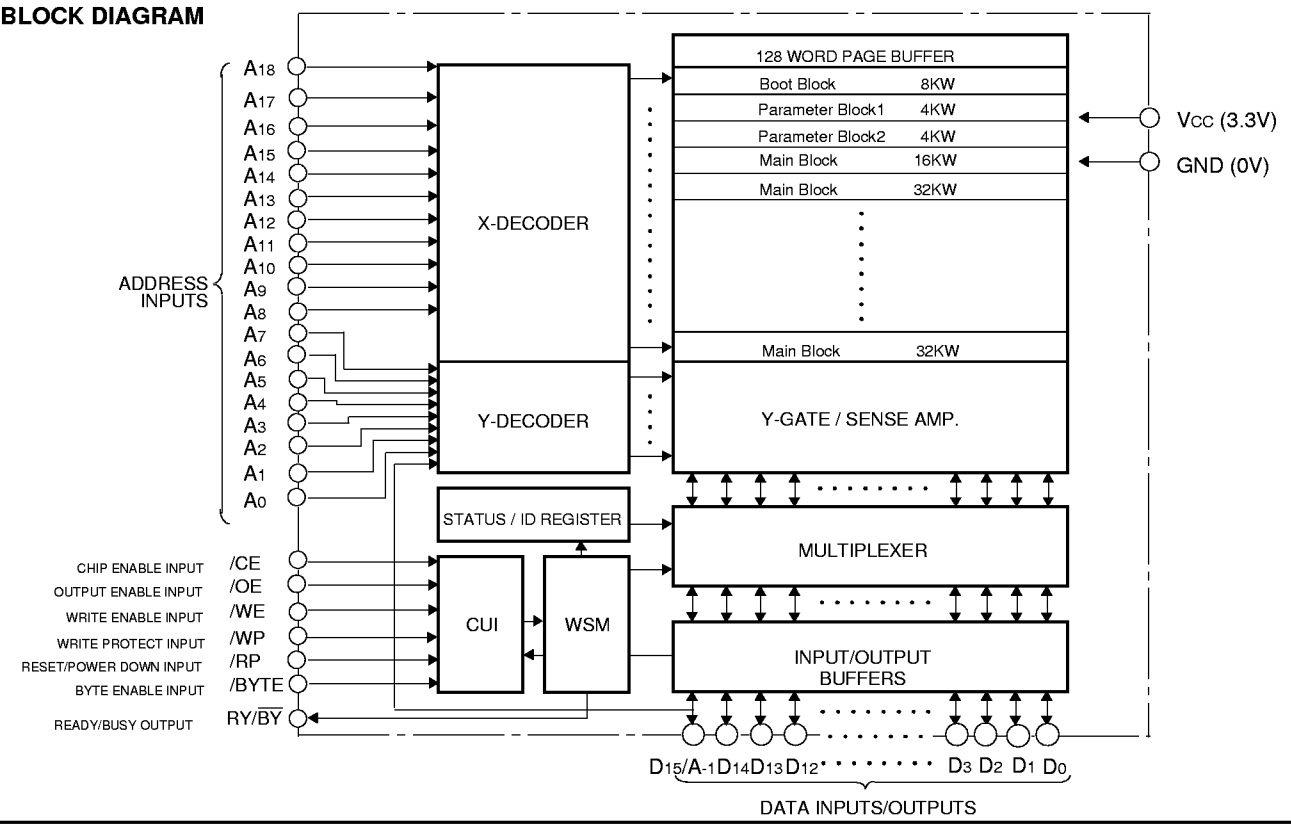
Outline 48pin TSOP type-I (12 X 20mm)
VP(Normal bend): 48P3R-B



RV(Reverse bend): 48P3R-C

NC : NO CONNECTION

BLOCK DIAGRAM



FUNCTION

The M5M29FB/T800FP,VP,RV includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Powerdown mode is enabled when the /RP pin is at GND, minimizing power consumption.

Read

The M5M29FB/T800FP,VP,RV has three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the M5M29FB/T800 automatically resets to read array mode. In the read array mode, low level input to /CE and /OE, high level input to /WE and /RP, and address signals to the address inputs (A0-A18) output the data of the addressed location to the data input/output(D0-15).

Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing /WE to low level, while /CE is at low level and /OE is at high level. Address and data are latched on the earlier rising edge of /WE and /CE. Standard micro-processor write timings are used.

Output Disable

When /OE is at VIH, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

Standby

When /CE is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

Deep Power-Down

When /RP is at VIL, the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance(High-Z) state. After return from powerdown, the CUI is reset to Read Array , and the Status Register is cleared to value 80H.

During block erase or program modes, /RP low will abort either operation. Memory array data of the block being altered become invalid.

SOFTWARE COMMAND DEFINITIONS

The device operations are selected by writing specific software command into the Command User Interface.

Read Array Command (FFH)

The device is in Read Array mode on initial device powerup and after exit from deep powerdown, or by writing FFH to the Command User Interface. The device remains in Read Array mode until the other commands are written.

Read Device Identifier Command (90H)

Though PROM programmers can normally read device identifier codes by raising A9 to V_{ID}, multiplexing high voltage onto address lines is not desired for micro-processor system. It is an other means to read device identifier codes that Read Device Identifier Code Command(90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from address 0000H and 0001H, respectively.

Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface.
The contents of Status Register are latched on the later falling edge of /OE or /CE. So /CE or /OE must be toggled every status read.

Clear Status Register Command (50H)

The Erase Status and Program Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Page Program Commands(41H)

Page Program allows fast programming of 128words of data. Writing of 41H initiates the page program operation. From 2nd cycle to 129th cycle write data must be serially inputted. Address A6-0 have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

Basically re-program must not be done on a page which has already programmed.

Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

DATA PROTECTION

The M5M29FB/T800 provides selectable block locking of memory blocks. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the M5M29FB/T800 has a master Write Protect pin (/WP) which prevents any modifications to memory blocks whose lock-bits are set to "0", when /WP is low. When /WP is high or /RP is V_{HH}, all blocks can be programmed or erased regardless of the state of the lock-bits, and the lock-bits are cleared to "1" by erase.

Power Supply Voltage

When the power supply voltage (Vcc) is less than 2.2V, the device is set to the Read-only mode.
A delay time of 2 μs is required before any device operation is initiated. The delay time is measured from the time Vcc reaches Vccmin (2.7V).
During power up, /RP=GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

x8 (Bytemode)	x16 (Wordmode)	
F0000H-FFFFFH	78000H-7FFFFH	32Kword MAIN BLOCK
E0000H-EFFFFH	70000H-77FFFH	32Kword MAIN BLOCK
D0000H-DFFFFH	68000H-6FFFFH	32Kword MAIN BLOCK
C0000H-CFFFFH	60000H-67FFFH	32Kword MAIN BLOCK
B0000H-BFFFFH	58000H-5FFFFH	32Kword MAIN BLOCK
A0000H-AFFFFH	50000H-57FFFH	32Kword MAIN BLOCK
90000H-9FFFFH	48000H-4FFFFH	32Kword MAIN BLOCK
80000H-8FFFFH	40000H-47FFFH	32Kword MAIN BLOCK
70000H-7FFFFH	38000H-3FFFFH	32Kword MAIN BLOCK
60000H-6FFFFH	30000H-37FFFH	32Kword MAIN BLOCK
50000H-5FFFFH	28000H-2FFFFH	32Kword MAIN BLOCK
40000H-4FFFFH	20000H-27FFFH	32Kword MAIN BLOCK
30000H-3FFFFH	18000H-1FFFFH	32Kword MAIN BLOCK
20000H-2FFFFH	10000H-17FFFH	32Kword MAIN BLOCK
10000H-1FFFFH	08000H-0FFFFH	32Kword MAIN BLOCK
08000H-0FFFFH	04000H-07FFFH	16Kword MAIN BLOCK
06000H-07FFFH	03000H-03FFFH	4Kword PARAMETER BLOCK
04000H-05FFFH	02000H-02FFFH	4Kword PARAMETER BLOCK
00000H-03FFFH	00000H-01FFFH	8Kword BOOT BLOCK
A_{-1}-A_{18}(Bytemode)	A_0-A_{18}(Wordmode)	

M5M29FB800 Memory Map

x8 (Bytemode)	x16 (Wordmode)	
FC000H-FFFFFH	7E000H-7FFFFH	8Kword BOOT BLOCK
FA000H-FBFFFH	7D000H-7DFFFH	4Kword PARAMETER BLOCK
F8000H-F9FFFH	7C000H-7CFFFH	4Kword PARAMETER BLOCK
F0000H-F7FFFH	78000H-7BFFFH	16Kword MAIN BLOCK
E0000H-EFFFFH	70000H-77FFFH	32Kword MAIN BLOCK
D0000H-DFFFFH	68000H-6FFFFH	32Kword MAIN BLOCK
C0000H-CFFFFH	60000H-67FFFH	32Kword MAIN BLOCK
B0000H-BFFFFH	58000H-5FFFFH	32Kword MAIN BLOCK
A0000H-AFFFFH	50000H-57FFFH	32Kword MAIN BLOCK
90000H-9FFFFH	48000H-4FFFFH	32Kword MAIN BLOCK
80000H-8FFFFH	40000H-47FFFH	32Kword MAIN BLOCK
70000H-7FFFFH	38000H-3FFFFH	32Kword MAIN BLOCK
60000H-6FFFFH	30000H-37FFFH	32Kword MAIN BLOCK
50000H-5FFFFH	28000H-2FFFFH	32Kword MAIN BLOCK
40000H-4FFFFH	20000H-27FFFH	32Kword MAIN BLOCK
30000H-3FFFFH	18000H-1FFFFH	32Kword MAIN BLOCK
20000H-2FFFFH	10000H-17FFFH	32Kword MAIN BLOCK
10000H-1FFFFH	08000H-0FFFFH	32Kword MAIN BLOCK
00000H-0FFFFH	00000H-07FFFH	32Kword MAIN BLOCK
A_{-1}-A_{18}(Bytemode)	A_0-A_{18}(Wordmode)	

M5M29FT800 Memory Map

BUS OPERATIONS

Bus Operations for Word-Wide Mode (/BYTE=V_{IH})

Mode \ Pins		/CE	/OE	/WE	/RP	DQ_{0-15}	RY/$\overline{BY}$
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data out	V_{OH} (Hi-Z)
	Status Register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Status Register Data	X 1)
	Lock Bit Status	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Lock Bit Data (DQ6)	X
	Identifier Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Identifier Code	V_{OH} (Hi-Z)
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	X
Stand by		V_{IH}	X 2)	X	V_{IH}	Hi-Z	X
Write	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command/Data in	X
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
	Others	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
Deep Power Down		X	X	X	V_{IL}	Hi-Z	V_{OH} (Hi-Z)

Bus Operations for Byte-Wide Mode (/BYTE=V_{IL})

Mode \ Pins		/CE	/OE	/WE	/RP	DQ_{0-7}	RY/$\overline{BY}$
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data out	V_{OH} (Hi-Z)
	Status Register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Status Register Data	X 1)
	Lock Bit Status	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Lock Bit Data (DQ6)	X
	Identifier Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Identifier Code	V_{OH} (Hi-Z)
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	X
Stand by		V_{IH}	X 2)	X	V_{IH}	Hi-Z	X
Write	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command/Data in	X
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
	Others	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
Deep Power Down		X	X	X	V_{IL}	Hi-Z	V_{OH} (Hi-Z)

1) X at RY/$\overline{BY}$ is V_{OL} or V_{OH}(Hi-Z).
*The RY/$\overline{BY}$ is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation.
A pull-up resistor of 10K-100K Ohms is required to allow the RY/$\overline{BY}$ signal to transition high indicating a Ready WSM condition.
2) X can be V_{IH} or V_{IL} for control pins.

SOFTWARE COMMAND DEFINITION

Command List

Command	1st bus cycle			2nd bus cycle			3rd bus cycle		
	Mode	Address	Data (D_{7-0})	Mode	Address	Data (D_{7-0})	Mode	Address	Data (D_{7-0})
Read Array	Write	X	FFH						
Device Identifier	Write	X	90H	Read	IA 2)	ID 2)			
Read Status Register	Write	X	70H	Read	X	SRD 3)			
Clear Status Register	Write	X	50H						
Page Program 4)	Write	X	41H	Write	WA0 4)	WD0 4)	Write	WA1	WD1
Block Erase / Confirm	Write	X	20H	Write	BA 5)	D0H			
Suspend	Write	X	B0H						
Resume	Write	X	D0H						
Read Lock Bit Status	Write	X	71H	Read	BA	DQ6 6)			
Lock Bit Program / Confirm	Write	X	77H	Write	BA	D0H			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0H			
Sleep 7)	Write	X	F0H						

1) In the word-wide mode, upper byte data (D8-D15) is ignored.
2) IA=ID Code Address : A0=VIL (Manufacturer's Code) : A0=VIH (Device Code), ID=ID Code,
/BYTE =VIL : A-1, A1-A18 = VIL, /BYTE =VIH : A1-A18 = VIL
3) SRD = Status Register Data
4) WA=Write Address, WD=Write Data.
/BYTE =VIL : Write Address and Write Data must be provided sequentially from 00H to FFH for A-1-A6.
Page size is 256Byte (256byte x 8bit), /BYTE =VIH : Write Address and Write Data must be provided sequentially from 00H to 7FH for A0-A6. Page size is 128word (128word x 16bit).
5) BA = Block Address (Addresses except Block Address mest be VIH.)
6) DQ6 provides Block Lock Status, DQ6 = 1 : Block Unlock, DQ6 = 0 : Block Locked.
7) Sleep command (F0H) put the device into the sleep mode after completing the current operation. The active current is reduced to deep power -down levels. The Read Array command (FFH) must be written to get the device out of sleep mode.

BLOCK LOCKING

SOP Package		TSOP Package			Write Protection Provided
/RP	Lock Bit(Internally)	/RP	/WP	Lock Bit(Internally)	
V_{IL}	X	V_{IL}	X	X	All Blocks Locked (Deep Power Down Mode)
V_{HH}	X	V_{HH}	X	X	All Blocks UnLocked
V_{IH}	0	V_{IH}	V_{IL}	0	Blocks Locked (Depend on Lock Bit Data)
V_{IH}	1	V_{IH}	V_{IL}	1	Blocks Unlocked (Depend on Lock Bit Data)
		V_{IH}	V_{IH}	X	All Blocks Unlocked

D_6 provides Lock Status of each block after writing the Read Lock Status command (71H).
In case of TSOP package, /WP pin must not be switched during performing Read / Write operations or WSM Busy (WSMS = 0).

STATUS REGISTER

Symbol	Status	Definition	
		"1"	"0"
SR.7 (D_7)	Write State Machine Status	Ready	Busy
SR.6 (D_6)	Suspend Status	Suspended	Operation in Progress / Completed
SR.5 (D_5)	Erase Status	Error	Successful
SR.4 (D_4)	Program Status	Error	Successful
SR.3 (D_3)	Block Status after Program	Error	Successful
SR.2 (D_2)	*Reserved*	-	-
SR.1 (D_1)	*Reserved*	-	-
SR.0 (D_0)	Device Sleep Status	Device in Sleep	Device Not in Sleep

*The RY/$\overline{BY}$ is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation. A pull-up resistor of 10K-100K Ohms is required to allow the RY/$\overline{BY}$ signal to transition high indicating a Ready WSM condition.

*D3 indicates the block status after the page programming. When D3 is "1", the page has the over-programed cell . If over-program occures, the device is block fail. However if D3 is "1", please try the block erase to the block. The block may revive.

DEVICE IDENTIFIER CODE

Code \ Pins	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hex. Data
Manufacturer Code	V_{IL}	0	0	0	1	1	1	0	0	1CH
Device Code (-T)	V_{IH}	0	1	0	1	1	1	0	1	5DH
Device Code (-B)	V_{IH}	0	1	0	1	1	1	1	0	5EH

In the word-wide mode, the same data as D_{7-0} is read out from D_{15-8}.
A_9 = V_{HH} Mode : A_9 = 11.4V to 12.6V Set A9 to V_{HH} min.200ns before falling edge of /CE in ready status. Min.200ns after return to V_{IH} ,device can't be accessed.
A_1 to A_8, A_{10} to A_{18}, /CE,/OE = VIL, /WE = V_{IH}
D_{15}/A-1 = V_{IL} (/BYTE = L)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	V_{CC} voltage	With respect to Ground	-0.2	4.6	V
V_{I1}	All input or output voltage except V_{CC},A9,/RP[1)]		-0.6	4.6	V
V_{I2}	A9,RP supply voltage		-0.6	14.0	V
T_a	Ambient temperature		0	70	°C
T_{bs}	Temperature under bias		-10	80	°C
T_{stg}	Storage temperature		-65	125	°C
I_{OUT}	Output short circuit current			100	mA

1) Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods < 20ns. Maximum DC voltage on input/output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+1.5V for periods < 20ns.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, Control Pins)	Ta = 25°C, f = 1MHz, V_{in} = V_{out} = 0V			8	pF
C_{OUT}	Output capacitance				12	pF

DC ELECTRICAL CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 2.7V to 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ1)	Max	
I_{LI}	Input leakage current	0V≤V_{IN}≤V_{CC}			±1.0	µA
I_{LO}	Output leakage current	0V≤V_{OUT}≤V_{CC}			±10	µA
I_{SB1}	V_{CC} standby current	V_{CC} = 3.6V, V_{IN}=V_{IL}/V_{IH}, /CE = /RP =/WP = V_{IH}		50	200	µA
I_{SB2}		V_{CC} = 3.6V, V_{IN}=GND or V_{CC}, /CE = /RP = /WP= V_{CC}±0.3V		0.1	5	µA
I_{SB3}	V_{CC} deep powerdown current	V_{CC} = 3.6V, V_{IN}=V_{IL}/V_{IH}, /RP = V_{IL}		5	15	µA
I_{SB4}		V_{CC} = 3.6V, V_{IN}=GND or V_{CC}, /RP =GND±0.3V		0.1	5	µA
I_{CC1}	V_{CC} read current for Word or Byte	V_{IN}=V_{IL}/V_{IH}, /CE = V_{IL}, /RP=/OE=V_{IH}, f = 12.5MHz, I_{OUT} = 0mA; V_{CC} = 3.3V		17	25	mA
		V_{CC} = 3.6V			30	
I_{CC2}	V_{CC} Write current for Word or Byte	V_{CC} = 3.6V,V_{IN}=V_{IL}/V_{IH}, /CE =/WE= V_{IL}, /RP=/OE=V_{IH}			30	mA
I_{CC3}	V_{CC} program current	V_{CC} = 3.6V, V_{IN}=V_{IL}/V_{IH}, /CE = /RP =/WP = V_{IH}			40	mA
I_{CC4}	V_{CC} erase current	V_{CC} = 3.6V, V_{IN}=V_{IL}/V_{IH}, /CE = /RP =/WP = V_{IH}			40	mA
I_{CC5}	V_{CC} suspend current	V_{CC} = 3.6V, V_{IN}=V_{IL}/V_{IH}, /CE = /RP =/WP = V_{IH}			200	µA
I_{RP}	/RP all block unlock current	/RP = $V_{HH\ max}$			100	µA
I_{ID}	A9 intelligent identifier current	A9 = $V_{ID\ max}$			100	µA
V_{IHH}	/RP unlock voltage		11.4	12.0	12.6	V
V_{ID}	A9 intelligent identifier voltage		11.4	12.0	12.6	V
V_{IL}	Input low voltage		– 0.5		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+0.5	V
V_{OL}	Output low voltage	I_{OL} = 4.0mA			0.45	V
V_{OH1}	Output high voltage	I_{OH} = –2.0mA	0.85Vcc			V
V_{OH2}		I_{OH} = –100µA	V_{CC}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out voltage 2)		1.5		2.5	V

All currents are in RMS unless otherwise noted.
1) Typical values at Vcc=3.3V, Ta=25°C
2) To protect against initiation of write cycle during Vcc power-up/ down, a write cycle is locked out for Vcc less than V_{LKO}.
If Vcc is less than V_{LKO}, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Vcc is less than V_{LKO}, the alteration of memory contents may occur.

AC ELECTRICAL CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 2.7V to 3.6V)

Read-Only Mode

Symbol		Parameter	Limits									Unit
			80ns (Vcc = 3.0V)			100ns			120ns			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC}	t_{AVAV}	Read cycle time	80			100			120			ns
$t_{a(AD)}$	t_{AVQV}	Address access time			80			100			120	ns
$t_{a(CE)}$	t_{ELQV}	Chip enable access time			80			100			120	ns
$t_{a(OE)}$	t_{GLQV}	Output enable access time			40			50			60	ns
t_{CLZ}	t_{ELQX}	Chip enable to output in low-Z	0			0			0			ns
$t_{DF(CE)}$	t_{EHQZ}	Chip enable high to output in high Z			25			25			30	ns
t_{OLZ}	t_{GLQX}	Output enable to output in low-Z	0			0			0			ns
$t_{DF(OE)}$	t_{GHQZ}	Output enable high to output in high Z			25			25			30	ns
t_{PHZ}	t_{PLQZ}	/RP low to output high-Z			150			150			300	ns
$t_{a(BYTE)}$	$t_{FL/HQV}$	/BYTE access time			80			100			120	ns
t_{BHZ}	t_{FLQZ}	/BYTE low to output high-Z			25			25			30	ns
t_{OH}	t_{OH}	Output hold from /CE, /OE, addresses	0			0			0			ns
t_{BCD}	$t_{ELFL/H}$	/CE low to /BYTE high or low			5			5			5	ns
t_{BAD}	$t_{AVFL/H}$	Address to /BYTE high or low			5			5			5	ns
t_{OEH}	t_{WHGL}	OE hold from /WE high	80			100			120			ns
t_{PS}	t_{PHEL}	/RP recovery to /CE low	500			500			500			ns

Timing measurements are made under AC waveforms for read operations.

AC ELECTRICAL CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 2.7V to 3.6V)

Write Mode (/WE control)

Symbol		Parameter	Limits									Unit
			80ns (Vcc = 3.0V)			100ns			120ns			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WC}	t_{AVAV}	Write cycle time	80			100			120			ns
t_{AS}	t_{AVWH}	Address set-up time	50			50			50			ns
t_{AH}	t_{WHAX}	Address hold time	10			10			10			ns
t_{DS}	t_{DVWH}	Data set-up time	50			50			50			ns
t_{DH}	t_{WHDX}	Data hold time	10			10			10			ns
t_{CS}	t_{ELWL}	Chip enable set-up time	0			0			0			ns
t_{CH}	t_{WHEH}	Chip enable hold time	0			0			0			ns
t_{WP}	t_{WLWH}	Write pulse width	60			60			60			ns
t_{WPH}	t_{WHWL}	Write pulse width high	20			20			20			ns
t_{BS}	$t_{FL/HWH}$	Byte enable high or low set-up time	50			50			50			ns
t_{BH}	$t_{WHFL/H}$	Byte enable high or low hold time	80			100			120			ns
t_{BLS}	t_{PHHWH}	Block Lock set-up to write enable high	80			100			120			ns
t_{BLH}	t_{QVPH}	Block Lockhold from valid SRD	0			0			0			ns
t_{DAP}	t_{WHRH1}	Duration of auto-program operation		7.5	120		7.5	120		7.5	120	ms
t_{DAE}	t_{WHRH2}	Duration of auto-block erase operation		50	600		50	600		50	600	ms
t_{WHRL}	t_{WHRL}	Write enable high to RY/$\overline{BY}$ low			80			100			120	ns
t_{PS}	t_{PHWL}	/RP high recovery to write enable low	500			500			500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at Vcc=3.3V, Ta=25°C

AC ELECTRICAL CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 2.7V to 3.6V)

Write Mode (/CE control)

Symbol		Parameter	Limits									Unit
			80ns (Vcc = 3.0V)			100ns			120ns			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WC}	t_{AVAV}	Write cycle time	80			100			120			ns
t_{AS}	t_{AVEH}	Address set-up time	50			50			50			ns
t_{AH}	t_{EHAX}	Address hold time	10			10			10			ns
t_{DS}	t_{DVEH}	Data set-up time	50			50			50			ns
t_{DH}	t_{EHDX}	Data hold time	10			10			10			ns
t_{WS}	t_{WLEL}	Write enable set-up time	0			0			0			ns
t_{WH}	t_{EHWH}	Write enable hold time	0			0			0			ns
t_{CEP}	t_{ELEH}	/CE pulse width	60			60			60			ns
t_{CEPH}	t_{EHEL}	/CE pulse width high	20			20			20			ns
t_{BS}	$t_{FL/HEH}$	Byte enable high or low set-up time	50			50			50			ns
t_{BH}	$t_{EHFL/H}$	Byte enable high or low hold time	80			100			120			ns
t_{BLS}	t_{PHHEH}	Block Lock set-up to write enable high	80			100			120			ns
t_{BLH}	t_{QVPH}	Block Lockhold from valid SRD	0			0			0			ns
t_{DAP}	t_{EHRH1}	Duration of auto-program operation		7.5	120		7.5	120		7.5	120	ms
t_{DAE}	t_{EHRH2}	Duration of auto-block erase operation		50	600		50	600		50	600	ms
t_{EHRL}	t_{EHRL}	/CE enable high to RY/$\overline{BY}$ low			80			100			120	ns
t_{PS}	t_{PHEL}	/RP high recovery to write enable low	500			500			500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at Vcc=3.3V, Ta=25°C

Erase and Program Performance

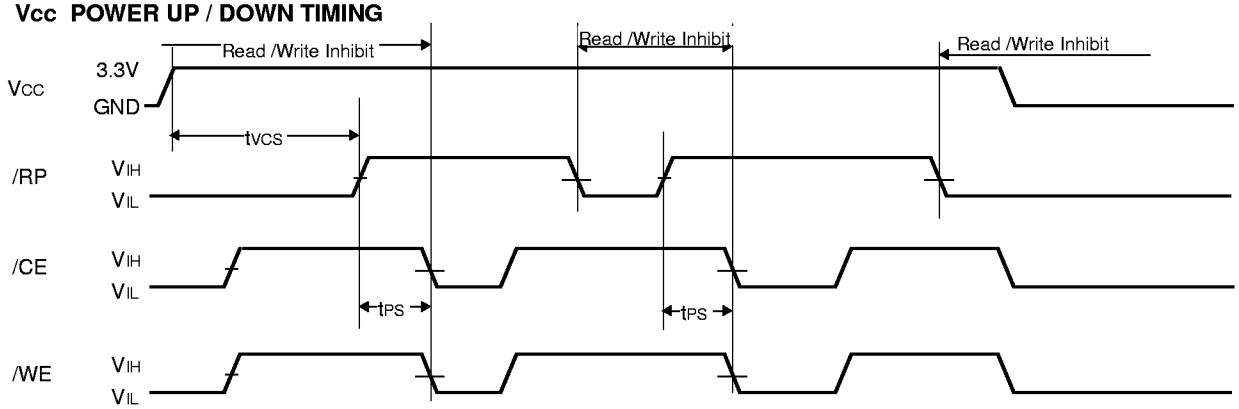
Parameter	Min	Typ	Max	Unit
Block Erase Time		50	600	ms
Main Block Write Time (Page Mode)		1.9	3.8	sec
Page Write Time		7.5	120	ms

Vcc Power Up / Down Timing

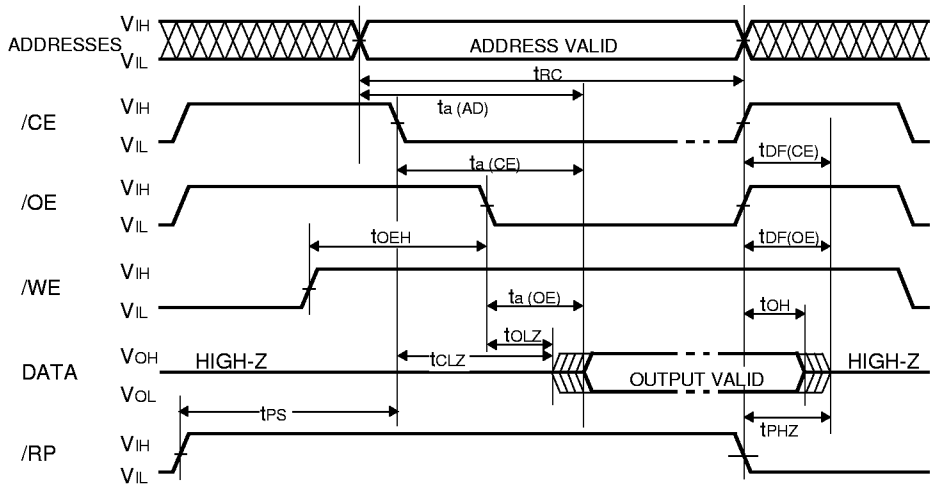
Symbol	Parameter	Min	Typ	Max	Unit
t_{VCS}	/RP =V_{IH} set-up time from Vccmin	2			µs

During power up/down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming.
The device must be protected against initiation of write cycle for memory contens during power up/down.
The delay time of min.2µsec is always required before read operation or write operation is initiated from the time Vcc reaches Vccmin during power up/down. By holding /RP V_{IL}, the contens of memory is protected during Vcc power up/down.
During power up, /RP must be held V_{IL} for min.2µs from the time Vcc reaches Vccmin.
During power down, /RP must be held V_{IL} until Vcc reaches GND.
/RP doesn't have latch mode ,so /RP must be held V_{IH} during read operation or erase/program operation.

Vcc POWER UP / DOWN TIMING



AC WAVEFORMS FOR READ OPERATION AND TEST CONDITIONS

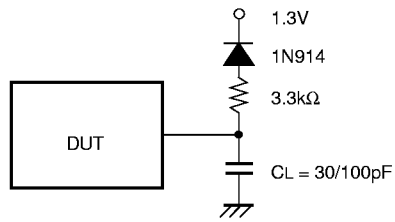


TEST CONDITIONS
FOR AC CHARACTERISTICS

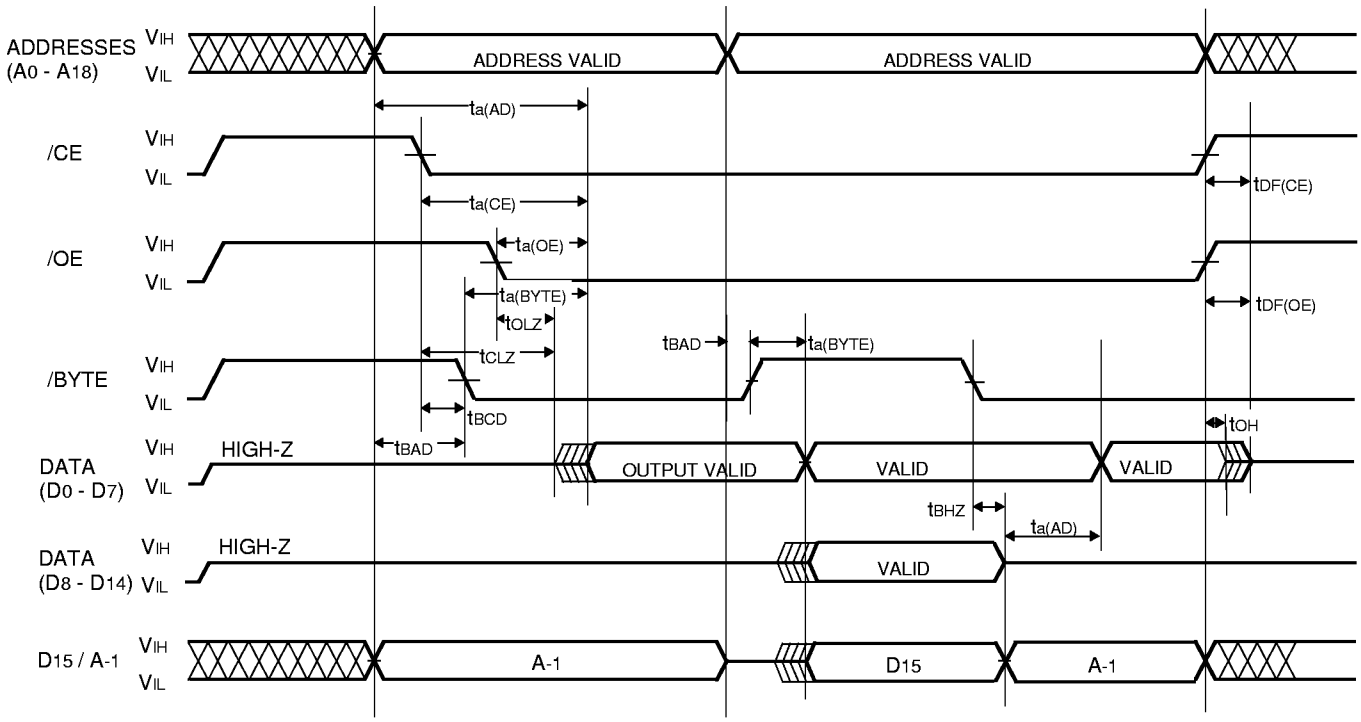
Input voltage : V_{IL} = 0V, V_{IH} = 2.7 V
Input rise and fall times : ≤5ns (80/100ns)
≤10ns (120ns)
Reference voltage
at timing measurement : 1.5V

Output load : 1TTL gate + CL

Acc.Time	Vcc	CL
80ns	3.0V	30pF
100ns	2.7V	30pF
	3.0V	100pF
120ns	2.7V	100pF

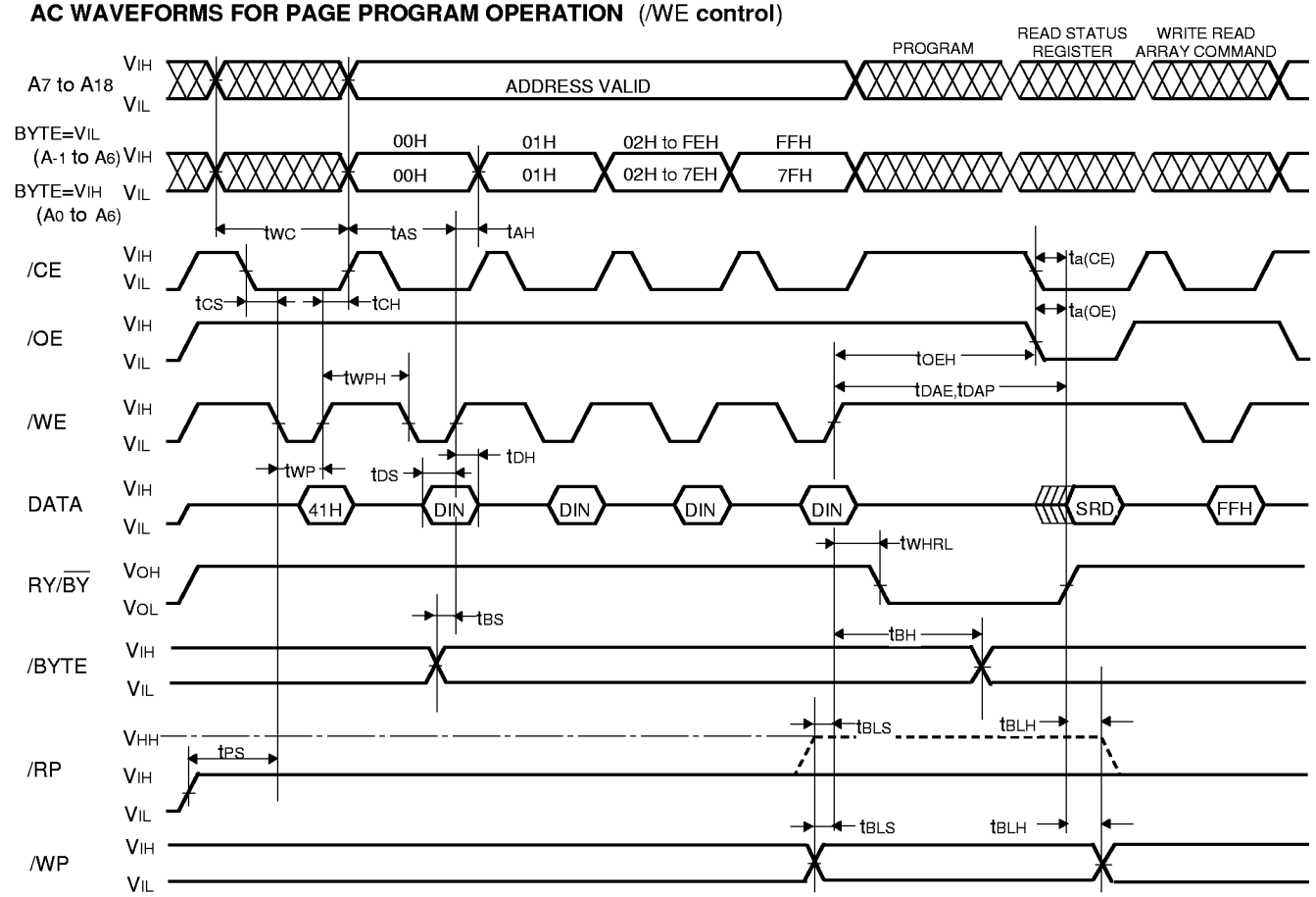


BYTE AC WAVEFORMS FOR READ OPERATION

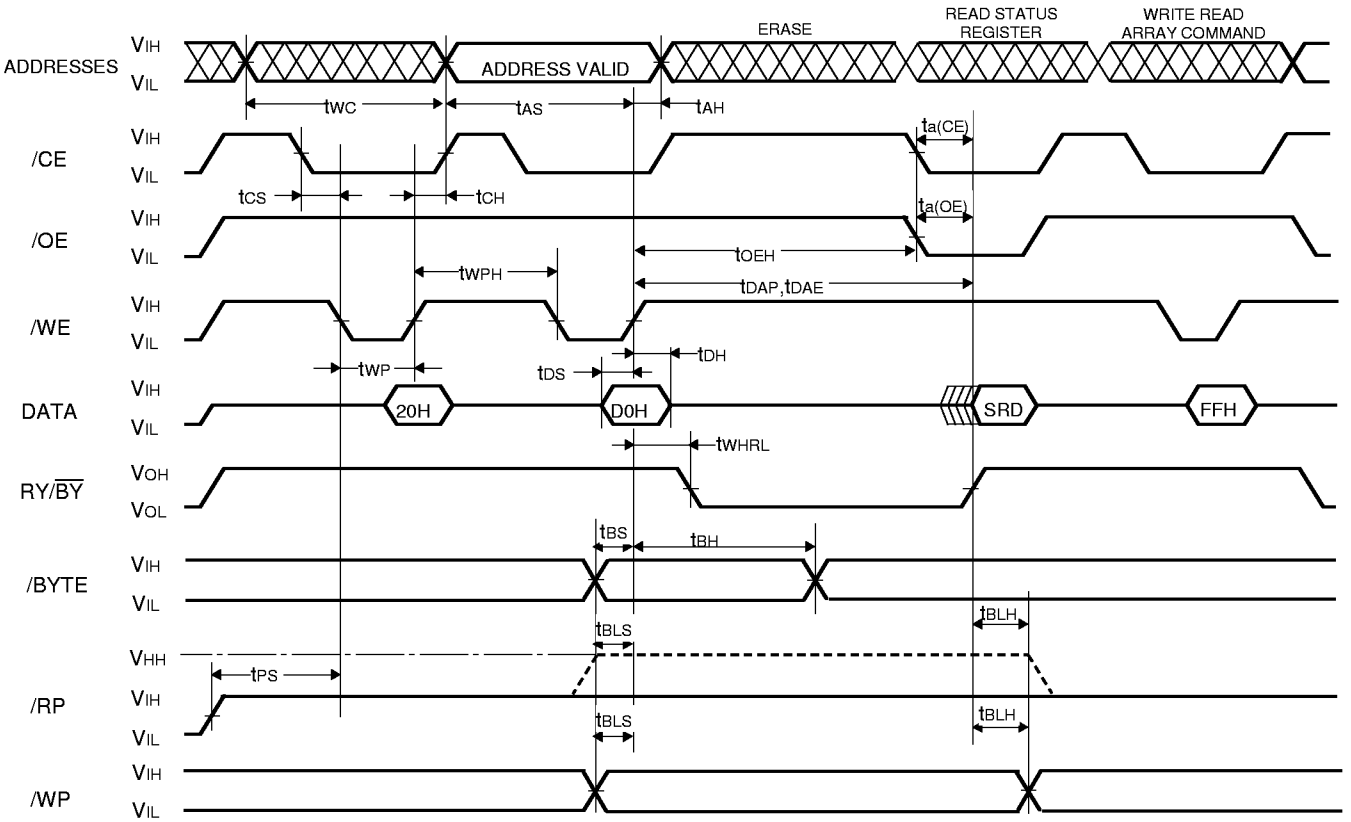


When /BYTE=V_{IH}, /CE=/OE=V_{IL} , D_{15}/A_{-1} is output status. At this time, input signal must not be applied.

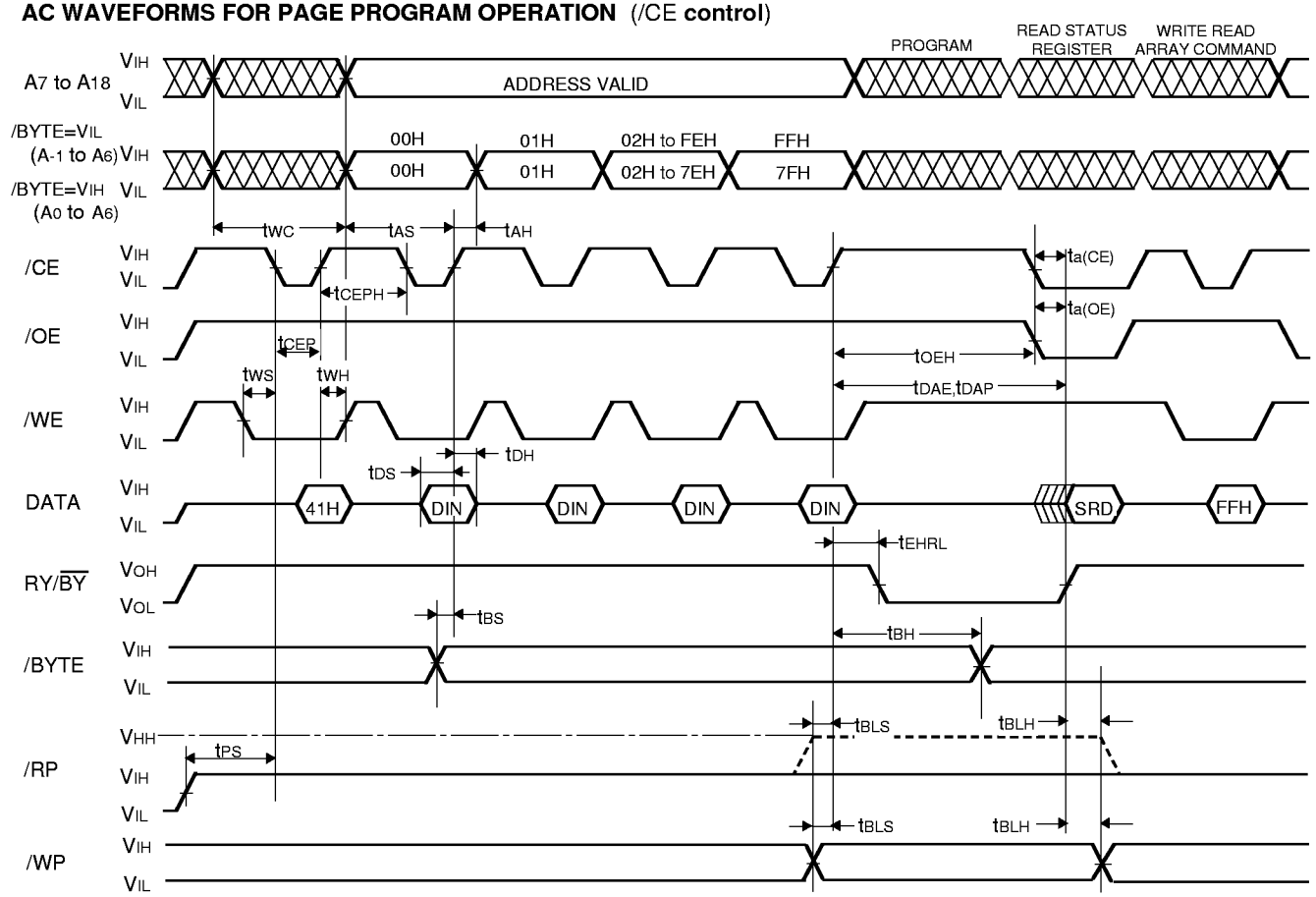
AC WAVEFORMS FOR PAGE PROGRAM OPERATION (/WE control)



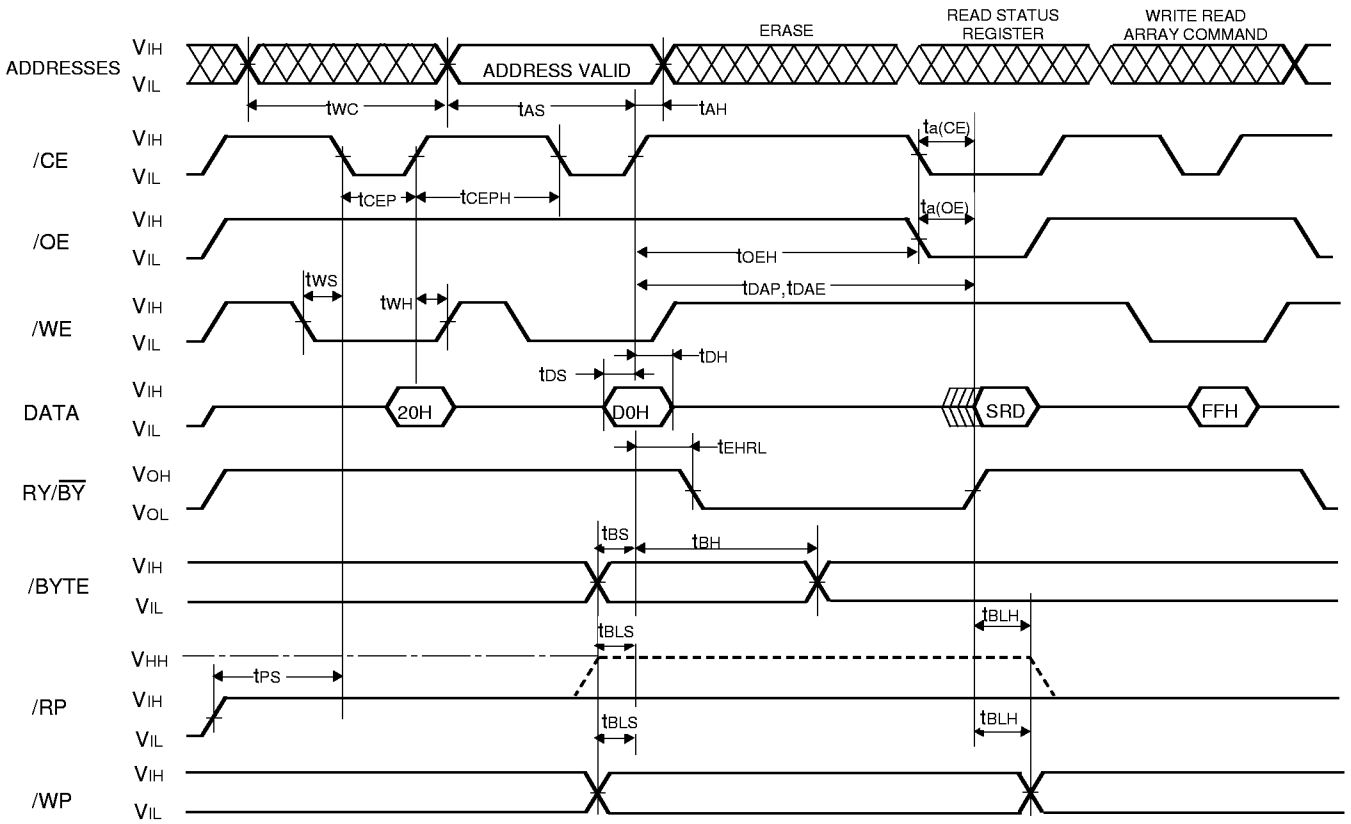
AC WAVEFORMS FOR ERASE OPERATIONS (/WE control)



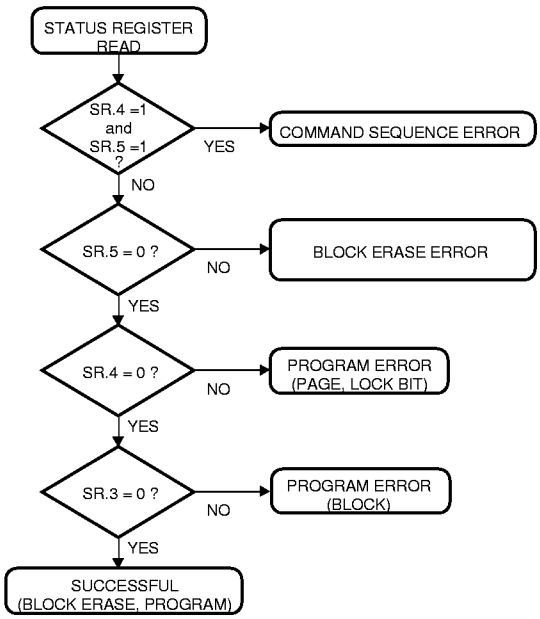
AC WAVEFORMS FOR PAGE PROGRAM OPERATION (/CE control)



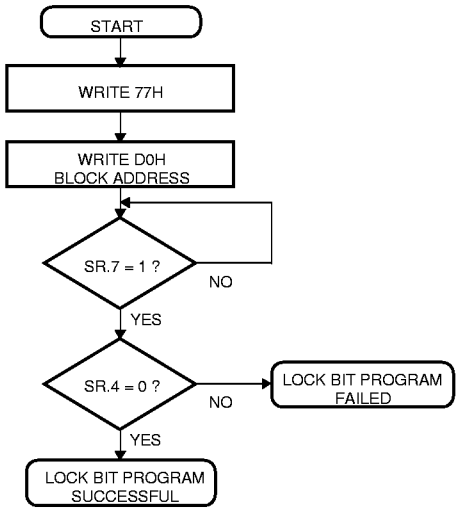
AC WAVEFORMS FOR ERASE OPERATIONS (/CE control)



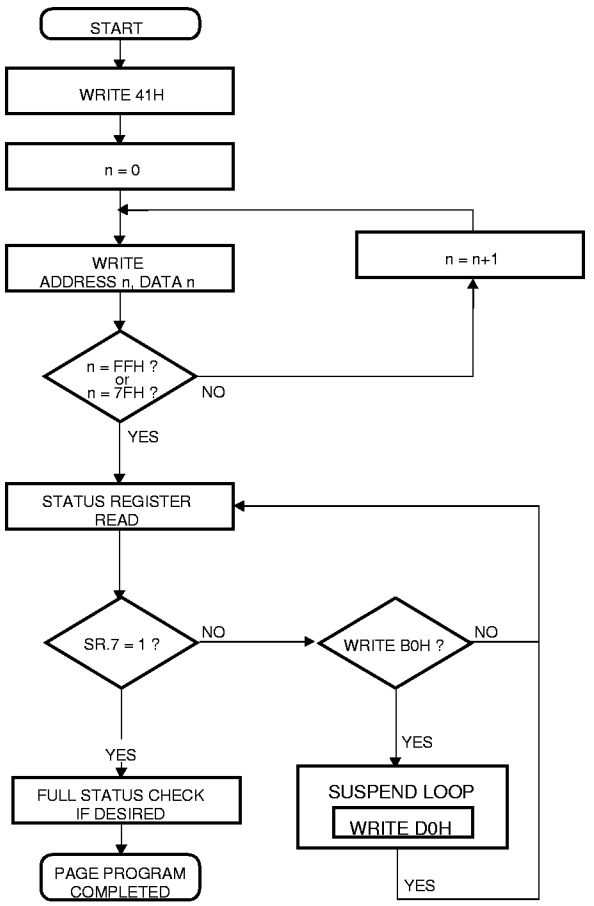
FULL STATUS CHECK PROCEDURE



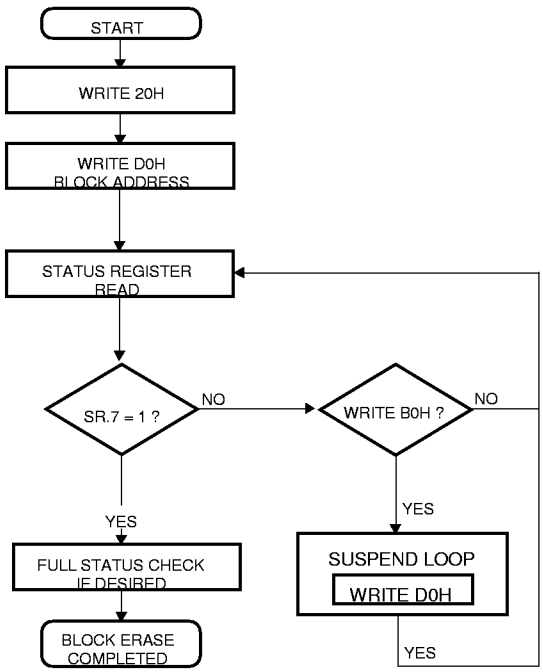
LOCK BIT PROGRAM FLOW CHART



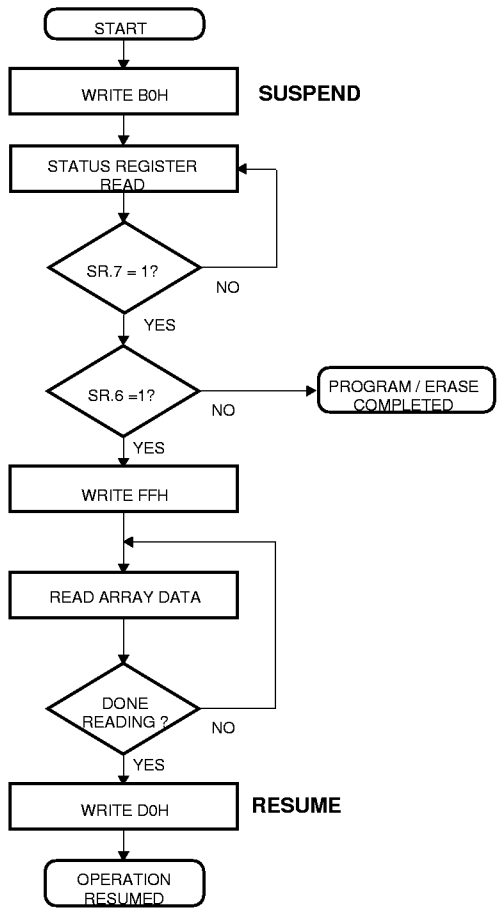
PAGE PROGRAM FLOW CHART



BLOCK ERASE FLOW CHART



SUSPEND / RESUME FLOW CHART



OPERATION STATUS and EFFECTIVE COMMAND