**TENTATIVE** TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

# 33,554,432-WORD BY 72-BIT SYNCHRONOUS DRAM MODULE

## DESCRIPTION

The THMY25E10C is a 33,554,432-word by 72-bit synchronous dynamic RAM module consisting of nine TC59SM808CFT DRAMs and PLL/Registers on a printed circuit board.

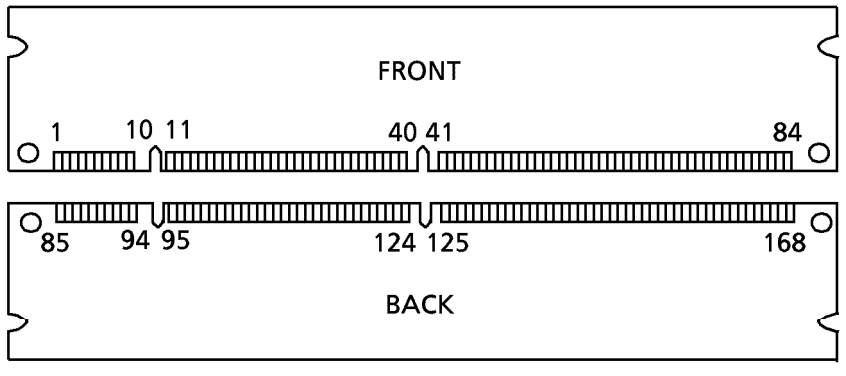
## FEATURES

- 33,554,432-word by 72-bit (single-bank) organization

| | | 70 | 75 | 80 |
|---|---|---|---|---|
| $t_{CK}$ | Clock Cycle Time (DIMM CL = 4) | 7 ns | 7.5 ns | 8 ns |
| $t_{RAS}$ | Active-to-Precharge Command Period (min) | 40 ns | 45 ns | 48 ns |
| $t_{AC}$ | Access Time from CLK (DIMM CL = 4) | 5.4 ns | 5.4 ns | 6 ns |
| $t_{RC}$ | Ref/Active-to-Ref/Active Command Period (min) | 56 ns | 65 ns | 68 ns |

- Single power supply of 3.3 V ± 0.3 V
- Pipeline architecture
- Auto-refresh and Self-refresh capability
- All inputs and outputs LVTTL-compatible
- 8192 refresh cycles per 64 ms
- Package: 168-pin DIMM Gold contacts
- Based on Intel PC133 Rev. 1.0 (70, 75)
- Based on Intel PC100 Rev. 1.2 (80)

## PIN ASSIGNMENT (TOP VIEW)




## PIN NAMES

| | |
|---|---|
| A0 to A12 | Address Inputs |
| BA0, 1 | Bank Select |
| DQ0 to DQ63 | Data Inputs / Outputs |
| CB0 to 7 | Check Bits |
| /CS0,2 | Chip Select |
| /RAS | Row Address Strobe |
| /CAS | Colum Address Strobe |
| /WE | Write Enable |
| DQMB0 to 7 | Output Disable / Write Mask |
| CLK0 to 3 | Clock Input |
| CKE | Clock Enable |
| REGE | Register Enable |
| SDA | Serial Data / Address for PD |
| SCL | Clock for PD |
| SA0 to 2 | Address for PD |
| WP | Write Protect for PD |
| VDD | Power (+3.3 V) |
| VSS | Ground |
| NC | No Connection |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VSS | 85 | VSS | 29 | DQMB1 | 113 | DQMB5 | 57 | DQ18 | 141 | DQ50 |
| 2 | DQ0 | 86 | DQ32 | 30 | /CS0 | 114 | NC | 58 | DQ19 | 142 | DQ51 |
| 3 | DQ1 | 87 | DQ33 | 31 | NC | 115 | /RAS | 59 | VDD | 143 | VDD |
| 4 | DQ2 | 88 | DQ34 | 32 | VSS | 116 | VSS | 60 | DQ20 | 144 | DQ52 |
| 5 | DQ3 | 89 | DQ35 | 33 | A0 | 117 | A1 | 61 | NC | 145 | NC |
| 6 | VDD | 90 | VDD | 34 | A2 | 118 | A3 | 62 | NC | 146 | NC |
| 7 | DQ4 | 91 | DQ36 | 35 | A4 | 119 | A5 | 63 | NC | 147 | REGE |
| 8 | DQ5 | 92 | DQ37 | 36 | A6 | 120 | A7 | 64 | VSS | 148 | VSS |
| 9 | DQ6 | 93 | DQ38 | 37 | A8 | 121 | A9 | 65 | DQ21 | 149 | DQ53 |
| 10 | DQ7 | 94 | DQ39 | 38 | A10 | 122 | BA0 | 66 | DQ22 | 150 | DQ54 |
| 11 | DQ8 | 95 | DQ40 | 39 | BA1 | 123 | A11 | 67 | DQ23 | 151 | DQ55 |
| 12 | VSS | 96 | VSS | 40 | VDD | 124 | VDD | 68 | VSS | 152 | VSS |
| 13 | DQ9 | 97 | DQ41 | 41 | VDD | 125 | CLK1 | 69 | DQ24 | 153 | DQ56 |
| 14 | DQ10 | 98 | DQ42 | 42 | CLK0 | 126 | A12 | 70 | DQ25 | 154 | DQ57 |
| 15 | DQ11 | 99 | DQ43 | 43 | VSS | 127 | VSS | 71 | DQ26 | 155 | DQ58 |
| 16 | DQ12 | 100 | DQ44 | 44 | NC | 128 | CKE | 72 | DQ27 | 156 | DQ59 |
| 17 | DQ13 | 101 | DQ45 | 45 | /CS2 | 129 | NC | 73 | VDD | 157 | VDD |
| 18 | VDD | 102 | VDD | 46 | DQMB2 | 130 | DQMB6 | 74 | DQ28 | 158 | DQ60 |
| 19 | DQ14 | 103 | DQ46 | 47 | DQMB3 | 131 | DQMB7 | 75 | DQ29 | 159 | DQ61 |
| 20 | DQ15 | 104 | DQ47 | 48 | NC | 132 | NC | 76 | DQ30 | 160 | DQ62 |
| 21 | CB0 | 105 | CB4 | 49 | VDD | 133 | VDD | 77 | DQ31 | 161 | DQ63 |
| 22 | CB1 | 106 | CB5 | 50 | NC | 134 | NC | 78 | VSS | 162 | VSS |
| 23 | VSS | 107 | VSS | 51 | NC | 135 | NC | 79 | CLK2 | 163 | CLK3 |
| 24 | NC | 108 | NC | 52 | CB2 | 136 | CB6 | 80 | NC | 164 | NC |
| 25 | NC | 109 | NC | 53 | CB3 | 137 | CB7 | 81 | WP | 165 | SA0 |
| 26 | VDD | 110 | VDD | 54 | VSS | 138 | VSS | 82 | SDA | 166 | SA1 |
| 27 | /WE | 111 | /CAS | 55 | DQ16 | 139 | DQ48 | 83 | SCL | 167 | SA2 |
| 28 | DQMB0 | 112 | DQMB4 | 56 | DQ17 | 140 | DQ49 | 84 | VDD | 168 | VDD |

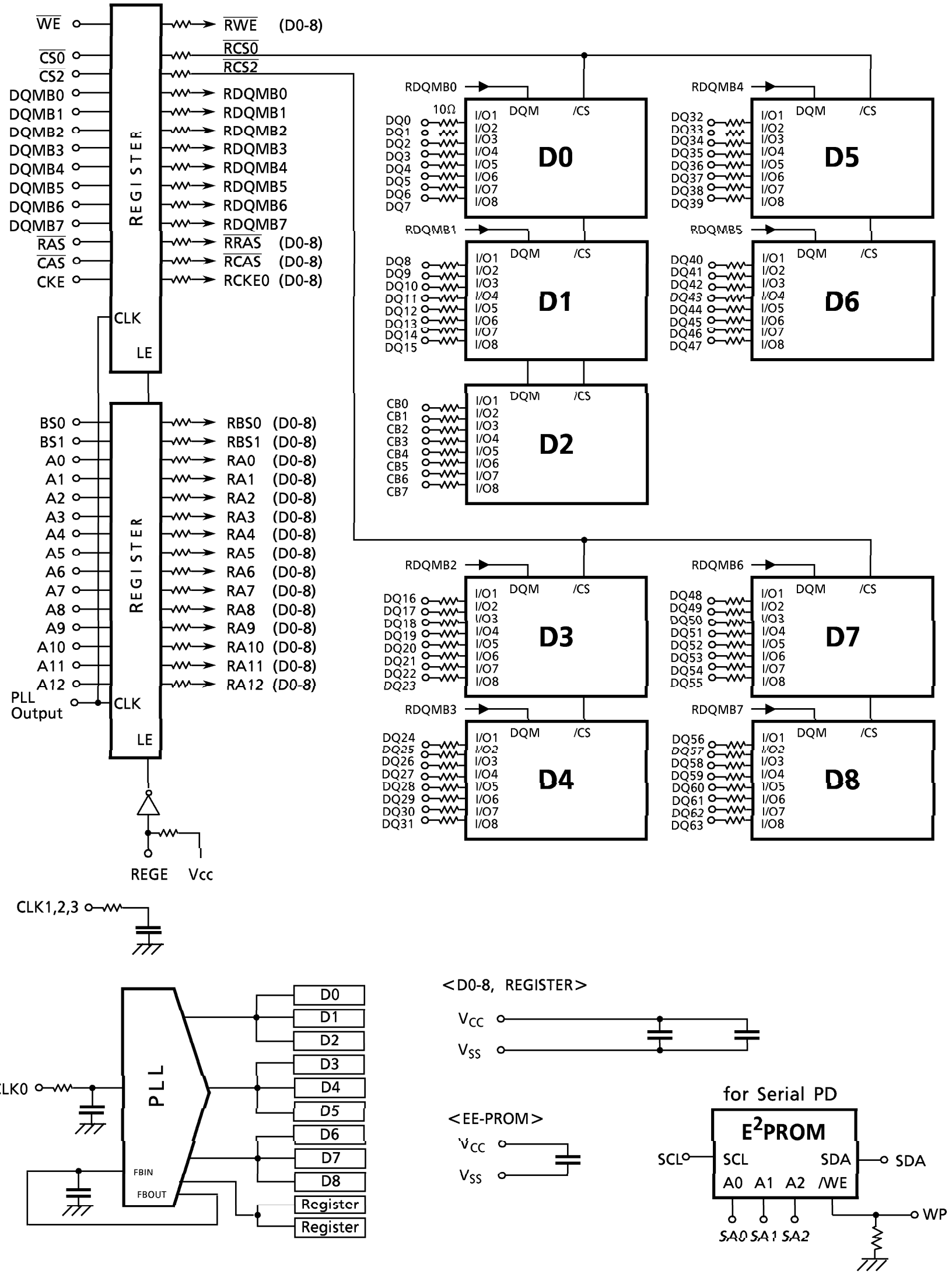
## SERIAL PRESENCE DETECT

| Byte Number | Function Described | 70 | | 75 | | 80 | |
|---|---|---|---|---|---|---|---|
| | | Entry Value | Entry | Entry Value | Entry | Entry Value | Entry |
| 0 | Defines # Bytes Written into Serial Memory at Module mfgr | 128 Bytes | 80h | 128 Bytes | 80h | 128 Bytes | 80h |
| 1 | Total # Bytes in SPD Memory Device | 256 Bytes | 08h | 256 Bytes | 08h | 256 Bytes | 08h |
| 2 | Fundamental Memory Type (FPM, EDO, SDRAM...) from Appendix A | SDRAM | 04h | SDRAM | 04h | SDRAM | 04h |
| 3 | # Row Addresses on this Assembly | RA0-RA12 | 0Dh | RA0-RA12 | 0Dh | RA0-RA12 | 0Dh |
| 4 | # Column Addresses on this Assembly | CA0-CA9 | 0Ah | CA0-CA9 | 0Ah | CA0-CA9 | 0Ah |
| 5 | # Module Banks on this Assembly | 1 Bank | 01h | 1 Bank | 01h | 1 Bank | 01h |
| 6 | Data Width of this Assembly... | x72 | 48h | x72 | 48h | x72 | 48h |
| 7 | ...Data Width Continuation | x72 | 00h | x72 | 00h | x72 | 00h |
| 8 | Voltage Interface Standard for this Assembly | LVTTL | 01h | LVTTL | 01h | LVTTL | 01h |
| 9 | SDRAM Cycle Time at Max. Supported CAS Latency (CL), CL = X | CL = 3, 7.0 ns | 70h | CL = 3, 7.5 ns | 75h | CL = 3, 8.0 ns | 80h |
| 10 | SDRAM Access from Clock @ CL = X | CL = 3, 5.0 ns | 50h | CL = 3, 5.4 ns | 54h | CL = 3, 6.0 ns | 60h |
| 11 | DIMM Configuration Type (Non-parity, Parity, ECC) | ECC | 02h | ECC | 02h | ECC | 02h |
| 12 | Refresh Rate/Type | 7.8 μs/Self-Refresh | 82h | 7.8 μs/Self-Refresh | 82h | 7.8 μs/Self-Refresh | 82h |
| 13 | SDRAM Width, Primary DRAM | x8 | 08h | x8 | 08h | x8 | 08h |
| 14 | Error Checking SDRAM Data Width | x8 | 08h | x8 | 08h | x8 | 08h |
| 15 | Minimum Clock Delay, Back-to-Back Random Column Addresses | 1 CLK | 01h | 1 CLK | 01h | 1 CLK | 01h |
| 16 | Burst Lengths Supported | 1,2,4,8 Full page | 8Fh | 1,2,4,8 Full page | 8Fh | 1,2,4,8 Full page | 8Fh |
| 17 | # Banks on Each SDRAM Device | 4 Banks | 04h | 4 Banks | 04h | 4 Banks | 04h |
| 18 | CAS # Latencies Supported | 2,3 | 06h | 2,3 | 06h | 2,3 | 06h |
| 19 | CS # Latency | | 01h | | 01h | | 01h |
| 20 | WE # Latency | | 01h | | 01h | | 01h |
| 21 | SDRAM Module Attributes | PLL (Clock)/ Registered | 16h | PLL (Clock)/ Registered | 16h | PLL (Clock)/ Registered | 16h |
| 22 | SDRAM Device Attributes: General | | 0Eh | | 0Eh | | 0Eh |
| 23 | Minimum Clock Cycle Time at CL- X-1 | CL = 2, 7.5 ns | 75h | CL = 2, 10 ns | A0h | CL = 2, 10 ns | A0h |
| 24 | Maximum Data Access Time from Clock @ CL X-1 | CL = 2, 5.4 ns | 54h | CL = 2, 6.0 ns | 60h | CL = 2, 6.0 ns | 60h |
| 25 | Minimum Clock Cycle Time at CL X-2 | | 00h | | 00h | | 00h |
| 26 | Maximum Data Access Time from Clock @ CL X-2 | | 00h | | 00h | | 00h |
| 27 | Minimum Row Precharge Time | 15 ns | 0Fh | 20 ns | 14h | 20 ns | 14h |
| 28 | Minimum Row Active to Row Active Delay | 15 ns | 0Fh | 15 ns | 0Fh | 20 ns | 14h |
| 29 | Minimum RAS-to-CAS Delay | 15 ns | 0Fh | 20 ns | 14h | 20 ns | 14h |
| 30 | Minimum RAS Pulse Width | 42 ns | 2Ah | 45 ns | 2Dh | 48 ns | 30h |
| 31 | Module/Bank Density | 256 MB | 40h | 256 MB | 40h | 256 MB | 40h |
| 32 | Command & Address signal input Setup Time | 1.5 ns | 15h | 1.5 ns | 15h | 2.0 ns | 20h |
| 33 | Command & Address signal input Hold Time | 0.8 ns | 08h | 0.8 ns | 08h | 1.0 ns | 10h |
| 34 | Data signal input Setup Time | 1.5 ns | 15h | 1.5 ns | 15h | 2.0 ns | 20h |
| 35 | Data signal input Hold Time | 0.8 ns | 08h | 0.8 ns | 08h | 1.0 ns | 10h |
| 36-61 | Superset Information (May Be Used in Future) | | 00h | | 00h | | FFh |
| 62 | SPD Revision | JEDEC Rev.2 | 02h | JEDEC Rev.2 | 02h | Rev. 1.2A | 12h |
| 63 | Checksum for Bytes 0-62 | 49Dh | 9Dh | 4EAh | EAh | 1F25h | 25h |

## OPTION

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 64 | Manufacturers JEDEC ID Code per JEP-106E | | | | | | |
| 65-71 | | | | | | | |
| 72 | Manufacturing Location | | | | | | |
| 73-90 | Manufacturer's Part Number | | | | | | |
| 91-92 | Revision Code | | | | | | |
| 93-94 | Date of Manufacture | | | | | | |
| 95-98 | Assembly Serial Number | | | | | | |
| 99-125 | Manufacturer-Specific Data | | | | | | |
| 126 | Reserved | JEDEC Rev.02 | 64h | JEDEC Rev.02 | 64h | Intel Specification | 64h |
| 127 | Reserved | | 87h | | 87h | Intel Specification | 87h |
| 128-255 | | | | | | | |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | ITEM | RATING | UNIT | NOTES |
|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | – 0.3 to $V_{CC}$ + 0.3 | V | 1 |
| $V_{OUT}$ | Output Voltage | – 0.3 to $V_{CC}$ + 0.3 | V | 1 |
| $V_{DD}$ | Power Supply Voltage | – 0.3 to 4.6 | V | 1 |
| $T_{OPR}$ | Operating Temperature | 0 to 70 | °C | 1 |
| $T_{STG}$ | Storage Temperature | – 55 to 125 | °C | 1 |
| $P_D$ | Power Dissipation | 7.4 | W | 1 |
| $I_{OUT}$ | Short Circuit Output Current | 50 | mA | 1 |

## RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° to 70°C)

| SYMBOL | PARAMETER | MIN | TYP. | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V | 2 |
| $V_{IH}$ | LVTTL Input High Voltage | 2.0 | – | $V_{DD}$ + 0.3 | V | 2 |
| $V_{IL}$ | LVTTL Input Low Voltage | – 0.3 | – | 0.8 | V | 2 |

## CAPACITANCE ($V_{CC}$ = 3.3 V, f = 1 MHz, Ta = 25°C)

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $C_I$ | Input Capacitance (A0 to A11) | – | 10 | pF |
| $C_2$ | Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0,1) | – | 10 | pF |
| $C_3$ | Input Capacitance (CLK0 to 3) | – | 28 | pF |
| $C_4$ | Input Capacitance ($\overline{CS0}$ to 2) | – | 10 | pF |
| $C_5$ | Input Capacitance (DQMB0 to 7) | – | 10 | pF |
| $C_6$ | Input Capacitance ($\overline{CKE}$) | – | 10 | pF |
| $C_{DQ}$ | I / O Capacitance (DQ0 to DQ63, CB0 to 7) | – | 15 | pF |

## DC CHARACTERISTICS ($V_{CC}$ = 3.3 V ± 0.3 V, Ta = 0° to 70°C)

| SYMBOL | ITEM | | 70 | | 75 | | 80 | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| $I_{CC1}$ | OPERATING CURRENT<br>Active-Precharge Command Cycling without Burst Operation<br>($t_{CK}$ = min, $t_{RC}$ = min) | 1-Bank Operation | – | 1843 | – | 1798 | – | 1392 | mA | |
| $I_{CC2}$ | STANDBY CURRENT<br>($t_{CK}$ = min, $\overline{CS}$ = $V_{IH}$,<br>$V_{IH/L}$ = $V_{IH}$ (min) / $V_{IL}$ (max)<br>Bank: Inactive State) | CKE = $V_{IH}$ | – | 675 | – | 630 | – | 508 | mA | 3, 5-A |
| $I_{CC2P}$ | | CKE = $V_{IL}$<br>(Power-down Mode) | – | 324 | – | 324 | – | 247 | | |
| $I_{CC2S}$ | STANDBY CURRENT<br>(CLK = $V_{IL}$, CS = $V_{IH}$,<br>$V_{IH/L}$ = $V_{IH}$ (min) / $V_{IL}$ (max)<br>Bank: Inactive State) | CKE = $V_{IH}$ | – | 116 | – | 116 | – | 116 | mA | 5-A |
| $I_{CC2PS}$ | | CKE = $V_{IL}$<br>(Power-down Mode) | – | 35 | – | 35 | – | 35 | | |
| $I_{CC3}$ | NO OPERATING CURRENT<br>($t_{CK}$ = min, $\overline{CS}$ = $V_{IH}$ (min)<br>Bank: Active State (4 banks)) | CKE = $V_{IH}$ | – | 855 | – | 810 | – | 688 | mA | 3, 5-B |
| $I_{CC4}$ | BURST OPERATING CURRENT<br>($t_{CK}$ = min, $\overline{CS}$ = $V_{IH}$ (min), Read/Write Command Cycling) | | – | 1215 | – | 1170 | – | 1048 | mA | 3, 4 |
| $I_{CC5}$ | AUTO-REFRESH CURRENT<br>($t_{CK}$ = min, $t_{RC}$ = min, Auto-Refresh Command Cycling) | | – | 1845 | – | 1755 | – | 1588 | mA | 3 |
| $I_{CC6}$ | SELF-REFRESH CURRENT<br>(Self-Refresh Mode, CKE = 0.2 V) | | – | 53 | – | 53 | – | 53 | mA | 3, 5-C |
| $I_{I(L)}$ | INPUT LEAKAGE CURRENT<br>(0 V ≦ $V_{IN}$ ≦ $V_{DD}$, All Other Pins Not under Test = 0 V) | | – 5 | 5 | – 5 | 5 | – 5 | 5 | μA | |
| $I_{O(L)}$ | OUTPUT LEAKAGE CURRENT<br>($D_{OUT}$ Is Disabled, 0 V ≦ $V_{OUT}$ ≦ $V_{DD}$) | | – 5 | 5 | – 5 | 5 | – 5 | 5 | μA | |
| $V_{OH}$ | OUTPUT LEVEL<br>LVTTL Output H Level Voltage ($I_{OUT}$ = – 2 mA) | | 2.4 | – | 2.4 | – | 2.4 | – | V | |
| $V_{OL}$ | OUTPUT LEVEL<br>LVTTL Output L Level Voltage ($I_{OUT}$ = 2 mA) | | – | 0.4 | – | 0.4 | – | 0.4 | V | |

## AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

($V_{CC}$ = 3.3 V ± 0.3 V, Ta = 0° to 70°C) (Notes 5, 6, 7)

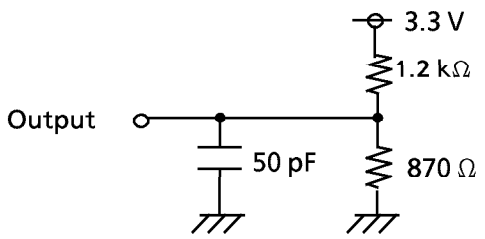
| SYMBOL | PARAMETER | | 70 | | 75 | | 80 | | UNIT | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| $t_{RC}$ | Ref/Active-Ref/Active Command Period | | 56 | – | 65 | – | 68 | – | ns | 10 |
| $t_{RAS}$ | Active- Precharge Command Period | | 40 | 100000 | 45 | 100000 | 48 | 100000 | | |
| $t_{RCD}$ | Active-Read/Write Command Delay Time | | 15 | – | 20 | – | 20 | – | | |
| $t_{CCD}$ | Read/Write(a) -Read/Write(b) Command Period | | 1 | – | 1 | – | 1 | – | cycle | |
| $t_{RP}$ | Precharge-Active Command Period | | 15 | – | 20 | – | 20 | – | ns | |
| $t_{RRD}$ | Active(a)-Active(b) Command Period | | 15 | – | 15 | – | 20 | – | | |
| $t_{WR}$ | Write Recovery Time | CL* = 3 | 7.5 | – | 10 | – | 10 | – | | |
| | | CL* = 4 | 7 | – | 7.5 | – | 8 | – | | |
| $t_{CK}$ | CLK Cycle Time | CL* = 3 | 7.5 | 20 | 10 | 20 | 10 | 20 | | |
| | | CL* = 4 | 7 | 20 | 7.5 | 20 | 8 | 20 | | |
| $t_{CH}$ | CLK High Level Width | | 2.5 | – | 2.5 | – | 3 | – | | 11 |
| $t_{CL}$ | CLK Low Level Width | | 2.5 | – | 2.5 | – | 3 | – | | |
| $t_{AC}$ | Access Time from CLK | CL* = 3 | – | 5.4 | – | 6 | – | 6 | | |
| | | CL* = 4 | – | 5.4 | – | 5.4 | – | 6 | | |
| $t_{OH}$ | Output Data Hold Time | | 3 | – | 3 | – | 3 | – | | |
| $t_{HZ}$ | Output Data High Impedance Time | | 3 | 7 | 3 | 7.5 | 3 | 8 | | 9 |
| $t_{LZ}$ | Output Data Low Impedance Time | | 0 | – | 0 | – | 0 | – | | |
| $t_{SB}$ | Power-down Mode Entry Time | | 0 | 7 | 0 | 7.5 | 0 | 8 | | |
| $t_T$ | Transition Time of CLK (Rise and Fall) | | 0.5 | 10 | 0.5 | 10 | 0.5 | 10 | | |
| $t_{DS}$ | Data-in Set-up Time | | 1.5 | – | 1.5 | – | 2 | – | | |
| $t_{DH}$ | Data-in Hold Time | | 0.8 | – | 0.8 | – | 1 | – | | |
| $t_{AS}$ | Address Set-up Time | | 1.5 | – | 1.5 | – | 2 | – | | |
| $t_{AH}$ | Address Hold Time | | 0.8 | – | 0.8 | – | 1 | – | | |
| $t_{CKS}$ | CKE Set-up Time | | 1.5 | – | 1.5 | – | 2 | – | | |
| $t_{CKH}$ | CKE Hold Time | | 0.8 | – | 0.8 | – | 1 | – | | |
| $t_{CMS}$ | Command Set-up Time | | 1.5 | – | 1.5 | – | 2 | – | | |
| $t_{CMH}$ | Command Hold Time | | 0.8 | – | 0.8 | – | 1 | – | | |
| $t_{REF}$ | Refresh Time | | – | 64 | – | 64 | – | 64 | ms | |
| $t_{RSC}$ | Mode Register Set Cycle Time | | 14 | – | 15 | – | 16 | – | ns | 9 |

* CL is $\overline{CAS}$ latency. (DIMM Level)

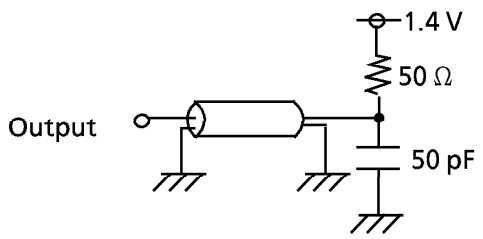
NOTES:

1. Conditions outside the limits listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltages are referenced to Vss.
3. These parameters depend on the cycle rate and their values are measured at the minimum cycle rate value $t_{CK}$ and $t_{RC}$. Input signals are changed once during $t_{CK}$.
4. These parameters depend on the output loading. The specified values are obtained with the output open.
5. These values are measured under the following conditions.
   - -A Address, BA, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are fixed High level, and DQMB is fixed Low level.
   - -B After bank active, Address, BA, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are fixed High level, and DQMB is fixed Low level.
   - -C Under self refresh, CLK is fixed Low level, and Address, BA, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are fixed High level, and DQMB is fixed Low level.
6. The power-up sequence is described in Note 12.
7. AC TEST CONDITIONS

| | |
|---|---|
| Reference Level of Output Signals | 1.4 V / 1.4 V |
| Output Load | See the diagram for AC Test Load (B) below |
| Input Signal Levels | 2.4 V / 0.4 V |
| Transition Time (Rise and Fall) of Input Signals | 2 ns |
| Reference Level of Input Signals | 1.4 V |



AC TEST LOAD (A)



AC TEST LOAD (B)

8. Transition times are measured between the $V_{IH}$ and $V_{IL}$ levels. The transition (rise and fall) of input signals has a fixed slope.
9. $t_{HZ}$ defines the time at which the outputs go open circuit and are not reference levels.
10. These parameters depend on the number of clock cycles and depend on the operating frequency of the clock as follows:

    Number of clock cycles = Specified value of timing / Clock period
    (Round up fractions to a whole number.)

11. $t_{CH}$ is the pulse width of CLK measured from the positive edge to the negative edge and referenced to $V_{IH}$ (min). $t_{CL}$ is the pulse width of CLK measured from the negative edge to the positive edge and referenced to $V_{IL}$ (max).

12. Power-up Sequence

Power-up must be performed in the following sequence.

1) Power must be applied to $V_{DD}$ with all input signals held in the NOP state. The CLK signal must be started at the same time as power is applied.

2) After power-up a pause of at least 200 $\mu$seconds is required. Then, DQMB and CKE must be held High (at the $V_{DD}$ level) to ensure that the DQ and CB outputs are high-impedance.

3) Both banks must be precharged.

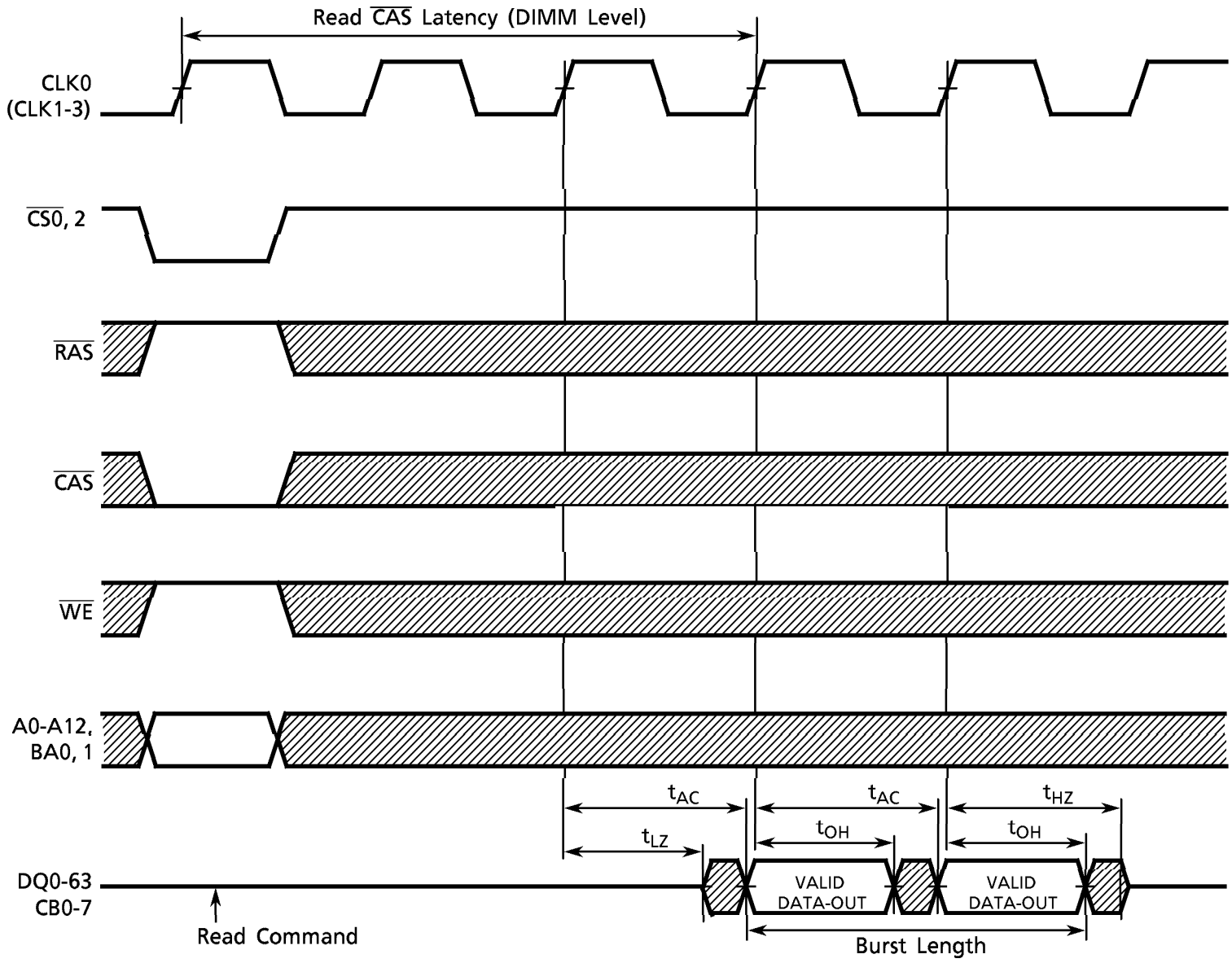
4) The Mode Register Set command must be asserted to initialize the Mode register.

5) An Auto-Refresh operation must consist of at least eight Auto-Refresh cycles.

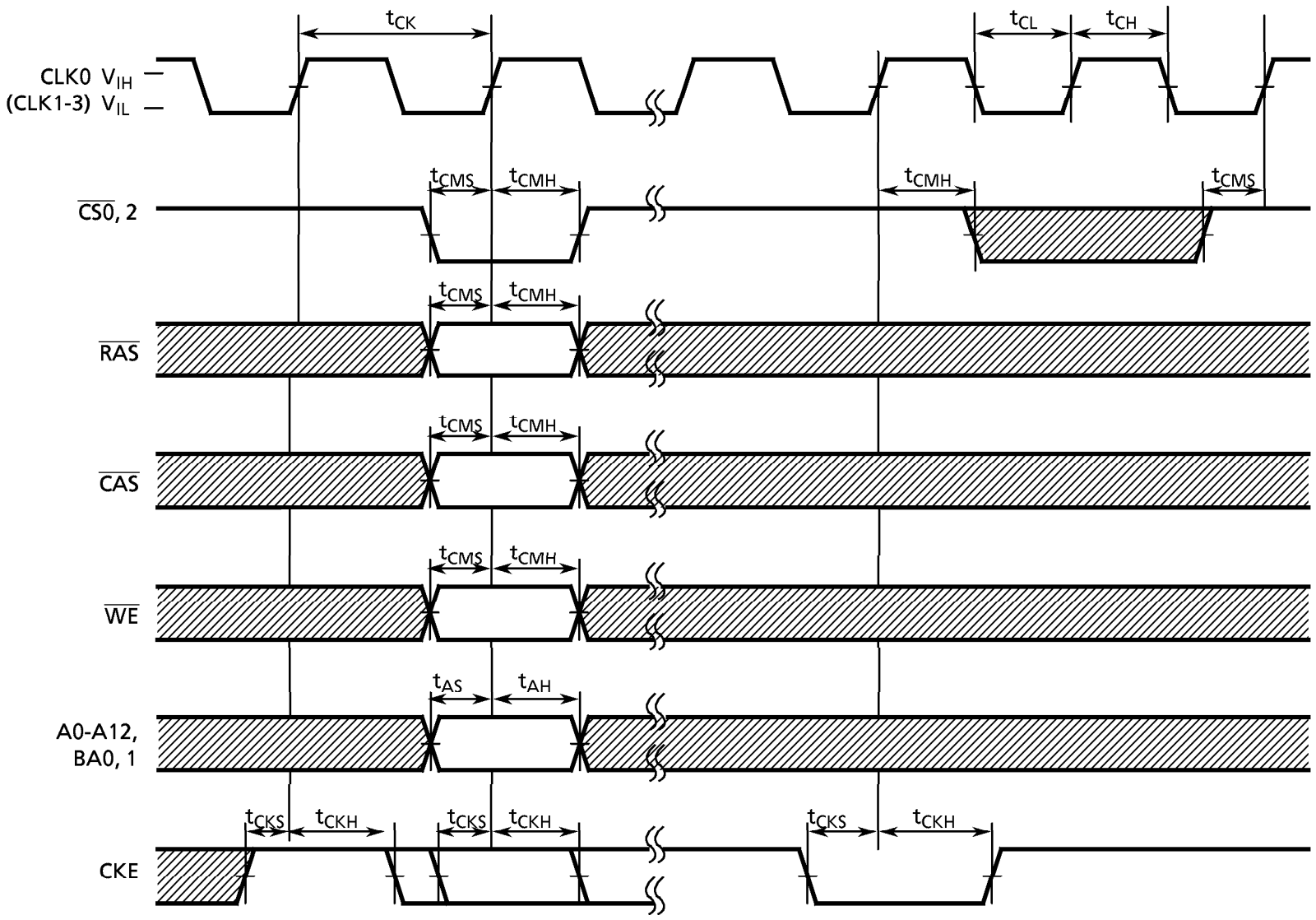
The order in which 4) and 5) are performed is interchangeable.

## TIMING DIAGRAMS

### Read Timing

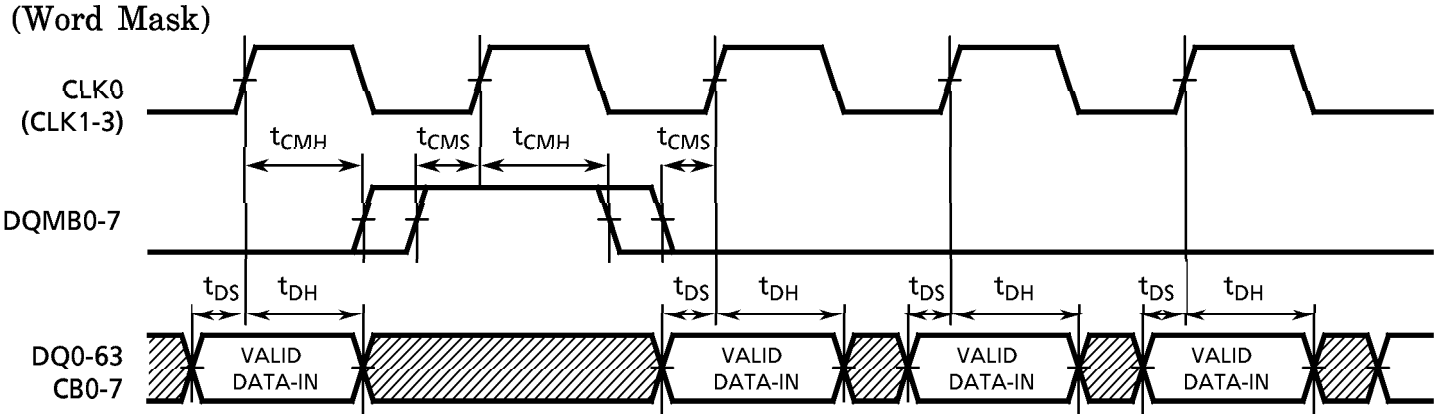


## Command Input Timing

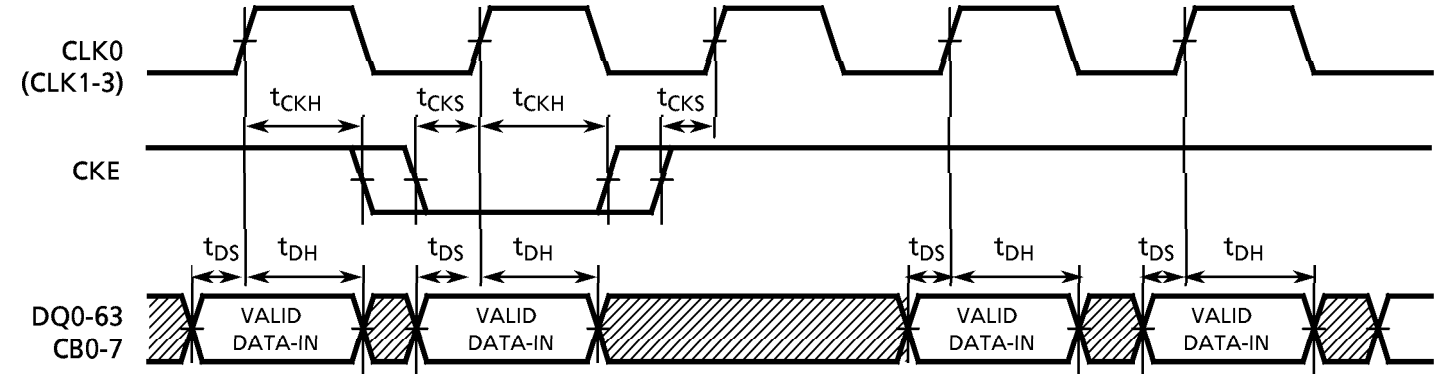


## Control Timing for Input Data

(Word Mask)

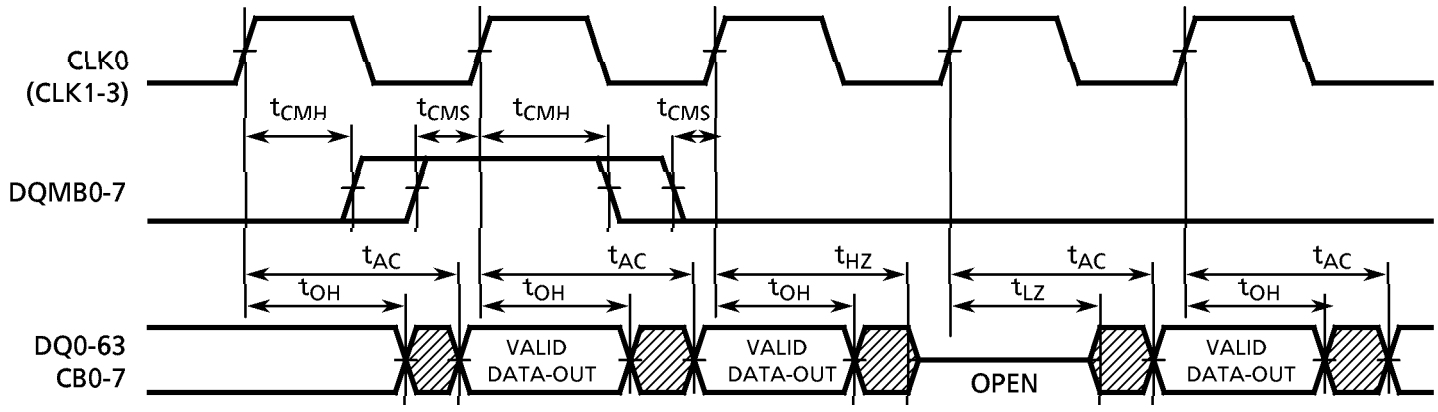



(Clock Mask)

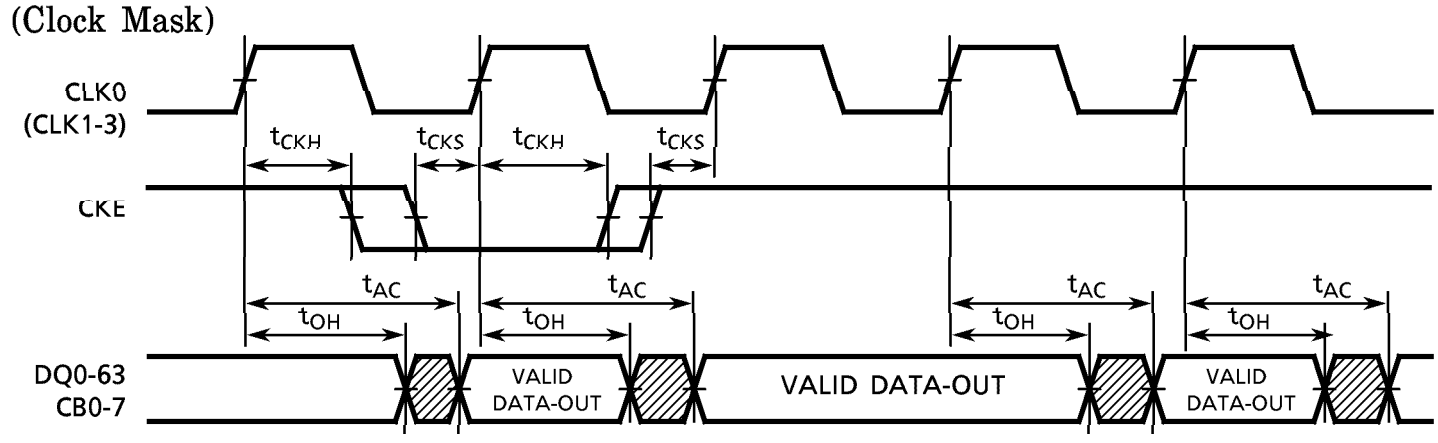



## Control Timing for Output Data

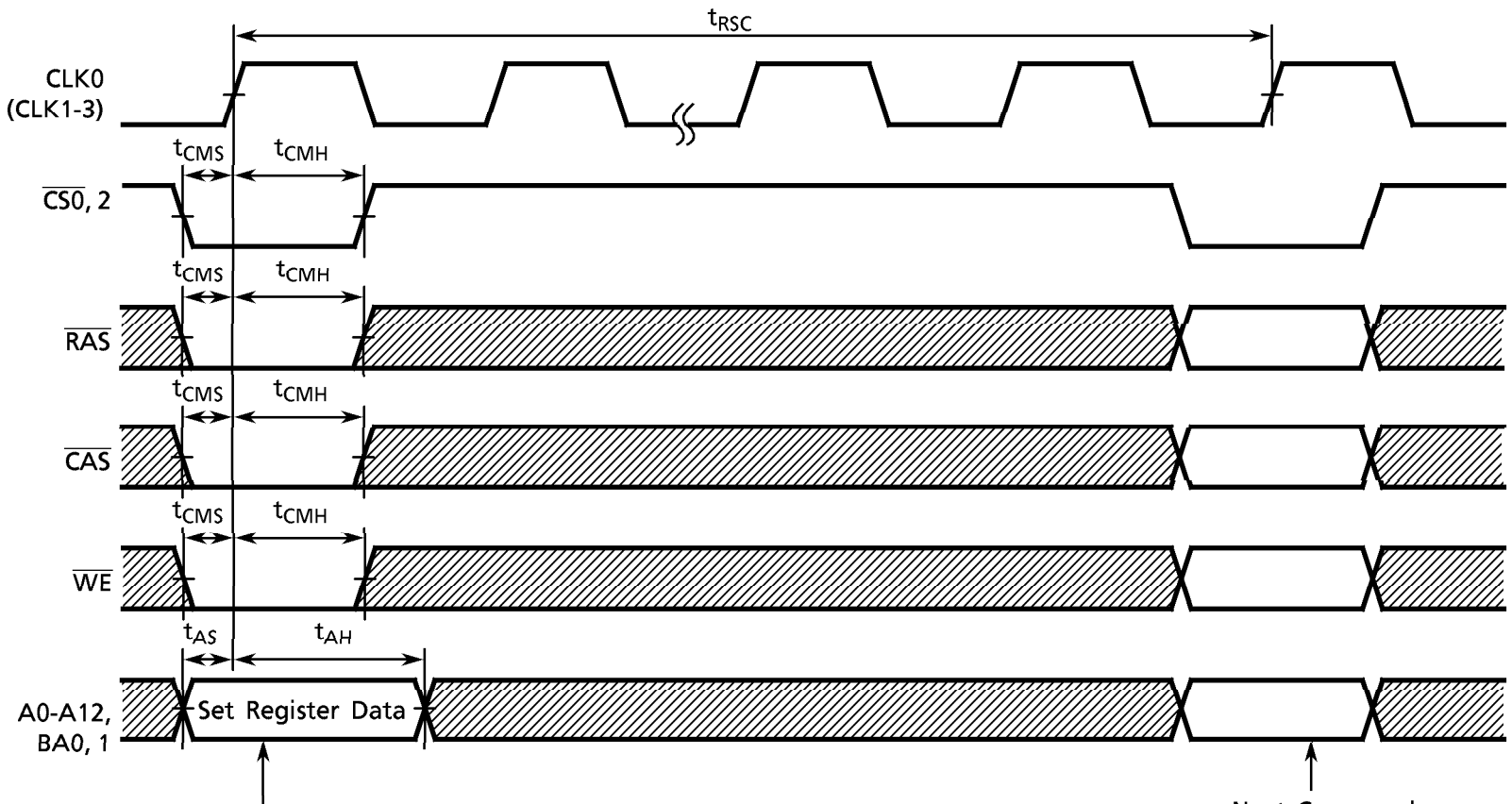
(Output Enable)




(Clock Mask)



## Mode Register Set Cycle




| | | |
|---|---|---|
| A0 | Burst Length | |
| A1 | | |
| A2 | | |
| A3 | Addressing Mode | |
| A4 | CAS Latency | |
| A5 | | |
| A6 | | |
| A7 | 0 | (Test Mode) |
| A8 | 0 | Reserved |
| A9 | Write Mode | |
| A10 | 0 | Reserved |
| A11 | 0 | |
| A12 | 0 | |
| BA0 | 0 | |
| BA1 | 0 | |

| | | | Burst Length | |
|---|---|---|---|---|
| A2 | A1 | A0 | Sequential | Interleave |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | Full Page | |

| A3 | Addressing Mode |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

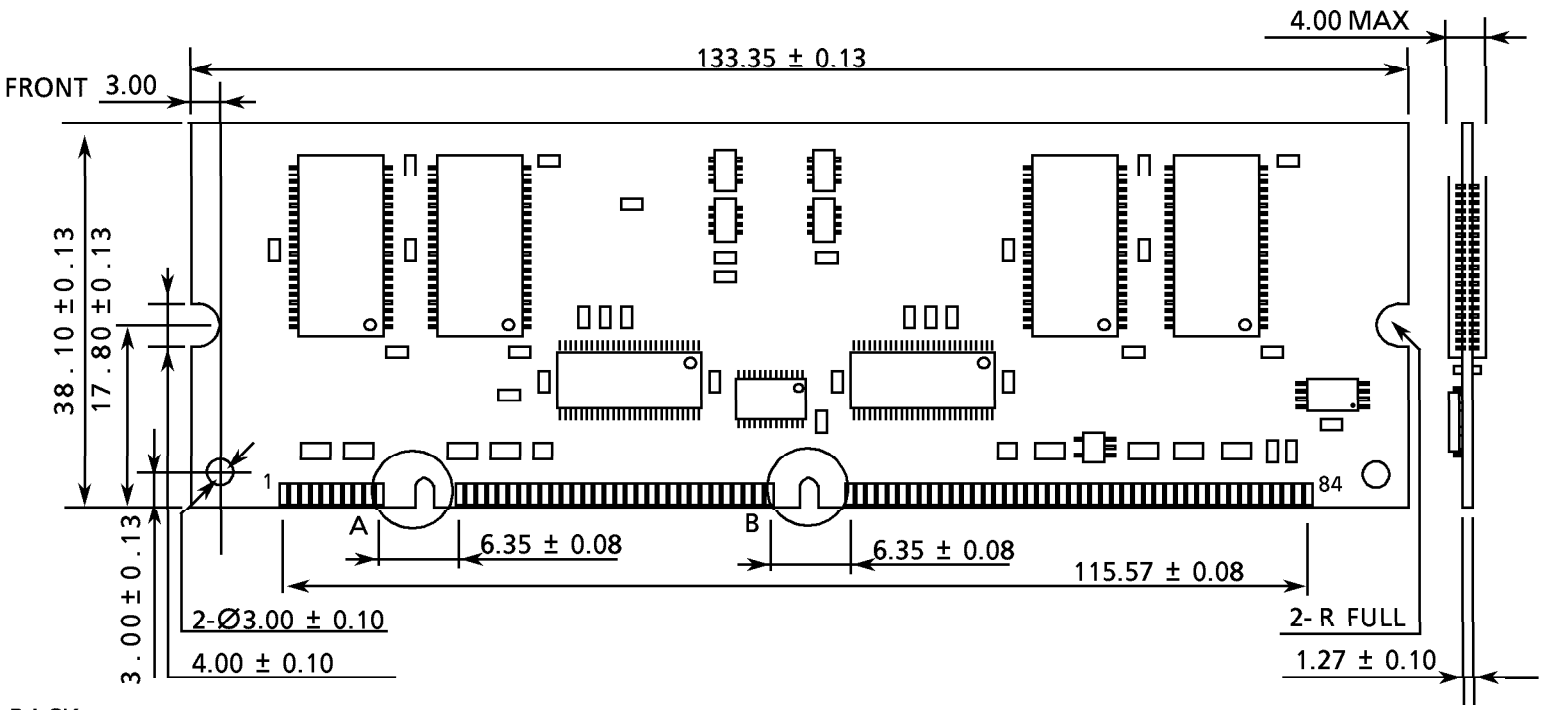
| A6 | A5 | A4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |

DIMM Level

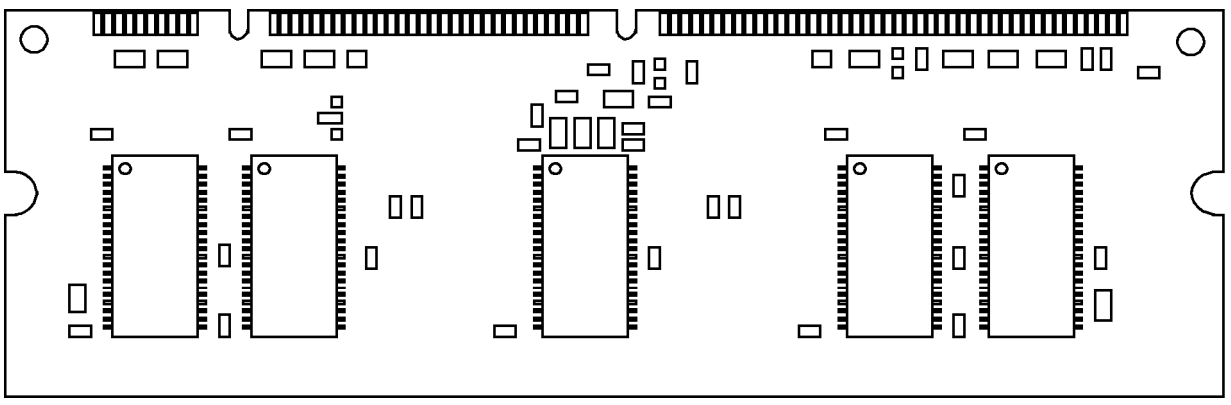
| A9 | Single-Write Mode |
|---|---|
| 0 | Burst Read and Burst Write |
| 1 | Burst Read and Single Write |

**PACKAGE DIMENSIONS** (THMY25E10C)

Unit: mm

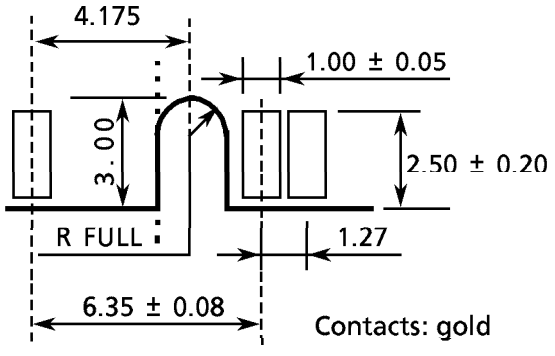



BACK



CONTACT DIMENSIONS

A: Registered keying




B: 3.3-V keying