Am25LS194A • Am54LS/74LS194A
Am25LS195A • Am54LS/74LS195A

Four-Bit High-Speed Shift Registers

DISTINCTIVE CHARACTERISTICS

- Shift right or parallel load with JK inputs on Am25LS195A
- Shift left, right, parallel load or do nothing on Am25LS194A
- Fully synchronous shifting and parallel loading
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL}
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am25LS194A and Am25LS195A are 4-bit registers that exhibit fully synchronous operation in all operating modes. The Am25LS195A can either parallel load all four register bits via the parallel inputs (A, B, C, D) or shift each of the four register bits right one place. The shifting or parallel loading is under control of the shift/load input (S/L). When the shift/load input is LOW, data is loaded from the parallel data inputs; when the shift/load input is HIGH, data is loaded from the register bits on the left. The first bit, Q_A, is loaded via the J and $\overline{K}$ inputs in the shift mode.

The Am25LS194A operates in four modes under control of the two select inputs, S_0 and S_1. The four modes are parallel load (data comes from the parallel inputs), shift right (data comes from the flip-flop to the left, with the Q_A bit input from R), shift left (data comes from the flip-flop to the right, with the Q_D input from L), and hold or do nothing (each flip-flop receives data from its own output).

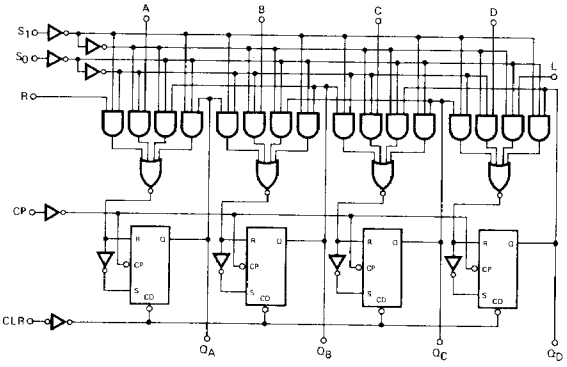
For both devices the outputs change state synchronously following a LOW-to-HIGH transition on the clock input, CP. Both devices have an active-LOW synchronous clear (CLR) which forces all outputs to the LOW state ($\overline{Q}_D$ HIGH) independent of any other inputs.

Because all the flip-flops are D-type they do not catch 0's or 1's, and the only requirements on any inputs is that they meet the short set-up and hold time intervals with respect to the clock LOW-to-HIGH transition.

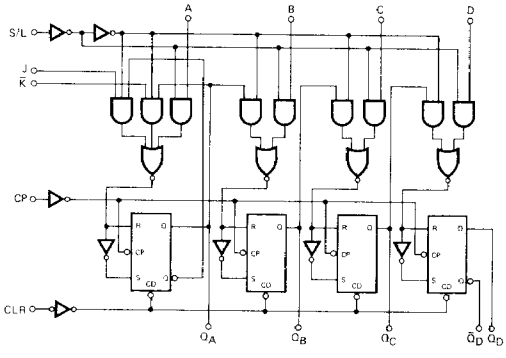
The Am54LS/74LS194A and 195A are standard performance versions of the Am25LS194A and 195A. See appropriate electrical characteristic tables for detailed Am25LS improvements.

LOGIC DIAGRAMS

'LS194A



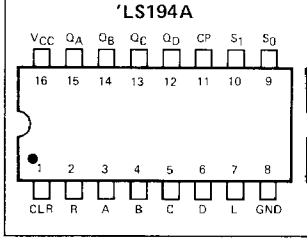
'LS195A



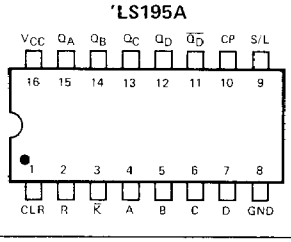
CONNECTION DIAGRAMS

Top Views

'LS194A

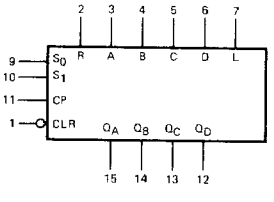


'LS195A

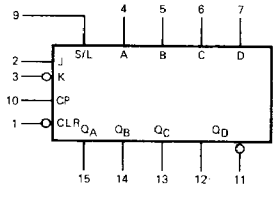


LOGIC SYMBOLS

'LS194A



'LS195A



V_{CC} = Pin 16
GND = Pin 8

Am25LS194A • Am25LS195A

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 4mA			0.4	Volts
			I_{OL} = 8mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	LS194A (Note 4)		15	23	mA
			LS195A (Note 5)		14	21	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open. Inputs A, B, C, D grounded. Inputs S_0, S_1, Clear, L, R, at 4.5 V. Measured after a momentary ground, then 4.5 V applied to clock.
5. Outputs open. S/L grounded. A, B, C, D, J, $\overline{K}$ at 4.5 V. Measured after applying a momentary ground then 4.5 V to the clear followed by ground then 4.5 V to clock.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Am54LS/74LS194A • Am54LS/74LS195A
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	Am74LS	2.7	3.4		Volts
			Am54LS	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	All, I_{OL} = 4mA			0.4	Volts
			74LS only, I_{OL} = 8mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	Am54LS			0.7	Volts
			Am74LS			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	LS194A (Note 4)		15	23	mA
			LS195A (Note 5)		14	21	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open. Inputs A, B, C, D grounded. Inputs S_0, S_1, Clear, L, R, at 4.5V. Measured after a momentary ground, then 4.5V applied to clock.
5. Outputs open. S/L grounded. A, B, C, D, J, $\overline{K}$ at 4.5V. Measured after applying a momentary ground then 4.5V to the clear followed by ground then 4.5V to clock.

Am25LS194A • Am54LS/74LS194A
SWITCHING CHARACTERISTICS

($T_A = 25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	Clock to Output		13	21		14	22	ns	$C_L = 15pF$, $R_L = 2.0k\Omega$
t_{PHL}	Clock to Output		12	18		17	26	ns	
t_{PHL}	Clear to Output		17	26		19	30	ns	
t_{pw}	Clock Pulse Width	17			20			ns	
t_{pw}	Clear Pulse Width	17			20			ns	
t_s	Mode Control Set-up Time	25			30			ns	
t_s	Data Input Set-up Time	16			20			ns	
t_s	Clear Recovery to Clock	20			25			ns	
t_h	Data Hold Time	0			0			ns	
f_{max} (Note 1)	Maximum Clock Frequency	35	55		25	36		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS194A ONLY
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Min.	Am25LS COM'L Max.	Am25LS MIL $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output		31		36	ns	$C_L = 50pF$, $R_L = 2.0k\Omega$
t_{PHL}	Clock to Output		28		32	ns	
t_{PHL}	Clear to Output		38		44	ns	
t_{pw}	Clock Pulse Width	26		30		ns	
t_{pw}	Clear Pulse Width	26		30		ns	
t_s	Mode Control Set-up Time	37		42		ns	
t_s	Data Input Set-up Time	25		29		ns	
t_s	Clear Recovery to Clock	30		35		ns	
t_h	Data Hold Time	4		5		ns	
f_{max} (Note 1)	Maximum Clock Frequency	26		23		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS195A • Am54LS/74LS195 SWITCHING CHARACTERISTICS

($T_A = 25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	Clock to Output		13	21		14	22	ns	$C_L = 15pF$, $R_L = 2.0k\Omega$
t_{PHL}	Clock to Output		12	18		17	26	ns	
t_{PHL}	Clear to Output		17	26		19	30	ns	
t_{pw}	Clock Pulse Width	16			16			ns	
t_{pw}	Clear Pulse Width	12			12			ns	
t_s	Mode Control Set-up Time	25			25			ns	
t_s	Data Input Set-up Time	15			15			ns	
t_s	Clear Recovery to Clock	20			25			ns	
t_h	Data Hold Time	0			0			ns	
t_R	Shift/Load Release Time Am54LS/74LS195A Only			0			0	ns	
f_{max} (Note 1)	Maximum Clock Frequency	35	55		30	39		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS195A ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L Min. ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$)	Am25LS COM'L Max.	Am25LS MIL Min. ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$)	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output		31		36	ns	$C_L = 50pF$, $R_L = 2.0k\Omega$
t_{PHL}	Clock to Output		27		32	ns	
t_{PHL}	Clear to Output		38		44	ns	
t_{pw}	Clock Pulse Width	25		29		ns	
t_{pw}	Clear Pulse Width	20		23		ns	
t_s	Mode Control Set-up Time	37		42		ns	
t_s	Data Input Set-up Time	24		27		ns	
t_s	Clear Recovery to Clock	30		35		ns	
t_h	Data Hold Time	4		5		ns	
t_R	Shift/Load Release Time Am54LS/74LS195A Only		4		5	ns	
f_{max} (Note 1)	Maximum Clock Frequency	26		23		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

'LS194A FUNCTION TABLE

FUNCTION	Clear	Mode S_1	Mode S_0	Clock	Serial Left	Serial Right	Parallel A	Parallel B	Parallel C	Parallel D	OUTPUTS Q_A	Q_B	Q_C	Q_D
Clear	L	X	X	X	X	X	X	X	X	X	L	L	L	L
No Change	H	X	X	L	X	X	X	X	X	X	NC	NC	NC	NC
	H	X	X	H	X	X	X	X	X	X	NC	NC	NC	NC
Parallel Load	H	H	H	↑	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
Shift Right	H	L	H	↑	X	L	X	X	X	X	L	Q_A	Q_B	Q_C
	H	L	H	↑	X	H	X	X	X	X	H	Q_A	Q_B	Q_C
Shift Left	H	H	L	↑	L	X	X	X	X	X	Q_B	Q_C	Q_D	L
	H	H	L	↑	H	X	X	X	X	X	Q_B	Q_C	Q_D	H
Hold	H	L	L	X	X	X	X	X	X	X	NC	NC	NC	NC

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
D_i = May be a HIGH or a LOW and the respective output will assume the same state.

'LS195A FUNCTION TABLE

Clear	Shift/Load	Clock	Serial J	Serial $\overline{K}$	Parallel A	Parallel B	Parallel C	Parallel D	OUTPUTS Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	X	L	X	X	X	X	X	X	NC	NC	NC	NC	NC
H	X	H	X	X	X	X	X	X	NC	NC	NC	NC	NC
H	L	↑	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3	$\overline{D}_3$
H	H	↑	L	H	X	X	X	X	Q_A	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	L	L	X	X	X	X	L	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	H	H	X	X	X	X	H	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_A$	Q_A	Q_B	Q_C	$\overline{Q}_C$

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
D_i = May be a HIGH or a LOW and the respective output will assume the same state.

Notes: 1. If the J and $\overline{K}$ inputs are tied together, the common line becomes a D-Type input to the first bit in the shift mode.
2. Linear feedback shift counters can be made by connecting the Q_D and $\overline{Q}_D$ outputs to the $\overline{K}$ and J inputs, respectively.

DEFINITION OF FUNCTIONAL TERMS

J, $\overline{K}$ The logic inputs used for controlling the Q_A flip-flop of the Am25LS195A register when S/L is HIGH.

CLR Clear. The asynchronous master reset input.

CP Clock pulse for the register. Enters data on the LOW-to-HIGH transition.

S/L Shift/Load. The input for selection of parallel or serial shifting for the Am25LS195A register. S/L LOW selects parallel entry.

S_0, S_1 The mode select inputs of the Am25LS194A.

A, B, C, D The four parallel data inputs for the register.

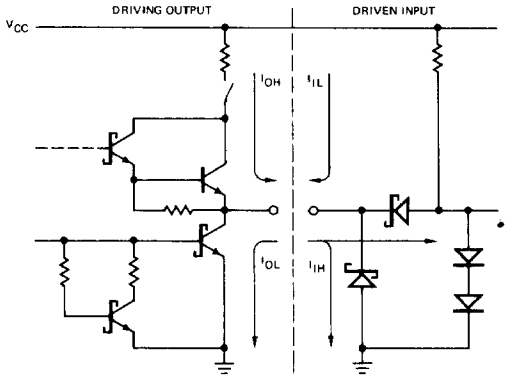
R The serial input to the Q_A flip-flop of the Am25LS194A in the right shift mode.

L The serial input to the Q_D flip-flop of the Am25LS194A in the left shift mode.

Q_A, Q_B, Q_C, Q_D The four true outputs of the register.

$\overline{Q}_D$ The complement output of the Q_D flip-flop. (Am25LS 195A only).

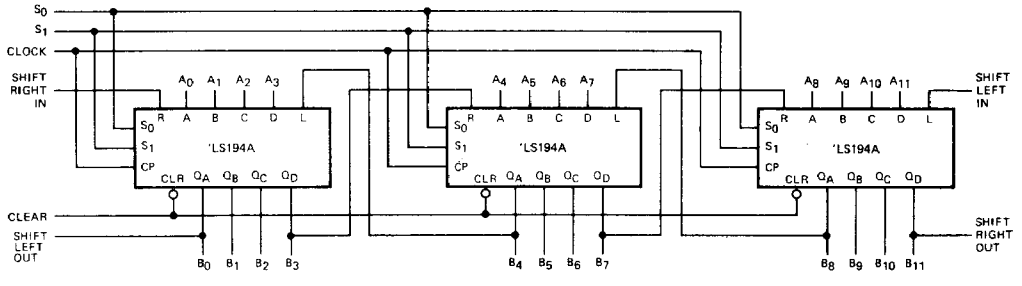
Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

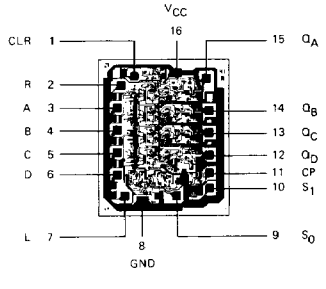
APPLICATION

12-BIT SHIFT-LEFT, SHIFT-RIGHT, PARALLEL LOAD REGISTER



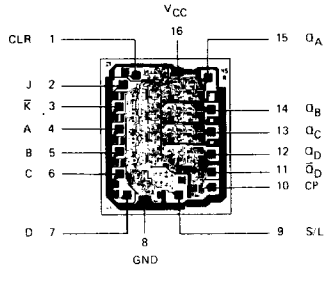
Metallization and Pad Layouts

'LS194A



DIE SIZE 0.067" X 0.080"

'LS195A



DIE SIZE 0.067" X 0.080"