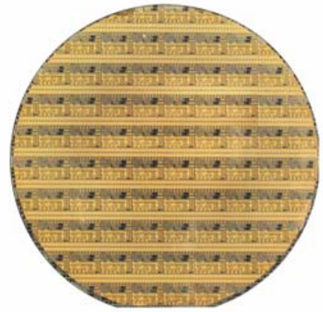
Think fast.

25673DV
DC to 25 GHz Divide-by-8 Prescaler (Die)
Data Sheet



Applications

- Phase-locked loop (PLL) applications from DC to 25 GHz
- Point-to-point and point-to-multipoint digital radios
- Broadband test and measurement equipment

Features

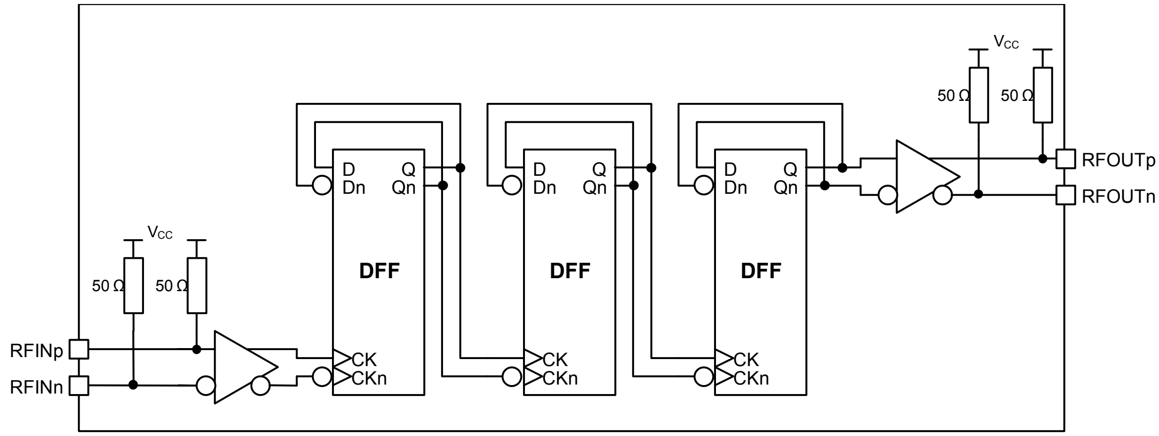
- Wide frequency range: DC to 25 GHz
- High input power sensitivity: –20 dBm typical
- Supports single-ended and differential operation
- Single +3.0 to +3.4 V power supply
- Low supply current: 64 mA typical
- Available in die form
- Also available in QFN plastic package or LGA ceramic package
- Evaluation board available

Description

The 25673DV divide-by-8 prescaler is designed for a wide range of communications and broadband test and measurement applications from DC to 25 GHz. It is typically used in high-frequency phase-locked loop (PLL) oscillator and signal-path down conversion circuits.

The 25673DV operates from a single +3.0 to +3.4 V power supply and is available in die form. This part is also available in 3 x 3 mm quad flat no lead (QFN) plastic package, or in a 7 x 7 mm land grid array (LGA) ceramic package. Please contact Inphi to obtain data sheets for these versions. The packaged parts are also available on an evaluation board.

Block Diagram



Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply Voltage	V_{CC}		–0.5	+3.6	V
CW RF Input Power	P_{IN} (CW)		---	+5	dBm
DC Input Voltage	V_{RFIN}		V_{CC}-2	V_{CC}+0.6	V
DC Output Voltage	V_{RFOUT}		V_{CC}-1.5	V_{CC}+1.0	V
Junction Temperature - Die	T_J		–40	+175	°C
Case Temperature	T_C		–55	+125	°C
Shipping/Storage Temperature	T_{STORE}		–65	+125	°C
Humidity	RH		0	100	%

Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}		+3.0	+3.3	+3.4	V
Supply Current	I_{CC}		52	64	75	mA
Operating Temperature (Junction)	T_J		–20	---	+125	°C
Operating Temperature (Case)	T_C		–40	---	+85	°C
Thermal Resistance	R_{JC}		---	---	54	°C/W

Electrical Specifications

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions.						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Max Input Frequency	F_{IN} (max)		25	26	---	GHz
Min Input Frequency[1]	F_{IN} (min)		---	0.5	1.0	GHz
Input Return Loss	RL_{IN}	< 25 GHz, $V_{CMIN} \leq V_{CC}$	10	---	---	dB
		< 25 GHz, $V_{CMIN} > V_{CC}$	6	---	---	dB
Input Power Range[2]	P_{IN}	1 – 4 GHz (sine wave) Single ended, AC coupled	–4	> –10	4	dBm
		4 – 8 GHz (sine wave) Single ended, AC coupled	–10	> –20	4	dBm
		8 – 20 GHz (sine wave) Single ended, AC coupled	–16	> –25	4	dBm
		20 – 24 GHz (sine wave) Single ended, AC coupled	–8	> –15	4	dBm
Output Return Loss	RL_{OUT}	< 13 GHz	10	---	---	dB
Output Power	P_{OUT}	Single ended, AC coupled, F_{IN} = 24 GHz	–3	0	---	dBm
Reverse Leakage (output power appearing at input ports)	$P_{LEAKAGE}$	Both RF outputs terminated (For F_{IN} = 12.5 to 25 GHz)	---	–65	---	dBm
		One RF output terminated	---	–35	---	dBm
Harmonics	$2F_{OUT}$	P_{IN} = 0 dBm, F_{IN} = 24 GHz	---	–32	---	dBc
	$3F_{OUT}$	P_{IN} = 0 dBm, F_{IN} = 24 GHz	---	–11	---	dBc
Jitter rms		F_{IN} = 24 GHz	---	1.3	---	ps
Output Rise/Fall Time	t_r/t_f	20% – 80%, F_{IN} = 24 GHz	---	30	---	ps
SSB Phase Noise @ 100 kHz offset	Φ	F_{IN} = 25 GHz	---	-148	---	dBc/Hz
Spurious Output Power[3]		All Input Frequencies	---	---	none	dBc

Notes:

[1] For sine wave input signal. Prescaler will operate down to DC with a square wave signal.

[2] For digital square wave inputs, the minimum input amplitude should be 300 mVpp (differential or single-ended) over the frequency range of DC to 25 GHz. Note: The minimum slew rate needs to be 1 V/ns.

[3] The Spurious Output Power measured was too low to be statistically significant.

Typical Operating Characteristics

*** This data was taken on 25673DV-QFN. ***

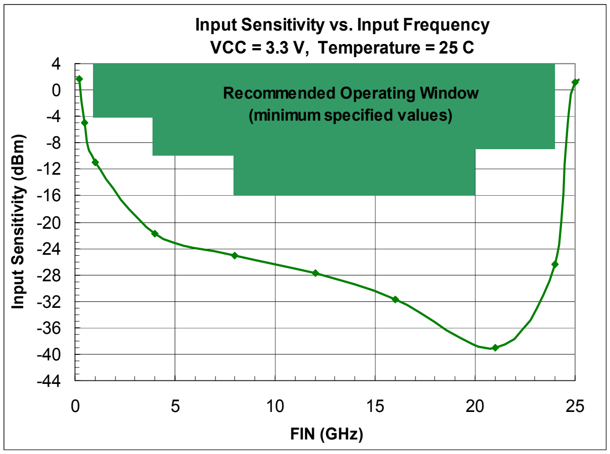


Figure 1. Input sensitivity over input frequency for Vcc = 3.3V at an ambient temperature of 25 C

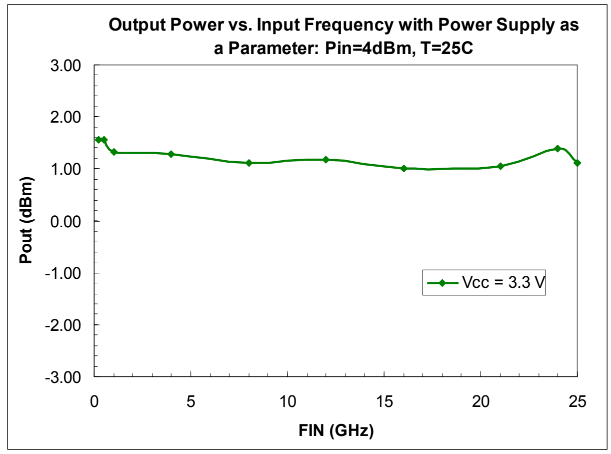


Figure 2. Output power (single-ended) versus input frequency for Vcc = 3.3V and Pin = 4 dBm at 25 C

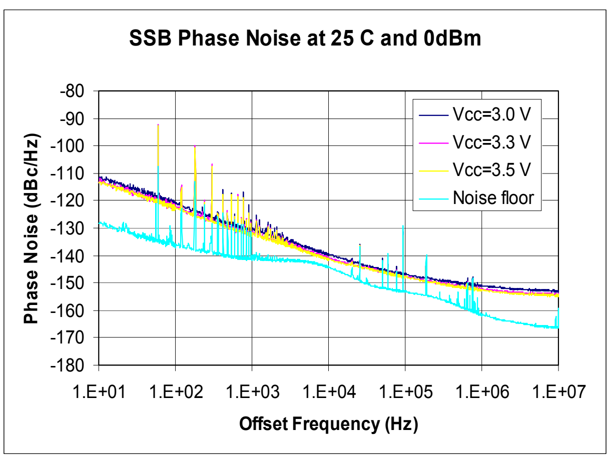


Figure 3. SSB phase noise for Fin = 25 GHz and Pin = 0 dBm at 25 C over supply voltage

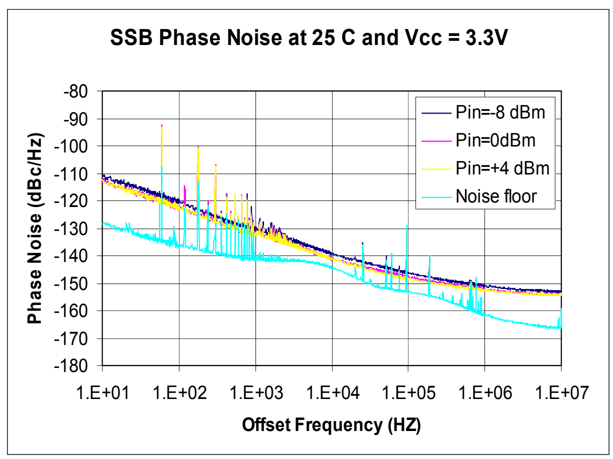


Figure 4. SSB phase noise for Fin = 25 GHz and Vcc = 3.3V at 25 C over input power

Typical Operating Characteristics (cont'd.)

<u>* This data was taken on 25673DV-QFN. *</u>

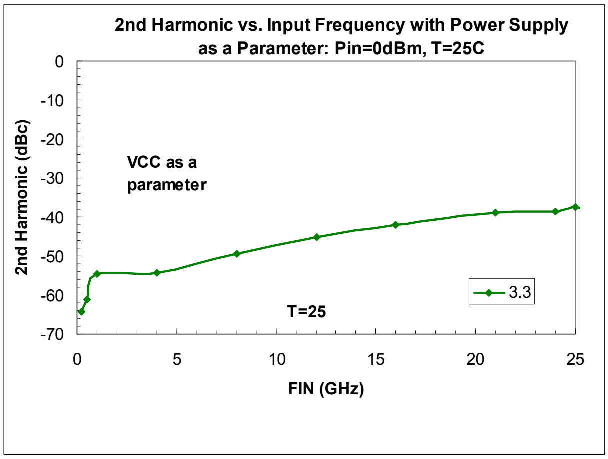


Figure 5. Second harmonic power versus input frequency at Vcc = 3.3V, Pin = 0 dBm at 25 C

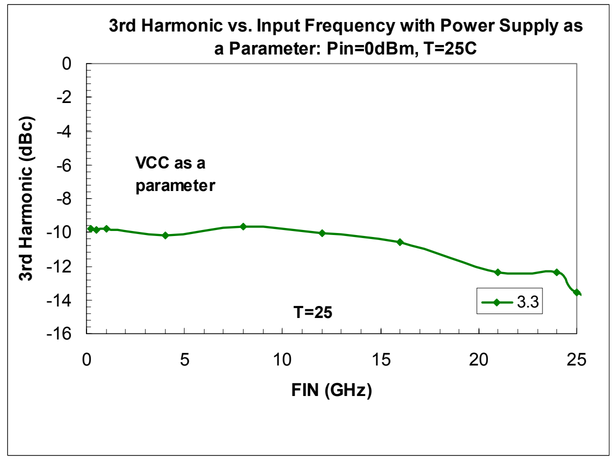


Figure 6. Third harmonic power versus input frequency at Vcc = 3.3V, Pin = 0 dBm at 25 C

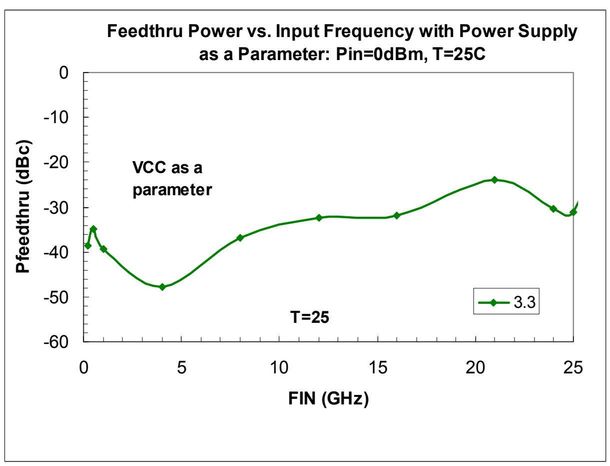


Figure 7. Feedthru power vs. Input Frequency at Vcc = 3.3 V, Pin = 0 dBm at 25 °C

Typical Time Domain Operating Characteristics

<u>* This data was taken on 25673DV-QFN. *</u>

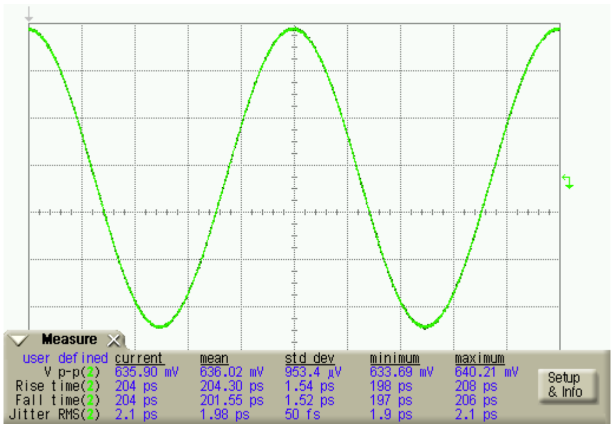


Figure 8. Input waveform, AC-coupled, for F_{IN} = 1 GHz and P_{IN} = 0 dBm; 200 ps/div, 100mV/div, T=25° C

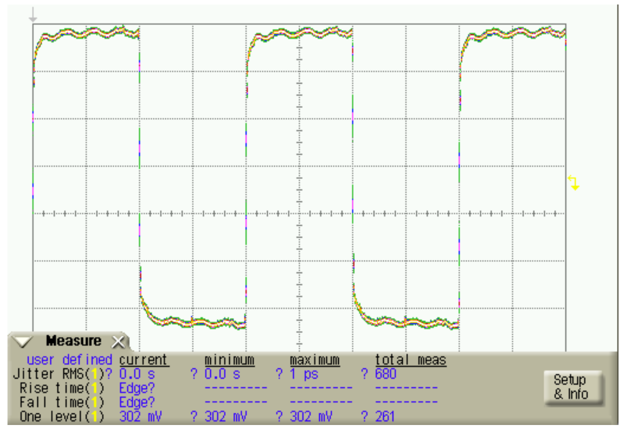


Figure 9. Output waveform, AC-coupled, for F_{IN} = 1 GHz and P_{IN} = 0 dBm; 2 ns/div, 100 mV/div, T=25° C; and Vcc=3.3 V

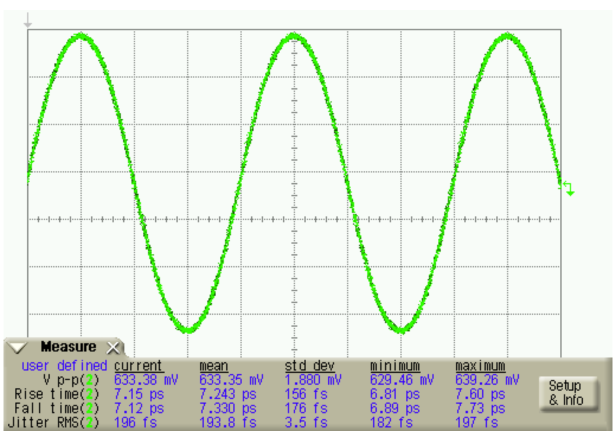


Figure 10. Input waveform, AC-coupled, for F_{IN} = 25 GHz and P_{IN} = 0 dBm; 10 ps/div, 100mV/div, T=25° C

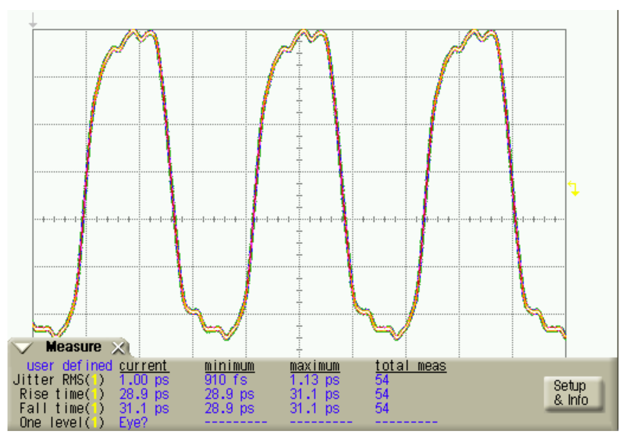


Figure 11. Output waveform, AC-coupled, for F_{IN} = 25 GHz and P_{IN} = 0 dBm; 100 ps/div, 100mV/div, T = 25° C; Vcc = 3.3 V

Application Notes

AC/DC Coupling and Termination
In a typical application, the RF inputs and outputs should be AC coupled via DC blocking capacitors mounted on a substrate or circuit board at each RF port. All unused RF outputs should be terminated with DC blocking capacitors and 50 Ω resistors to V_{CC} or ground for optimum performance. Unused output ports may be left open, but this configuration will result in additional power leakage from one RF port to the other.

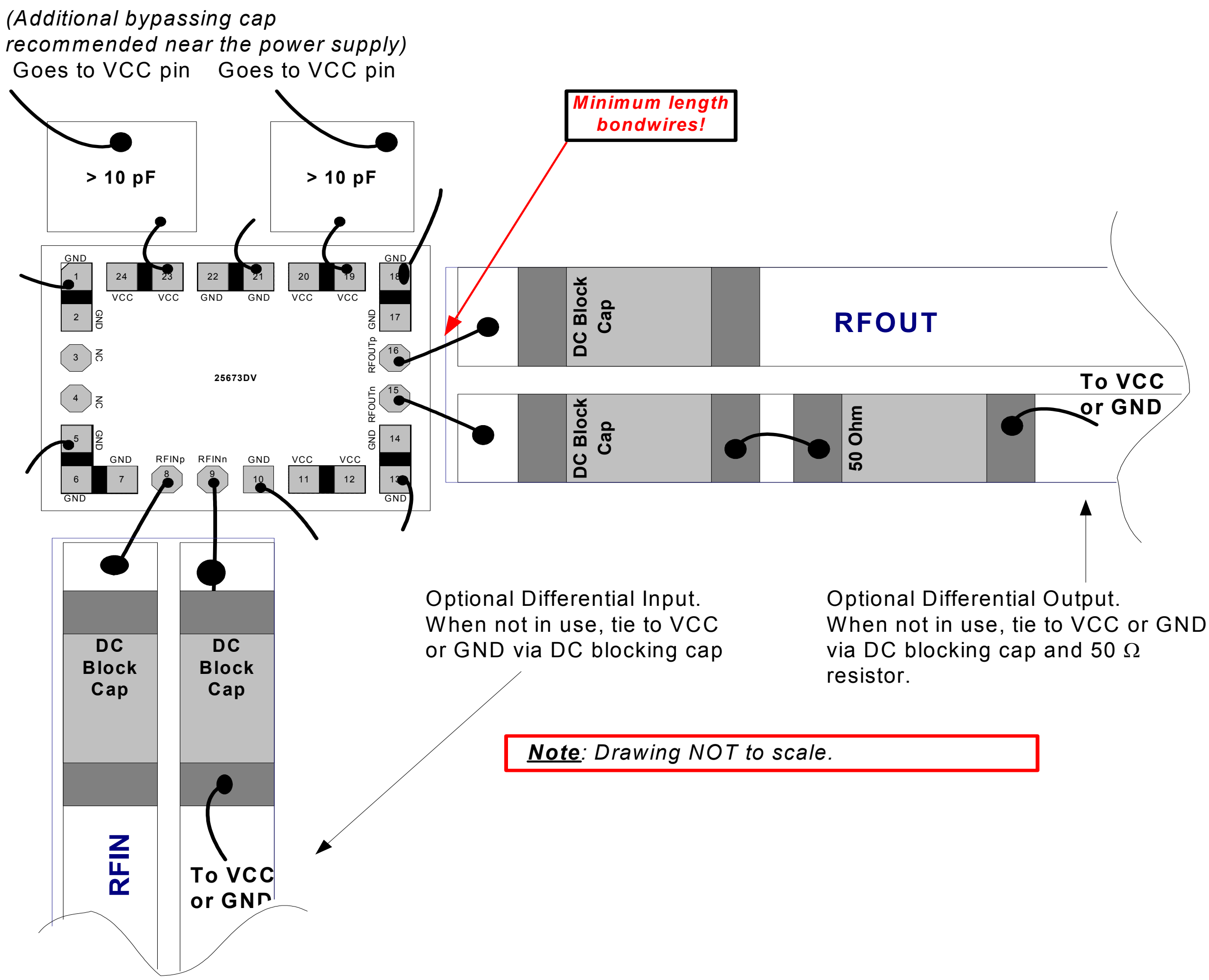
All unused RF inputs should be terminated with DC blocking capacitors and 50 Ω resistors to Vcc or ground for optimum performance. Unused RF input ports may be left open, but this configuration will result in additional power leakage from one RF port to the other. The improvement from adding the 50 Ω terminations is small, and may not be noticeable in all cases. It may be possible to omit the termination if the part meets all the customer requirements without it.

In applications where the use of DC blocking capacitors is not desirable, the part may be directly DC coupled at the RF inputs and outputs. However, care must be taken to ascertain that the DC voltages at all RF input and output ports stay within the specified limits (see Absolute Maximum Ratings on p. 2). All unused RF inputs and outputs should be terminated with 50 Ω resistors to V_{CC} (not ground) for optimum performance. Damage to the part may occur if the unused RF inputs and outputs are terminated directly to ground without the use of the DC blocking capacitors.

Single-Ended Operation
The 25673DV is designed for either single-ended or differential operation. For single-ended operation, the unused RF input and output should be terminated in the manner described above.

Input DC Offset
The 25673DV, under certain conditions, may self oscillate under no RF input power. This self-oscillation will produce an undesired output signal commonly referred to as "false trigger." To prevent false trigger, a small DC offset voltage between 20 mV and 100 mV may be applied between the RF input ports. Since the input has an internal 50 Ω resistor to V_{CC} (nominally +3.3 V), adding a 10 kΩ resistor between the unused RF input and ground will result in an offset voltage of approximately 16.5 mV between the RF inputs and prevent the false trigger.

Die Assembly Diagram



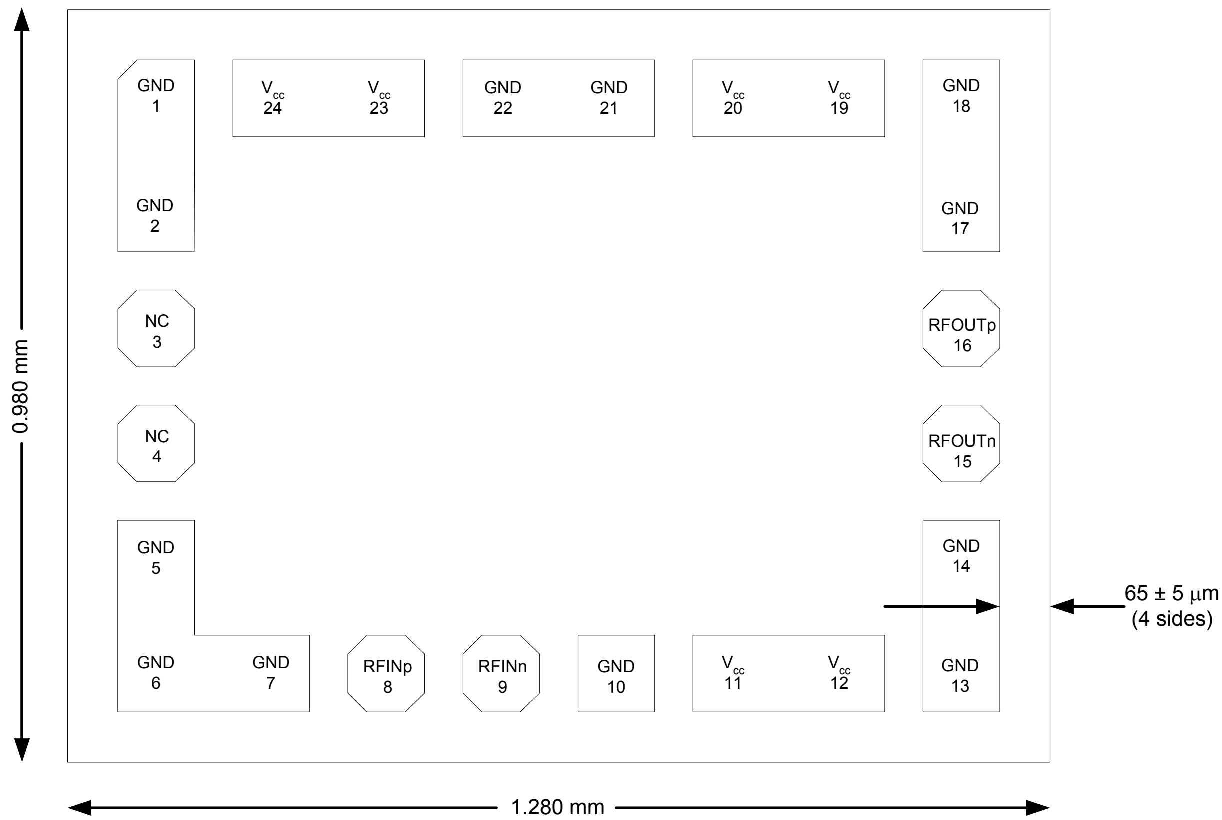
Chip Bonding Recommendation

We recommend the use of silver epoxy to bond the die to a chip carrier or substrate. Carefully control the amount of epoxy dispensed to avoid having the epoxy run over the top surface of the die.

Wire Bonding Recommendation

We recommend the use of 0.7-mil Au wire (99.99%). For optimum bond adhesion, the first bond should be made to the die and the second bond should be finished at the chip carrier or substrate.

Die Pad Layout



Notes:
[1]100 µm pads on 150 µm pitch.
[2]150 ± 10 µm die thickness.

Name	Pad	Description	Function
RFINp	8	RF Input positive (non-inverting)	Input
RFINn	9	RF Input negative (inverting)	Input
RFOUTp	16	RF Output positive (non-inverting)	Output
RFOUTn	15	RF Output negative (inverting)	Output
GND	1, 2, 5, 6, 7, 10, 13, 14, 17, 18, 21, 22	Ground	Supply
V_{CC}	11, 12, 19, 20, 23, 24	Power Supply: Connect to +3V to +3.4V Supply	Supply
NC	3, 4	Not Connected	NC

NOTE: DC blocking capacitors are required at RF input and RF output ports for AC coupling.

Die Pad Locations

For dimensioning purposes, reference origin (0,0) is the lower left corner of the lower left pad.

Pad #	Signal	Pad Lower Left Corner	
		X	Y
1	GND	0	750
2	GND	0	600
3	NC	0	450
4	NC	0	300
5	GND	0	150
6	GND	0	0
7	GND	150	0
8	RFINp	300	0
9	RFINn	450	0
10	GND	600	0
11	V_{CC}	750	0
12	V_{CC}	900	0
13	GND	1050	0
14	GND	1050	150
15	RFOUTn	1050	300
16	RFOUTp	1050	450
17	GND	1050	600
18	GND	1050	750
19	V_{CC}	900	750
20	V_{CC}	750	750
21	GND	600	750
22	GND	450	750
23	V_{CC}	300	750
24	V_{CC}	150	750

Order Information

Part No.	Description
25673DV-S03D	DC to 25 GHz Divide-by-8 Prescaler – Die

Related Products

Part No.	Description
25673DV-S03QFN	DC to 25 GHz Divide-by-8 Prescaler in Quad Flat No Lead Plastic Package
25673DV-S03L	DC to 25 GHz Divide-by-8 Prescaler in LGA Ceramic Package
25673DV-S03QFNEVB	DC to 25 GHz Divide-by-8 Prescaler in Quad Flat No Lead Plastic Package on an Evaluation Board with SMA Connectors
25673DV-S03LEVB	DC to 25 GHz Divide-by-8 Prescaler in LGA Ceramic Package on an Evaluation Board with SMA Connectors

Contact Information

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Qualification Notification

The 25673DV is fully qualified. Please contact Inphi for the qualification report.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Version Updates

From Version 1.4 to 2.0 (dated 2007-05-31)

1. Added disclaimers to Absolute Maximum Ratings table and removed "typical" column (page 2).
2. Updated Electrical Specifications Table (page 3):
    a. Added Input Return Loss parameter
        i. Symbol = RL_{IN}
        ii. 1st condition
            1. "< 25 GHz, $V_{CMIN} \leq V_{CC}$"
            2. Min = 10 dB
        iii. 2nd condition
            1. "< 25 GHz, $V_{CMIN} > V_{CC}$"
            2. Min = 6 dB
    b. Added Output Return Loss parameter
        i. Symbol = RL_{OUT}
        ii. Condition = < 13 GHz
        iii. Min = 10 dB
    c. For Reverse Leakage condition, added note: "(for F_{IN} = 12.5 to 25 GHz)" when both RF outputs are terminated.
    d. Removed Feedthru Power parameter
    e. Updated SSB Phase Noise
        i. Removed both conditions of F_{IN} = 12 GHz and 18 GHz
        ii. Added condition of F_{IN} = 25 GHz
        iii. Typ = -148 dBc/Hz
    f. Added Spurious Output Power
        i. Condition = All input frequencies
        ii. Max = none
        iii. Added footnote for this parameter.
    g. Added footnote for Input Power Range (P_{IN}), the minimum input amplitude and slew rate needed for digital square wave inputs.
3. Updated Typical Operating Characteristics (page 4 - 5):
    a. Added note "This data was taken on 25673DV-QFN".
    b. Replaced Figures 1 – 6.
    c. Added Figure 7, Feedthru Power plot
4. Updated Typical Time Domain Operating Characteristics (page 6):
    a. Added note "This data was taken on 25673DV-QFN".
    b. Added Figures 8 – 11.
5. Updated Application Notes to add information about optional 50 Ω resistors (page 7).
6. Separated positive and negative signal names in Die Pad Layout table (page 9).
7. Updated product part from S02 to S03 in Order Information and Related Products tables (page 11).
8. Updated Qualification Notification status to indicate that this product is fully qualified (page 11).