400 Mb/s/pin SLDRAM

4M x 18 SLDRAM

PIPELINED, EIGHT BANK, 2.5V OPERATION

FEATURES

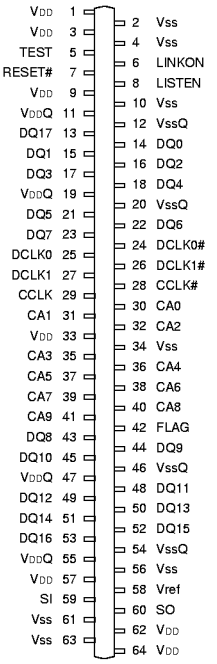
- Very High Speed - 400 MHz data rate
- 800 MB/s peak I/O Bandwidth - provides very high bandwidth over narrow system memory bus
- Pipelined (Concurrent) Operation - Up to 8 transactions (in one bank, or spread across multiple banks)
- Eight (this data sheet) or more internal banks for hiding row access/precharge
- Programmable burst lengths of 4 or 8
- 100% peak bandwidth sustainable over random row as well as random column accesses, even with 8 byte bursts.
- Packet Oriented Protocol - Provides pin compatibility across multiple densities
- Auto Refresh and Self Refresh
- Command Clock for commands and addresses; Bidirectional Data Clocks for read and write data
- Dual Data Clocks provide smooth handoff from one data source to another
- Programmable Offset between Data and Data Clocks
- Programmable Read Delays - Adjustable in coarse increments equal to one data bit time, and fine increments which are a fraction of a bit time; allows for specific temporal placement of data at the memory controller data pins
- Programmable Write Delays - Adjustable in coarse increments equal to one data bit time. Allows for optimally adjusted write data temporal placement by the memory controller
- Supports bank accesses (bank initially idle) and page accesses (bank active, row open)
- 64ms, 8192-cycle refresh
- SLIO Interface Technology -
  Drivers : calibrated VOH and VOL levels,
  Receivers : narrow set-up and hold windows
- Single +2.5V ± 5% power supply

OPTIONS — MARKING

- Timing
  400 MHz data rate — -400
- Plastic Package
  64-pin VSMP (400mil width, .4/.8mm pitch) — VS
- Part Number Example: SLD4M18DR400VS-400

PIN ASSIGNMENT (TOP VIEW)

64-Pin VSMP



GENERAL DESCRIPTION

The SLD4M18DR400 SLDRAM is a synchronous, very high-speed, packet-oriented, pipelined dynamic random access memory containing 75,497,472 bits. The SLD4M18DR400 SLDRAM is internally configured as eight banks of 128K x 72; each of the 128K x 72 banks is organized as 1024 rows by 128 columns by 72 bits. The 72 bits per column access are transferred over the I/O interface in a burst of four 18-bit words.

All transactions begin with a request packet. Read and write request packets contain the specific command and address information required. Read and write data are transferred in packets; a single-column access involves the transfer of a single data packet, which is a burst of four 18-bit words. Data from either one or two columns in a page may be accessed with a single request packet; the latter results in a continuous burst of eight 18-bit data words.

GENERAL DESCRIPTION (continued)

Read or write requests may be issued to idle banks, or to the open row in active banks. Read or write requests indicate whether to leave the row open after the access, or to perform a self-timed precharge at the completion of the access (auto-precharge).

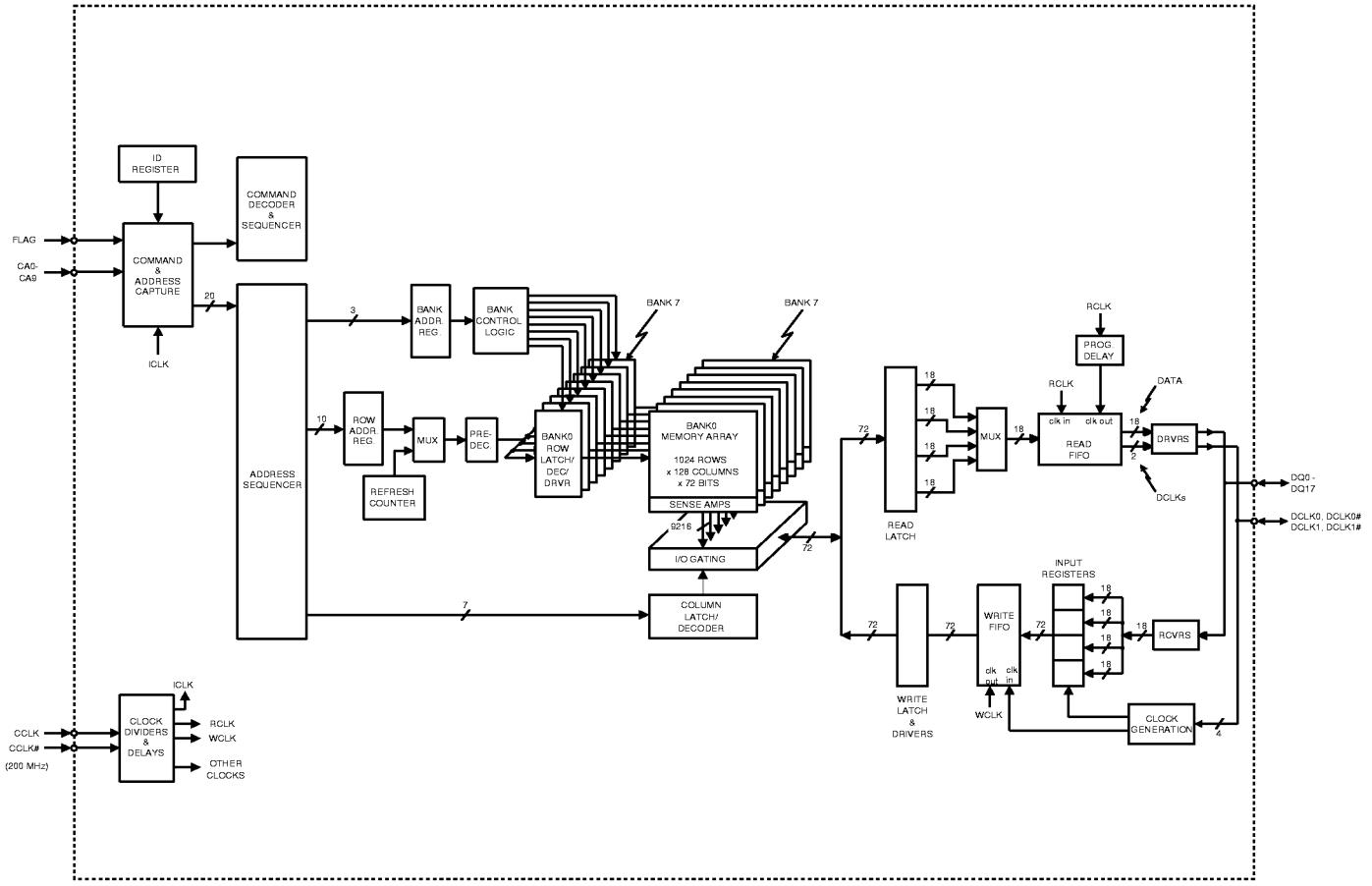
The SLD4M18DR400 uses a pipelined architecture and multiple internal banks to achieve high-speed operation and high effective bandwidth. Precharging one bank while accessing another bank will hide the precharge cycles, and provide seamless high-speed random access operation.

The SLD4M18DR400 is designed to operate in 2.5V memory systems. An auto-refresh mode is provided along with two power saving modes, standby and shutdown. Self-refresh is provided in the shutdown mode. The SLD4M18DR400 includes SLIO interface technology.

SLDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a very high data rate with automatic column-address generation, the ability to interleave between several internal banks in order to hide precharge time, and the capability to provide a continuous burst of data across random row and/or column locations, even with 8-byte granularity.

Terminology - the term "tick" is used throughout this data sheet as the equivalent of one-half of the CCLK clock period. Also, for simplicity, the clocks will be referred to and shown as CCLK, DCLK0 and DCLK1. It should be understood that these are differential clocks and that each has a complementary signal. Any reference to a specific edge of a particular clock refers to the true version of that clock (e.g. CCLK) not the complement (e.g. CCLK#).

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

VSMP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
29, 28	CCLK, CCLK#	SLIO Input	Command Clock (differential): CCLK is driven by the memory controller (or a separate clock chip) coincident with the leading edges of the command bits. SLDRAM command input signals are effectively sampled at each crossing of internally delayed versions of CCLK/CCLK#. Read clocks, write clocks, and other internal clocks are derived from CCLK.
25, 24, 27, 26	DCLK0, DCLK0#, DCLK1, DCLK1#	SLIO Input/ Output	Data Clocks (differential): For a read access, the specified pair of DCLK0/ DCLK0# or DCLK1/DCLK1# is driven by the SLDRAM, and for write accesses, the specified pair is driven by the memory controller. During read accesses, the SLDRAM provides 2 crossings on the selected DCLK pair prior to, and then 1 crossing coincident with, the beginning of each valid data word. During write accesses, the SLDRAM uses a delayed version of the DCLK pair received with the data to capture the data.
59, 60	SI, SO	LVCMOS Input, Output	Select In, Select Out: The controller and all SLDRAMs on a channel are connected in series using these pins. This connection is used to initialize the SLDRAMs.
6	LINKON	LVCMOS Input	Link On: Used to enter and exit Shutdown mode.
7	RESET#	LVCMOS Input	Reset#: Provides a hardware reset; resets all logic, including the ID register. Memory contents are not affected. An SLDRAM must be initialized following a hardware reset.
8	LISTEN	LVCMOS Input	Listen: Used to enter and exit Standby mode.
42	FLAG	SLIO Input	Flag: FLAG HIGH indicates the start of a valid request packet; FLAG then goes LOW for the remainder of the packet. FLAG LOW at any other time is interpreted as a NOP.
30-32, 35-41	CA0-CA9	SLIO Input	Command, Address: Commands, Addresses and/or Register Write Data are transferred on these signals, in packets of four words.
14-18, 21-23, 43-45, 48-53, 13	DQ0-DQ17	SLIO Input/ Output	Data I/O: Data bus.
5	TEST	—	Test Pin: Should be tied to V_{SS} during normal operation.
58	V_{REF}	—	Reference voltage.
11, 19, 47, 55	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
12, 20, 46, 54	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 3, 9, 33, 57, 62, 64	V_{DD}	Supply	Power Supply: +2.5V ± 5%.
2, 4, 10, 34, 56, 61, 63	V_{SS}	Supply	Ground.

FUNCTIONAL DESCRIPTION

The specific SLDRAM described in this data sheet is an octal 128K x 72 DRAM which operates at 2.5V and includes a high speed, packet-oriented, synchronous 18-bit interface, and a pipelined architecture. Each of the 128K x 72 bit banks is organized as 1024 rows by 128 columns by 72 bits.

Read and write accesses begin with the application of a request packet which includes all necessary address bits. The request packet is followed, after a specific programmed delay, by a data packet, to complete the transaction.

Prior to normal operation, the SLDRAM must be initialized. The following sections provide detailed information covering device initialization, packet definition, command descriptions, register definition, and device operation.

Initialization

POWER-UP/HARDWARE RESET

SLDRAMs must be powered-up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to V_{DD} and $V_{DD}Q$, then after a delay of tVTD, power must be applied to system V_{TERM}. V_{TERM} must be applied after $V_{DD}Q$ to avoid device latch-up, which may cause permanent damage to the device. V_{REF} can be applied any time after $V_{DD}Q$, but is expected to be nominally coincident with V_{TERM}. Inputs are not recognized as valid until after V_{REF} is applied. Upon power-up, the SLDRAM DQ and DCLK outputs will be High-Z and SO output will be driven LOW. The RESET# input should be held active for at least tRST. This hardware reset sets the internal ID Register to a value of 255, the SUB-ID Register to a value of 15, and sets programmable read and write delays to the minimum values.

EXIT SHUTDOWN/CONTROLLER DRIVER ADJUST

A LOW level on LINKON, and a stable CCLK, must be applied prior to deasserting RESET#; then after deasserting RESET#, continue the initialization sequence as if exiting the Shutdown mode (LISTEN LOW before LINKON HIGH, bring LINKON HIGH, wait tLHHC for DLLs to lock, then bring LISTEN HIGH). [Note: external buffer devices may require that LISTEN be LOW prior to deasserting RESET#, and that an additional lock delay must occur between LINKON going HIGH and LISTEN going HIGH]. After the exit Shutdown sequence, the device is active, and the command and write timing synchronization should be performed.

At some point prior to the start of command and write timing synchronization, the controller must perform a self-calibration of V_{OH} and V_{OL} on it's SLIO outputs and I/O pins.

COMMAND AND WRITE TIMING SYNCHRONIZATION

For command and write timing synchronization, the controller transmits the specified pattern on the FLAG, CA, DQ and DCLK signals, repetitively, until a LOW-to-HIGH transition is eventually detected on it's SI input (which occurs only after all devices on the channel are successfully synchronized). The controller brings it's SO output HIGH after transmitting the first cycle of the specified pattern. The packets are broadcast to all devices connected directly to the controller and are identified by a two-tick HIGH level on the FLAG input. During this operation, the SLDRAM devices use the SI/SO daisy-chain link to communicate to the controller that command and write timing synchronization has been completed. This is achieved by passing a LOW-to-HIGH transition from the controller SO output to the first SLDRAM SI input, and then from the first SLDRAM SO output to the second SLDRAM SI input, etc. through the last SLDRAM SO output driving SI input of the controller. Each SLDRAM device begins command and write timing synchronization upon detecting the specified pattern but does not drive it's SO output until both the transition at it's SI input, and the completion of command and write timing synchronization have occurred.

The receipt of the special pattern on FLAG prior to the LOW-to-HIGH transition on SI differentiates this activity on the SI/SO link from the similar procedure used during ID assignment. The controller stops sending the specified patterns after detecting SI HIGH, and then waits 16 ticks before sending a valid command or resetting the SI/SO link (the FLAG signal should be LOW for 16 ticks). This delay allows the SLDRAM devices to detect the absence of the special pattern on the FLAG input and to recognize the next HIGH level on the FLAG input as being the start of a valid command packet. The controller resets the SI/SO link by bringing it's SO LOW and waiting for it's SI to go LOW; HIGH-to-LOW transitions propagate through the link independent of device status or operation.

Although this data sheet describes a 400 Mb/s/p device, it is noted for future designs that faster devices up through 800 Mb/s/p will include the capability to synchronize at the 400 Mb/s/p rate.

ID ASSIGNMENT

Next, each SLDRAM on the channel(s) is sequentially assigned a unique ID and SUB-ID combination. Each SLDRAM is individually selected in turn by using the SI/SO link. This mode of operation is identified by a LOW-to-HIGH transition on SI followed by an ID Register Write Request Packet. Each ID Register Write Request will be followed by a corresponding SUB-ID Register Write Re-

quest Packet, and n of these request pairs will be issued, (where n equals the number of SLDRAM devices in the system). Only the SLDRAM which has SI HIGH, ID = 255 and SUB-ID = 15 will react to any given request pair. The selected SLDRAM reacts by writing the ID contained in the first packet to it's internal ID Register, writing the SUB-ID contained in the second packet to it's internal SUB-ID Register, and then driving it's SO HIGH. The controller provides enough delay (tID plus related maximum routing delays) between the assertion of it's SO output HIGH and the first issued request pair (and between subsequent issued request pairs) to allow for SO to propagate to the SI of the next device. ID assignment is complete when SI of the controller goes HIGH. Then the controller again resets the SI/SO link, as before.

PRE-CONFIGURATION/SLDRAM DRIVER ADJUST

At this point the SLDRAMs can receive commands, and each SLDRAM is uniquely addressable. Next, the SLDRAM operating frequency should be programmed, and then V_{OH} and V_{OL} calibration should be performed. The information indicating the appropriate operating frequency will either be contained in the controller itself, or can be obtained by the controller by polling some other component (jumpers, Serial Presence Detect device, etc.). The appropriate values are then written to the respective registers of each SLDRAM. For programmed operating frequencies other than 200 MHz (400 Mb/s/p) the command and write synchronization would be repeated at this point for the new frequency.

V_{OH} calibration is performed for each SLDRAM by sending a Drive DCLKs HIGH command and iteratively sending Increment/Decrement V_{OH} commands and observing the output level until the desired level is achieved. V_{OL} calibration is performed similarly using the Drive DCLKs LOW and Increment/Decrement V_{OL} commands. The controller should then issue a Disable DCLKs command packet.

READ TIMING SYNCHRONIZATION

At this point the controller can send commands to individual SLDRAMs, and the operating frequency is selected, so read timing synchronization can be performed.

For each SLDRAM, the controller should send a Read Sync Request packet. The specified data pattern is returned by the SLDRAM, with a delay equal to the Actual Page Read Delay (which, after reset, equals the Minimum Page Read Delay, measured in integer clock ticks at the maximum rated frequency of the device). The actual delay from each SLDRAM module will be different, and the specific delays are unknown to the controller at this point. The controller should enable the data synchronization circuitry immediately after sending a Read Sync Request command.

The controller should then adjust internal timing to capture data. This is accomplished by adjusting the Fine Read and Data Offset Verniers until the known data pattern is captured and the capture timing is optimized. At this point, the controller should issue a Stop Read Sync Packet, which instructs the SLDRAM to discontinue sending the sync pattern. After this is done for each SLDRAM, the controller can read data from each SLDRAM at the minimum latency for that particular device.

Command and Write Timing Synchronization, Write Timing Synchronization, Read Timing Synchronization or output level calibration may be repeated periodically if necessary for a given system design and environment. Such re-synchronizations or re-calibrations should be performed when no accesses are in progress.

DETECTING AND REPROGRAMMING READ AND WRITE LATENCIES

The controller may now detect the actual read latency in the system for each SLDRAM by sending a DRIVE DCLKs LOW command followed (after tDD) by a Read Status Register Request. The controller should enable data capture immediately after issuing the Read Status Register Request and should count clocks between sending the command and receiving the data. With the latency (including system delays) now known, the remaining status registers can be read as in normal operation (i.e. without first issuing the DRIVE DCLKs LOW command). Data from status registers is provided in a burst of 4 by the SLDRAM, at the Actual Read Latency of the device (which appears as the observed system latency at the controller).

After reading the status registers of all SLDRAMs, the controller uses the data provided, as well as the observed latencies, to determine the appropriate read latency to be programmed into the SLDRAMs.

In one suggested system design approach, the devices with shorter observed read latencies would be programmed with additional latency so as to match that of the SLDRAM(s) with the longest observed latency (for both bank and page accesses). This way, all read data arrives at the controller with the same latency from command to data, regardless of which SLDRAM device provides the data.

At this point the controller determines the optimum write latency corresponding to the above read latency at the controller I/O pins (optimizing the tradeoff of internal bus turnaround time and external bus turnaround time) and then must determine the corresponding write latency value for each SLDRAM (the write latency at a given SLDRAM may be different than that at the controller I/O pins, and may be different from that of other SLDRAMs). The controller must observe the system write latency for each SLDRAM compared to the corresponding programmed write latency for that device. This is accomplished by driving the DCLKs continually (toggling), issuing a Page Write to a specific address and sending a counting pattern on the DQs (start-

ing at the end of the write packet and continuing beyond the latency period, e.g. a count of 0-31 for 400 Mb/s/p). Reading back the value from the addressed location and comparing it with the value associated with the desired latency provides the delta to be used to reprogram the write latencies (for bank and page accesses) for a given SLDRAM.

Once the IDs have been assigned and the timing adjusted for each SLDRAM, the channel is ready for normal operation.

Figure 1
Command and Data Sync Patterns

SIGNAL	REPEATING PATTERN
Flag	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
CA9	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
CA8	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
CA7	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
CA6	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
CA5	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
CA4	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
CA3	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
CA2	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
CA1	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
CA0	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DQ17	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
DQ16	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DQ15	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
DQ14	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DQ13	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
DQ12	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DQ11	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
DQ10	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DQ9	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
DQ8	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DQ7	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
DQ6	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DQ5	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
DQ4	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DQ3	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
DQ2	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DQ1	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 ...
DQ0	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 ...
DCLK1	1 0 ...
DCLK0	1 0 ...

Packet Definition

General definitions for the various packets included in the protocol are shown in the following figures. More specific definitions are included, when necessary, in the Regsister Definition, Command Description and Device Operation sections of this data sheet.

READ, WRITE, OR ROW OP REQUEST PACKET

The Read, Write, or Row Op Request Packet is used to initiate any Read or Write Access, or to open or close a specific row in a specific bank.

A Read or Write request will result in the transfer of a Data Packet on the data bus at a specific time later. The Data Packet is driven by the SLDRAM for a READ, or by the memory controller for a Write. An Open Row or Close Row request generates no response.

Although unused address bits are not recognized by the SLDRAM device, zeroes should be applied for those bits, as shown.

REGISTER READ REQUEST PACKET

The Register Read Request Packet is used to initiate a Read access to a register address. In response to a Register Read Request Packet, the SLDRAM will provide a Data Packet on the data bus at a specific time later.

Although bits REG6-REG4, and the last 18 bits of the packet are not needed or recognized by the SLDRAM, zeroes should be applied for those bits, as shown.

Figure 2
READ, WRITE, OR ROW OP REQUEST PACKET DEFINITION

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	BNK2	BNK1	BNK0	ROW9	ROW8
0	ROW7	ROW6	ROW5	ROW4	ROW3	ROW2	ROW1	ROW0	0	0
0	0	0	0	COL6	COL5	COL4	COL3	COL2	COL1	COL0

ID8-ID0 = Device ID Value
CMD5-CMD0 = Command Code
BNK2-BNK0 = Bank Address

ROW9-ROW0 = Row Address
COL6-COL0 = Column Address
0 = Unused, apply 0 for this bit

Figure 3
REGISTER READ PACKET DEFINITION

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	REG6=0	REG5=0	REG4=0	REG3	REG2
0	REG1	REG0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0

ID8-ID0 = Device ID Value
CMD5-CMD0 = Command Code

REG6-REG0 = Register Address
0 = Unused, apply 0 for this bit

REGISTER WRITE REQUEST PACKET

The Register Write Request Packet is used to initiate a Write access to a register address. This packet consists of four words, with the latter two being the data to be written to the selected register.

Although bits REG6-REG4 are not needed or recognized by the SLDRAM, zeroes should be applied for those bits, as shown.

EVENT REQUEST PACKET

The Event Request Packet is used to initiate a hard or soft reset, an Autorefresh, or a Close All Rows command, or to enter or exit Self Refresh, adjust output voltage levels, adjust the Fine Read Vernier or adjust the Data Offset Vernier.

The output voltage levels, or the fine read or data offset verniers can be adjusted using a dedicated Adjust Settings Event Request Packet or as part of an Autorefresh Event. In either case, the bits ADJ0-ADJ4 and DO0-DO4 determine the specific adjustment to be made, according to Truth Table 3. An autorefresh without adjustment is performed when ADJ0-ADJ4 are all 0.

The default values shown should be applied to the unused bits. For events other than Autorefresh or Adjust Settings, the ADJ0-ADJ4 bits are unused and zeroes should be applied to these bits. Note: bits DO0-DO4 are defined for future use, the default value for these bits is, and will be, all ones.

Figure 4
REGISTER WRITE PACKET DEFINITION

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	SID4	SID3	SID2	SID1	SID0
0	REG6=0	REG5=0	REG4=0	REG3	REG2	REG1	REG0	0	0	0
0	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

ID8-ID0 = Device ID Value
SID4-0 = Device Sub-ID Value
RD9-RD0 = Register Data

CMD5-CMD0 = Command Code
REG6-REG0 = Register Address

Figure 5
EVENT PACKET DEFINITION

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	x	x	x	x	x	x	x	x	x	x
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	SID4	SID3	SID2	SID1	SID0
0	E6	E5	E4	E3	E2	E1	E0	0	0	0
0	ADJ4*	ADJ3*	ADJ2*	ADJ1*	ADJ0*	DO4*	DO3*	DO2*	DO1*	DO0*

* = For Autorefresh and Adjust Settings events only, otherwise unused (ADJx = 0, DOx=1)

ID8-ID0 = Device ID Value
SID4-0 = Device Sub-ID Value
ADJ4-0 = Adjust Setting Code

CMD5-CMD0 = Command Code
E6-E0 = Event Index Code
DO4-0 = Data Offset DQ Select (future use)

DATA PACKET

A Data Packet is provided by the controller for each Write Request, and by the SLDRAM for each Read Request. Each Data Packet contains either 8 bytes or 16 bytes, depending on whether the burst length was set to 4 or 8, respectively, in the corresponding request packet. There are no output disable or write masking capabilities within the data packet.

When the burst length of 8 is selected, the first 8 bytes in the packet correspond to the column address contained in the request packet, and the second 8 bytes correspond to the same column address except with an inverted LSB (i.e. the burst 'wraps').

Figure 6
DATA PACKET DEFINITION (FOR BURST LENGTH = 4)

DQ17 DQ16 DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9	DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
Byte 0	Byte 1
Byte 2	Byte 3
Byte 4	Byte 5
Byte 6	Byte 7

Figure 7
DATA PACKET DEFINITION (FOR BURST LENGTH = 8)

DQ17 DQ16 DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9	DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
Byte 0	Byte 1
Byte 2	Byte 3
Byte 4	Byte 5
Byte 6	Byte 7
Byte 8	Byte 9
Byte 10	Byte 11
Byte 12	Byte 13
Byte 14	Byte 15

Truth Table 1 - Commands

CMD5	CMD4	CMD3	Command	CMD2	CMD1	CMD0	Subcommand
0	0	0		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	0	0		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	0	0		0	1	0	Read Access, Close Row, Drive DCLK0
0	0	0	Page Access,	0	1	1	Read Access, Close Row, Drive DCLK1
0	0	0	Burst of 4	1	0	0	Write Access, Leave Row Open, Use DCLK0
0	0	0		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	0	0		1	1	0	Write Access, Close Row, Use DCLK0
0	0	0		1	1	1	Write Access, Close Row, Use DCLK1
0	0	1		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	0	1		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	0	1		0	1	0	Read Access, Close Row, Drive DCLK0
0	0	1	Page Access,	0	1	1	Read Access, Close Row, Drive DCLK1
0	0	1	Burst of 8	1	0	0	Write Access, Leave Row Open, Use DCLK0
0	0	1		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	0	1		1	1	0	Write Access, Close Row, Use DCLK0
0	0	1		1	1	1	Write Access, Close Row, Use DCLK1
0	1	0		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	1	0		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	1	0		0	1	0	Read Access, Close Row, Drive DCLK0
0	1	0	Bank Access,	0	1	1	Read Access, Close Row, Drive DCLK1
0	1	0	Burst of 4	1	0	0	Write Access, Leave Row Open, Use DCLK0
0	1	0		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	1	0		1	1	0	Write Access, Close Row, Use DCLK0
0	1	0		1	1	1	Write Access, Close Row, Use DCLK1
0	1	1		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	1	1		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	1	1		0	1	0	Read Access, Close Row, Drive DCLK0
0	1	1	Bank Access,	0	1	1	Read Access, Close Row, Drive DCLK1
0	1	1	Burst of 8	1	0	0	Write Access, Leave Row Open, Use DCLK0
0	1	1		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	1	1		1	1	0	Write Access, Close Row, Use DCLK0
0	1	1		1	1	1	Write Access, Close Row, Use DCLK1
1	0	0		0	0	0	Reserved
1	0	0		0	0	1	Open Row
1	0	0	Register	0	1	0	Close Row
1	0	0	Access,	0	1	1	Register Write
1	0	0	Row Op,	1	0	0	Register Read, Use DCLK0
1	0	0	or Event	1	0	1	Register Read, Use DCLK1
1	0	0		1	1	0	Reserved
1	0	0		1	1	1	Event
1	0	1		0	0	0	Read Sync (Drive both DCLKs)
1	0	1		0	0	1	Stop Read Sync
1	0	1		0	1	0	Drive DCLKs LOW
1	0	1	Data	0	1	1	Drive DCLKs HIGH
1	0	1	Sync	1	0	0	Write Sync (Both DCLKs toggling)
1	0	1		1	0	1	Reserved
1	0	1		1	1	0	Disable DCLKs
1	0	1		1	1	1	Drive DCLKs Toggling
1	1	0	Reserved	x	x	x	Reserved
1	1	1	Reserved	x	x	x	Reserved

*Index Range	Description
0 - 15	Defined Events - See Event Truth Table
16 - 63	Reserved
64 - 127	Vendor Dependent

* Index = value of E6-E0 in Event Request Packet

Figure 8
Event Index Codes

Truth Table 2 - Events

E6-E3	E2	E1	E0	Event
0	0	0	0	Set ID Register to 255, SUB-ID to 15, reset device
0	0	0	1	Reset device, except ID and SUB-ID Registers
0	0	1	0	Autorefresh
0	0	1	1	Close all rows
0	1	0	0	Enter Self Refresh
0	1	0	1	Exit Self Refresh
0	1	1	0	Adjust Settings
0	1	1	1	Reserved

Truth Table 3 - Adjust Settings

ADJ4	ADJ3	ADJ2	ADJ1	ADJ0	ADJUSTMENT
0	0	0	0	0	No Adjustment
0	0	0	0	1	Decrement Data Offset Vernier (delay DQs relative to DCLK0)
0	0	0	1	0	Increment Data Offset Vernier (advance DQs relative to DCLK0)
0	0	0	1	1	Reset Data Offset Vernier to Zero
0	0	1	0	0	Reserved
0	0	1	0	1	Decrement Fine Read Vernier for DQs and DCLK0
0	0	1	1	0	Increment Fine Read Vernier for DQs and DCLK0
0	0	1	1	1	Reset Fine Read Vernier for DQs and DCLK0 to Zero
0	1	0	0	0	Reserved
0	1	0	0	1	Decrement Fine Read Vernier for DCLK1
0	1	0	1	0	Increment Fine Read Vernier for DCLK1
0	1	0	1	1	Reset Fine Read Vernier for DCLK1 to Zero
0	1	1	0	0	Reserved
0	1	1	0	1	Decrement VOH Level
0	1	1	1	0	Increment VOH Level
0	1	1	1	1	Reset VOH to center of range
1	0	0	0	0	Reserved
1	0	0	0	1	Decrement VOL Level
1	0	0	1	0	Increment VOL Level
1	0	0	1	1	Reset VOL to center of range
1	0	1	0	0	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved
1	1	0	0	1	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

Command Descriptions

Truth Table 1 provides a quick reference of available commands. Detailed descriptions are provided in the following sections. All command packets must start on a positive edge of CCLK (with CCLK in this context being specific, not generic).

NO OPERATION (NOP)

FLAG HIGH indicates the start of a valid request packet; FLAG then goes LOW for the remainder of the packet. FLAG LOW at any other time results in a NO OPERATION (NOP). A NOP prevents unwanted commands from being registered during idle states. NOPs do not affect operations already in progress.

OPEN ROW

The OPEN ROW command is used to open (or activate) a row in a particular bank in preparation for a subsequent, but separate, column access command. The row remains open (or active) for accesses until a CLOSE ROW command or an access-and-close-row type command is issued to that bank. After an OPEN ROW command is issued to a given bank, a CLOSE ROW command or an access-and-close-row type command must be issued to that bank before a different row in that same bank can be opened.

The OPEN ROW command may be useful when a page access is anticipated, but the column address is not yet known, or when splitting a bank access into two components will facilitate scheduling.

CLOSE ROW

The CLOSE ROW command is used to close a row in a specific bank.

The CLOSE ROW command is used when it is desired to close a row that was previously left open in anticipation of subsequent page accesses.

READ

Page Read commands and Bank Read commands are used to initiate a read access to an open row, or to a closed row, respectively. The commands indicate the burst length, the selected DCLK, and whether to leave the row open after the access. Read data appears on the DQs subject to the corresponding Read Delay Register value and Read Data Vernier and Data Offset Vernier settings previously programmed into the device.

WRITE

Page Write commands and Bank Write commands are used to initiate a write access to an open row, or to a closed row, respectively. The commands indicate the burst length, the selected DCLK, and whether to leave the row open after the access. Write data is expected on the DQs at a time determined by the corresponding Write Delay Register value previously programmed into the device.

REGISTER READ

Used to read the contents of the device status registers. The register data is available on the DQs after the delay determined by the Page Read Delay Register value and the Read Data Vernier and Data Offset Vernier settings previously programmed into the device.

REGISTER WRITE

Used to write to the control registers of the device. The register data is included within the request packet containing the command.

EVENT

Used to issue commands not requiring a specific address within a device or devices.

Hard Reset - Sets ID register to 255, SUB-ID register to 15, and resets device

Soft Reset - Resets device, except ID and SUB-ID registers

Autorefresh - Performs a refresh operation to the row or group of rows addressed by the internal refresh counter. All banks must be idle prior to performing an autorefresh event. The same adjustments that are possible with an Adjust Settings event may also be performed during an Autorefresh event

Close All Rows - Closes any open rows in any banks.

Enter Self Refresh - Causes the device to enter the Self Refresh mode of operation.

Exit Self Refresh - Causes the device to exit the Self Refresh mode of operation.

Adjust Settings - Used to adjust the Data Offset Vernier, Fine Read Verniers, VOH levels, and VOL levels.

READ SYNC (STOP READ SYNC)

Instructs the SLDRAM to start (stop) transmitting the specified synchronization pattern to be used by the controller to adjust input capture timing.

WRITE SYNC

Instructs the SLDRAM to use the incoming data pattern to adjust input capture timing.

DRIVE DCLKs LOW (HIGH)

Instructs the SLDRAM to drive the DCLK outputs LOW (HIGH) until overridden by another DRIVE DCLK or READ command. DCLK is specific in this context; the DCLK# outputs will be in the opposite state.

DRIVE DCLKs TOGGLING

Instructs the SLDRAM to drive the DCLK outputs toggling at the operating frequency of the device (i.e. DCLKn and DCLKn# will cross every tCK/2 ns) until overridden by another DRIVE DCLK or READ command.

DISABLE DCLKs TOGGLING

Instructs the SLDRAM to disable (High-Z) the DCLK/DCLK# outputs until overridden by another DRIVE DCLK or READ command.

Register Definition

The SLDRAM includes two sets of registers, the control registers and the status registers. The control registers are write-only registers which are logically 20-bits wide. Physically, all control registers are currently 8-bits or less, so the remaining bits are 'don't care' to the SLDRAM. However, to allow for future revision, the controller should write a 0 to each 'don't care' bit. Data to be written to a control register is provided via the Command/Address bus as part of the Register Write Packet.

The status registers are read-only registers which are logically 72-bits wide. Physically, all status registers are currently 32-bits, so the remaining bits are driven LOW during status register reads. Data being read from a status register is provided in a burst of 4, after a delay equal to the Actual Page Read Delay previously programmed into the device.

REG3	REG2	REG1	REG0	CONTROL REGISTER	STATUS REGISTER
0	0	0	0	ID	Configuration
0	0	0	1	SUB-ID	Actual Delays
0	0	1	0	Operating Frequency	Minimum Delays
0	0	1	1	Test	Maximum Delays
0	1	0	0	Page Read Delay	Test
0	1	0	1	Page Write Delay	tRAS/tRP
0	1	1	0	Bank Read Delay	tRC1/tRC2
0	1	1	1	Bank Write Delay	tRCD/tXSR
1	0	0	0	Reserved	tWR/tWRD
1	0	0	1	Reserved	tPR/tBR
1	0	1	0	Reserved	tPW/tBW
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

Figure 9
REGISTER NAMES AND ADDRESSES

CONTROL REGISTERs

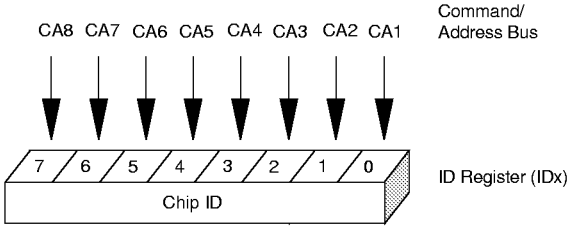
ID Register

The ID Register consists of eight bits which are all set to 1 (= ID value 255) upon hardware reset, and are subsequently programmed to a unique value during initialization. Each SLDRAM monitors the Command/Address Bus for the start of a request packet, and then performs a comparison between the ID contained in the request packet and the one contained in it's internal ID Register. If there is a match within a given SLDRAM, this device will process the request packet. The 9th ID bit in the request packet allows for an SLDRAM to be accessed either individually or as part of a group (multicast). Broadcast Request Packets are recognized by all SLDRAMs, regardless of ID Register value. For Register Write and Event Request Packets, the SUB-ID value must also be a match, a multicast, or a broadcast to select a given SLDRAM.

The ID Register is programmed using the Write ID Register Request packet shown below.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0
0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0

Figure 10
REGISTER WRITE REQUEST PACKET - ID REGISTER



Note: ID8 is not stored in the SLDRAM

Figure 11
ID REGISTER DEFINITION

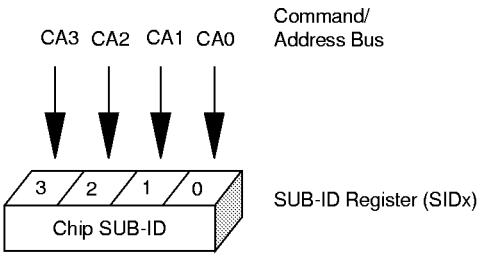
SUB-ID Register

The SUB-ID Register consists of four bits which are all set to 1 (= ID value 15) upon hardware reset, and are subsequently programmed to a unique value (for a given ID value) during initialization. For Register Write and Event Requests, SLDRAMs with an ID that matches that in the request packet will perform a comparison between the SUB-ID also contained in the request packet and the one contained in it's internal SUB-ID Register. If there is a match within a given SLDRAM, this device will process the request packet. The 5th SUB-ID bit in the request packet allows for an SLDRAM to be accessed either individually or as part of a group (multicast). Such request packets will be recognized by all SLDRAMs with a matching ID if the 5th SUB-ID bit is 1 (regardless of SUB-ID register value), and by all SLDRAMs (regardless of ID and SUB-ID) if both the 9th ID bit and the 5th SUB-ID bit are 1.

The SUB-ID Register is programmed using the Write SUB-ID Register Request packet shown below.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	SID3	SID2	SID1	SID0

Figure 12
REGISTER WRITE REQUEST PACKET - SUB-ID REGISTER



Note: SID4 is not stored in the SLDRAM

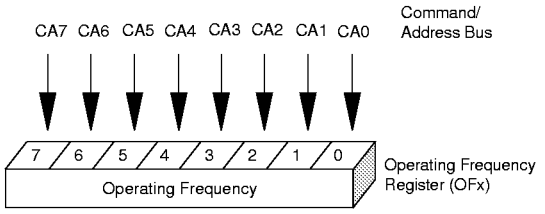
Figure 13
SUB-ID REGISTER DEFINITION

Operating Frequency Register

Future SLDRAM devices will be capable of operating at more than one distinct clock frequency (e.g. 200, 300 or 400 MHz clock frequencies, resulting in 400, 600 or 800 Mb/s per pin data rate, respectively). The desired frequency, of those available, is selected via the Operating Frequency Register, as shown below. This is shown for future planning; for the devices covered by this data sheet, the value written to this register must be 0000000010 (bits 9-0, respectively).

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	0	1	0	0	0	0
0	0	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

Figure 14
REGISTER WRITE REQUEST PACKET - OPERATING FREQUENCY REGISTER



Note: One, and only one, bit must be set to 1, and the corresponding operating frequency must be valid for a given device.

OFx: 7 6 5 4 3 2 1 0	Clock Frequency/ (data rate per pin)
0 0 0 0 0 0 0 1	100 MHz/(200 Mb/s/p)
0 0 0 0 0 0 1 0	200 MHz/(400 Mb/s/p)
0 0 0 0 0 1 0 0	300 MHz/(600 Mb/s/p)
0 0 0 0 1 0 0 0	400 MHz/(800 Mb/s/p)
0 0 0 1 0 0 0 0	500 MHz/(1 Gb/s/p)
0 0 1 0 0 0 0 0	600 MHz/(1.2 Gb/s/p)
All others	Reserved or Illegal

Figure 15
OPERATING FREQUENCY REGISTER/ BIT DEFINITION

Test Register

This register is for vendor specific device testing and should not be written to during normal device operation.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	0	1	1	0	0	0
T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

Figure 16
REGISTER WRITE REQUEST PACKET - TEST REGISTER

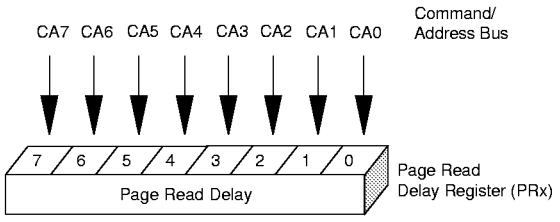
Page Read Delay Register

The Page Read Delay Register is used to program the number of integer clock ticks (a.k.a. half cycles, or bit times) between receiving a Page Read Request Packet and providing the corresponding Read Data output. Although the 8-bit register can support a range of 0 to 255 clock ticks, the value programmed must be between the minimum and maximum values as provided in the respective status registers. Different values may be programmed in different SLDRAMs on the same channel in order to compensate for differences in internal SLDRAM and external routing delays.

The value written to this register may subsequently be modified by Increment/Decrement Fine Read Vernier events. Such modifications are reflected in the Actual Delays Status Register.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	1	0	0	0	0	0
0	0	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0

Figure 17
REGISTER WRITE REQUEST PACKET - PAGE READ DELAY REGISTER



PRx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

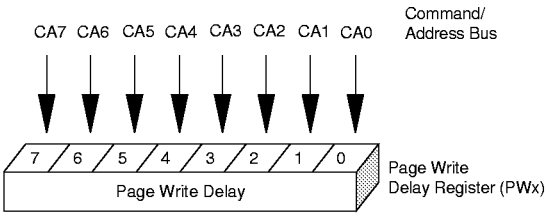
Figure 18
PAGE READ DELAY REGISTER/BIT DEFINITION

Page Write Delay Register

The Page Write Delay Register is used to program the number of integer clock ticks (a.k.a. half cycles, or bit times) between receiving a Page Write Request Packet and receiving the corresponding Write Data input. Although the 8-bit register can support a range of 0 to 255 clock ticks, the value programmed must be between the minimum and maximum values as provided in the respective status registers. It is expected, though not required, that the same value would be programmed in all SLDRAMs on a channel. The specific value, from the range of allowable values, can be chosen to achieve the optimum relationship between read latency and write latency.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	1	0	1	0	0	0
0	0	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0

Figure 19
REGISTER WRITE REQUEST PACKET - PAGE WRITE DELAY REGISTER



PWx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 20
PAGE WRITE DELAY REGISTER/BIT DEFINITION

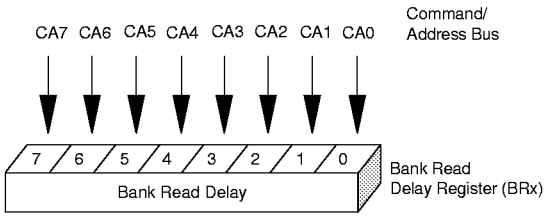
Bank Read Delay Register

The Bank Read Delay Register is used to program the number of integer clock ticks (a.k.a. half cycles, or bit times) between receiving a Bank Read Request Packet and providing the corresponding Read Data output. Although the 8-bit register can support a range of 0 to 255 clock ticks, the value programmed must be between the minimum and maximum values as provided in the respective status registers. Different values may be programmed in different SLDRAMs on the same channel in order to compensate for differences in internal SLDRAM and external routing delays.

The value written to this register may subsequently be modified by Increment/Decrement Fine Read Vernier events. Such modifications are reflected in the Actual Delays Status Register.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	1	1	0	0	0	0
0	0	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

Figure 21
REGISTER WRITE REQUEST PACKET - BANK READ DELAY REGISTER



BRx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

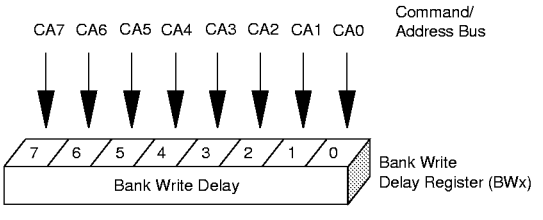
Figure 22
BANK READ DELAY REGISTER/BIT DEFINITION

Bank Write Delay Register

The Bank Write Delay Register is used to program the number of integer clock ticks (a.k.a. half cycles, or bit times) between receiving a Bank Write Request Packet and receiving the corresponding Write Data input. Although the 8-bit register can support a range of 0 to 255 clock ticks, the value programmed must be between the minimum and maximum values as provided in the respective status registers. It is expected, though not required, that the same value would be programmed in all SLDRAMs on a channel. The specific value, from the range of allowable values, can be chosen to achieve the optimum relationship between read latency and write latency.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	0	1	1	SID4	SID3	SID2	SID1	SID0
0	0	0	0	1	1	1	0	0	0
0	0	BW7	BW6	BW5	BW4	BW3	BW2	BW1	BW0

Figure 23
REGISTER WRITE REQUEST PACKET - BANK WRITE DELAY REGISTER



BWx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 24
BANK WRITE DELAY REGISTER/BIT DEFINITION

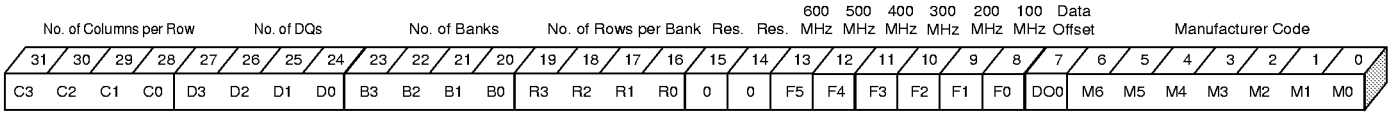


Figure 25
CONFIGURATION REGISTER

STATUS REGISTERs

Configuration Register

The Configuration Register contains a code which uniquely identifies the memory device vendor, the valid operating frequencies for the device, the number of banks in the device, the number of rows per bank, the number of columns per page and the number of DQs on the device.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Note: CMD0 is either 0 or 1, to select the appropriate DCLK

Figure 26
REGISTER READ REQUEST PACKET - CONFIGURATION REGISTER

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	DO0	M6	M5	M4	M3	M2	M1	M0
0	0	0	F5	F4	F3	F2	F1	F0
0	B3	B2	B1	B0	R3	R2	R1	R0
0	C3	C2	C1	C0	D3	D2	D1	D0

Figure 27
REGISTER READ DATA PACKET - CONFIGURATION REGISTER

Configuration Register - Data Offset Bit

The DO0 bit indicates whether the SLDRAM supports bit level data offset. If DO0 = 0, the device supports word-wide offset only. If DO0 = 1, the device supports both word-wide and bit level offset.

Configuration Register - Manufacturer Field

This field contains a code which uniquely identifies the memory device vendor.

Mx: 6 5 4 3 2 1 0	Manufacturer
0 0 0 0 0 0 0	Fujitsu
0 0 0 0 0 0 1	Hitachi
0 0 0 0 0 1 0	Hyundai
0 0 0 0 0 1 1	IBM
0 0 0 0 1 0 0	LG Semicon
0 0 0 0 1 0 1	Micron
0 0 0 0 1 1 0	Mitsubishi
0 0 0 0 1 1 1	Mosel Vitelic
0 0 0 1 0 0 0	Motorola
0 0 0 1 0 0 1	National/Panasonic
0 0 0 1 0 1 0	NEC
0 0 0 1 0 1 1	Nippon Steel
0 0 0 1 1 0 0	OKI
0 0 0 1 1 0 1	Samsung
0 0 0 1 1 1 0	Siemens
0 0 0 1 1 1 1	Texas Instruments
0 0 1 0 0 0 0	Toshiba
0 0 1 0 0 0 1	Vanguard
0 0 1 0 0 1 0	Reserved
:	:
1 1 1 1 1 1 1	Reserved

Figure 28
CONFIGURATION REGISTER -MANUFACTURER FIELD DEFINITION

Configuration Register - Frequency Field

This field indicates the valid operating frequencies for the device. Each defined bit corresponds to a specific operating frequency. At least one bit, and possibly more than one bit will be 1, indicating that the device supports that operating frequency. A 0 is provided on each reserved bit location as well as the bit locations for each operating frequency not supported. This is shown for future planning; for the devices covered by this data sheet, the value read from this field will be 000010 (bits F5-F0, respectively), indicating 200 MHz (or 400 Mb/s/p) operation.

F5	F4	F3	F2	F1	F0
600 MHz	500 MHz	400 MHz	300 MHz	200 MHz	100 MHz

Figure 29
CONFIGURATION REGISTER - FREQUENCY FIELD DEFINITION

Configuration Register - Bank Field

This field indicates the number of banks in the device.

B3	B2	B1	B0	No. of Banks
0	0	0	0	Reserved (1)
0	0	0	1	Reserved (2)
0	0	1	0	Reserved (4)
0	0	1	1	8
0	1	0	0	16
0	1	0	1	Reserved (32)
0	1	1	0	Reserved (64)
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Figure 30
CONFIGURATION REGISTER - BANK FIELD DEFINITION

Configuration Register - Row Field

This field indicates the number of rows per bank.

R3	R2	R1	R0	No. of Rows per Bank
0	0	0	0	Reserved
0	0	0	1	Reserved (512)
0	0	1	0	1K
0	0	1	1	2K
0	1	0	0	4K
0	1	0	1	Reserved (8K)
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Figure 31
CONFIGURATION REGISTER - ROW FIELD DEFINITION

Configuration Register - Column Field

This field indicates the number of columns per row.

C3	C2	C1	C0	No. of Columns per Row
0	0	0	0	Reserved
0	0	0	1	16
0	0	1	0	32
0	0	1	1	64
0	1	0	0	128
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Figure 32
CONFIGURATION REGISTER - COLUMN FIELD DEFINITION

Configuration Register - DQ Field

This field indicates the number of DQs per device.

D3	D2	D1	D0	No. of DQs
0	0	0	0	Reserved (4)
0	0	0	1	8
0	0	1	0	Reserved (9)
0	0	1	1	16
0	1	0	0	18
0	1	0	1	32
0	1	1	0	Reserved (36)
0	1	1	1	64
1	0	0	0	Reserved (72)
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Figure 33
CONFIGURATION REGISTER - DQ FIELD DEFINITION

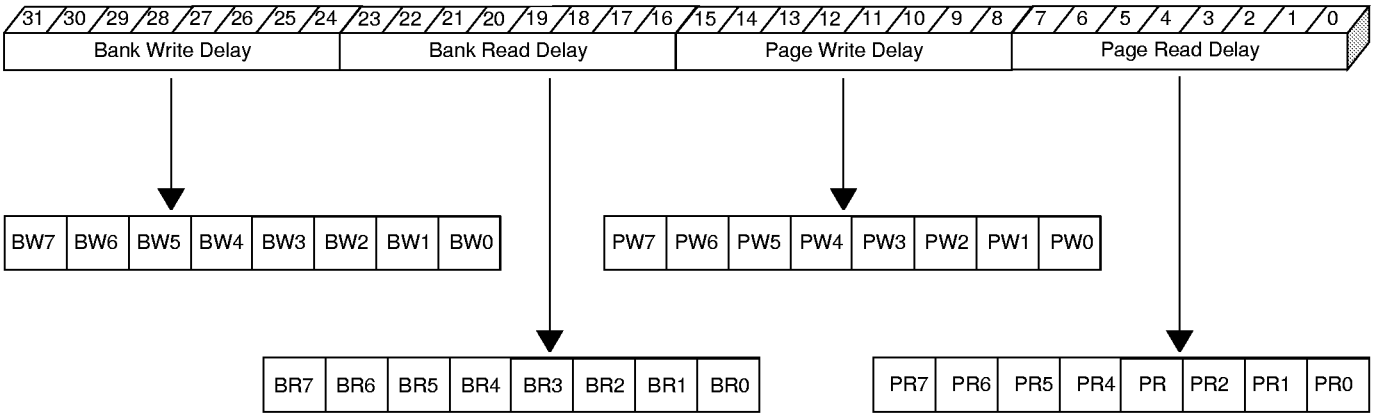


Figure 34
ACTUAL DELAY REGISTER FIELDS

Actual Delay Register

This register contains the actual Page Read Delay, Page Write Delay, Bank Read Delay, and Bank Write Delay settings for the device. These values will reflect any subsequent modifications to the initial values; such modifications may result from controller programming of the corresponding Control Registers or from Fine Read Vernier adjustments.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 35
REGISTER READ REQUEST PACKET - ACTUAL DELAY REGISTER

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
0	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
0	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
0	BW7	BW6	BW5	BW4	BW3	BW2	BW1	BW0

Figure 36
REGISTER READ DATA PACKET - ACTUAL DELAY REGISTER

Actual Delay Register - Actual Page Read Delay Field

This register contains the Actual Page Read Delay supported by the device (measured in integer clock ticks between receiving a Page Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

PRx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 37
ACTUAL DELAY REGISTER - ACTUAL PAGE READ DELAY FIELD DEFINITION

Actual Delay Register - Actual Page Write Delay Field

This field contains the Actual Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

PWx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 38
ACTUAL DELAY REGISTER - ACTUAL PAGE WRITE DELAY FIELD DEFINITION

Actual Delay Register - Actual Bank Read Delay Field

This register contains the Actual Bank Read Delay supported by the device (measured in integer clock ticks between receiving a Bank Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

BRx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 39
ACTUAL DELAY REGISTER - ACTUAL BANK READ DELAY FIELD DEFINITION

Actual Delay Register - Actual Bank Write Delay Field

This register contains the Actual Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

BWx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 40
ACTUAL DELAY REGISTER - ACTUAL BANK WRITE DELAY FIELD DEFINITION

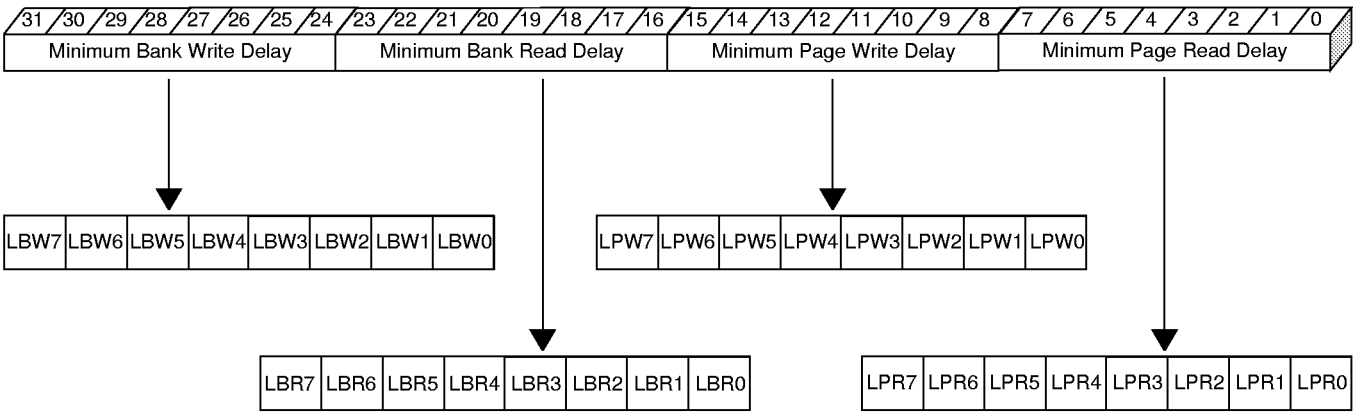


Figure 41
MINIMUM DELAY REGISTER FIELDS

Minimum Delay Register

This register contains the minimum Page Read Delay, Page Write Delay, Bank Read Delay, and Bank Write Delay settings for the device.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 42
REGISTER READ REQUEST PACKET - MINIMUM DELAY REGISTER

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	LPR7	LPR6	LPR5	LPR4	LPR3	LPR2	LPR1	LPR0
0	LPW7	LPW6	LPW5	LPW4	LPW3	LPW2	LPW1	LPW0
0	LBR7	LBR6	LBR5	LBR4	LBR3	LBR2	LBR1	LBR0
0	LBW7	LBW6	LBW5	LBW4	LBW3	LBW2	LBW1	LBW0

Figure 43
REGISTER READ DATA PACKET - MINIMUM DELAY REGISTER

The value contained in a particular Minimum Delay Register is the sum of the analog and digital values in the corresponding timing parameter registers, with the analog value having been converted to digital using the minimum CCLK cycle time of the device and rounding up to the next highest integer value. If the device is used at a slower frequency, the controller should compute these values using the timing parameter values and the actual operating frequency, and disregard the values of the Minimum Delay registers.

Minimum Delay Register - Minimum Page Read Delay Field

This register contains the minimum Page Read Delay supported by the device (measured in integer clock ticks between receiving a Page Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

LPRx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 44
MINIMUM DELAY REGISTER - MINIMUM PAGE READ DELAY FIELD DEFINITION

Minimum Delay Register - Minimum Page Write Delay Field

This register contains the minimum Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

LPWx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 45
MINIMUM DELAY REGISTER - MINIMUM PAGE WRITE DELAY FIELD DEFINITION

Minimum Delay Register - Minimum Bank Read Delay Field

This register contains the minimum Bank Read Delay supported by the device (measured in integer clock ticks between receiving a Bank Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

LBRx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 46
MINIMUM DELAY REGISTER - MINIMUM BANK READ DELAY FIELD DEFINITION

Minimum Delay Register - Minimum Bank Write Delay Field

This register contains the minimum Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

LBWx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 47
MINIMUM DELAY REGISTER - MINIMUM BANK WRITE DELAY FIELD DEFINITION

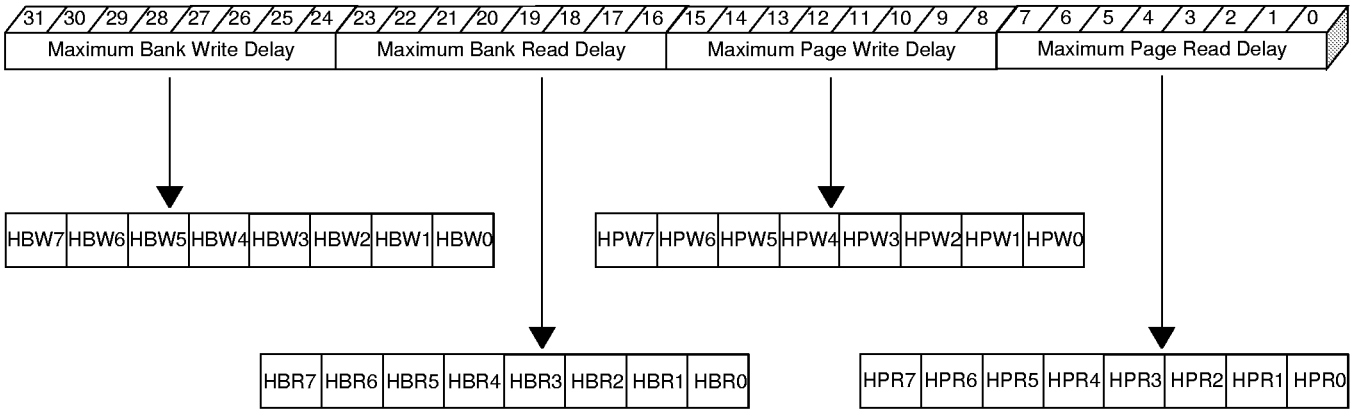


Figure 48
MAXIMUM DELAY REGISTER FIELDS

Maximum Delay Register

This register contains the maximum Page Read Delay, Page Write Delay, Bank Read Delay, and Bank Write Delay settings for the device.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 49
REGISTER READ REQUEST PACKET - MAXIMUM DELAY REGISTER

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	HPR7	HPR6	HPR5	HPR4	HPR3	HPR2	HPR1	HPR0
0	HPW7	HPW6	HPW5	HPW4	HPW3	HPW2	HPW1	HPW0
0	HBR7	HBR6	HBR5	HBR4	HBR3	HBR2	HBR1	HBR0
0	HBW7	HBW6	HBW5	HBW4	HBW3	HBW2	HBW1	HBW0

Figure 50
REGISTER READ DATA PACKET - MAXIMUM DELAY REGISTER

The value contained in a particular Maximum Delay Register is the sum of the analog and digital values in the corresponding timing parameter registers, with the analog value having been converted to digital using the minimum CCLK cycle time of the device and rounding up to the next highest integer value. If the device is used at a slower frequency, the controller should compute these values using the timing parameter values and the actual operating frequency, and disregard the values of the Maximum Delay registers.

Maximum Delay Register - Minimum Page Read Delay Field

This register contains the maximum Page Read Delay supported by the device (measured in integer clock ticks between receiving a Page Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

HPRx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 51
MAXIMUM DELAY REGISTER - MAXIMUM PAGE READ DELAY FIELD DEFINITION

Maximum Delay Register - Maximum Page Write Delay Field

This register contains the maximum Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

HPWx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 52
MAXIMUM DELAY REGISTER - MAXIMUM PAGE WRITE DELAY FIELD DEFINITION

Maximum Delay Register - Maximum Bank Read Delay Field

This register contains the maximum Bank Read Delay supported by the device (measured in integer clock ticks between receiving a Bank Read Request Packet and providing the corresponding Read Data output, as shown later in this data sheet).

HBRx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 53
MAXIMUM DELAY REGISTER - MAXIMUMBANK READ DELAY FIELD DEFINITION

Maximum Delay Register - Maximum Bank Write Delay Field

This register contains the maximum Page Write Delay supported by the device (measured in integer clock ticks between receiving a Page Write Request Packet and receiving the corresponding Write Data input, as shown later in this data sheet).

HBWx: 7 6 5 4 3 2 1 0	Integer Number of Clock Ticks
0 0 0 0 0 0 0 0	0
:	:
1 1 1 1 1 1 1 1	255

Figure 54
MAXIMUM DELAY REGISTER - MAXIMUM BANK WRITE DELAY FIELD DEFINITION

Test Register

This register contains test data meaningful only to the specific device vendor.

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 55
REGISTER READ REQUEST PACKET - TEST REGISTER

Timing Parameter Registers

The timing parameter registers contain representations of the corresponding timing parameters included in the device data sheet. The controller can use this information to program optimal timing based on the performance level(s) of the devices actually resident in the system.

Each register contains values for two timing parameters, and there is a digital component and an analog component for each parameter. The general format for data from a timing parameter register read is shown below.

DQ17-8	DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
0	PARAMETER 0 DIGITAL VALUE
0	PARAMETER 0 ANALOG VALUE
0	PARAMETER 1 DIGITAL VALUE
0	PARAMETER 1 ANALOG VALUE

Figure 56
GENERAL DATA FORMAT - TIMING PARAMETER REGISTER READ

The digital component is an integer value (from 0-255) that is independent of operating frequency. The analog value (in ns) is calculated by multiplying the step size represented by A7-A5 (Truth Table 4) by the decimal value represented by A4-A0 (the number of steps).

The total value (analog plus digital) for a given parameter may be obtained, if necessary, by converting the analog value to a digital value (by dividing by the actual CCLK cycle time of the device and rounding up to the next highest integer value) and adding the result to the stored digital value.

DQ17-8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
0	A7	A6	A5	A4	A3	A2	A1	A0

Figure 57
FORMAT FOR ANALOG VALUE BYTES WITHIN TIMING REGISTER READ DATA PACKETS

A7	A6	A5	STEP SIZE (ns)	RANGE (ns)
0	0	0	8	0-248
0	0	1	4	0-124
0	1	0	2	0-62
0	1	1	1	0-31
1	0	0	0.5	0-15.5
1	0	1	0.25	0-7.75
1	1	0	0.125	0-3.875
1	1	1	0.0625	0-1.9375

TRUTH TABLE 4 - ANALOG VALUE STEP SIZES AND RANGES

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 58
REGISTER READ REQUEST PACKET - tRAS/tRP TIMING PARAMETER REGISTER

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 59
REGISTER READ REQUEST PACKET - tRC1/tRC2 TIMING PARAMETER REGISTER

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 60
REGISTER READ REQUEST PACKET - tRCD/tXSR TIMING PARAMETER REGISTER

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 61
REGISTER READ REQUEST PACKET - tWR/tWRD TIMING PARAMETER REGISTER

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	1	0
0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 62
REGISTER READ REQUEST PACKET - tPR/tBR TIMING PARAMETER REGISTER

CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	1
0	0	1	0	CMD0	0	0	0	1	0
1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

Figure 63
REGISTER READ REQUEST PACKET - tPW/tBW TIMING PARAMETER REGISTER

READ ACCESSES

Read accesses are initiated with a Read request packet, as shown in Figures 68 and 69.

When accessing an idle bank (bank read access), the request packet includes the bank, row, and column addresses, the burst length, and a bit indicating whether or not to close the row after the access. When accessing the open row in an active bank (a page read access), the same is true, except that the row address will be ignored.

During a Read access, the first of four (or eight) data words in the data packet will be available following the total read delay; the remaining three (or seven) data words will follow, one each, every 2.5ns later. The total read delay is equal to the coarse delay (Bank Read Delay or Page Read Delay) programmed into the SLDRAM registers plus the fine delay of the Read Data Vernier, and subject to the Data Offset Vernier.

The delay of the Read Data Vernier is set by incrementing/decrementing an internal counter using the corresponding Event commands. The Read Data Vernier provides adjustment of the temporal placement of data in nominal steps of tCK/32 or less, and the counter wraps at the tick boundaries (i.e. decrementing from zero results in the maximum counter value and decrements the coarse Read Delay by one; incrementing from the maximum value resets the counter to zero and increments the coarse Read Delay by one).

Figure 68 shows minimum and maximum total read delays for a bank read access, and Figure 69 shows the same for a page read access. For clarity, the DCLK timing is shown only for the minimum read delay data timing.

The selected DCLK signal is driven by the SLDRAM along with the data, but with a leading cycle to allow for internal sampling edge adjustment in the controller. The Data and DCLK transitions are nominally coincident when the Data Offset Vernier is set to zero. The controller may add skew between the DCLK transitions and the DQ transitions by adjusting the Data Offset vernier.

The Data Offset Vernier provides for offset adjustment, in nominal steps of tCK/32 or less, between the DQs (as a group) and DCLK0 (which can in turn be aligned with DCLK1). The range of adjustment is at least +/- tCK/4 and there is no wrap (i.e. incrementing beyond the max, or decrementing beyond the min, is treated as a NOP).

READ DELAY TIMING

The SLDRAM clocking scheme is designed to provide for the temporal alignment, at the memory controller data pins, of all read data, regardless of the source SLDRAM. Upon system-power up, the controller will program initial values selected to achieve the preferred timing relationships. It is expected that periodic or continuous observation, combined with calibration as needed, will be performed by the memory controller to maintain the desired timing relationships.

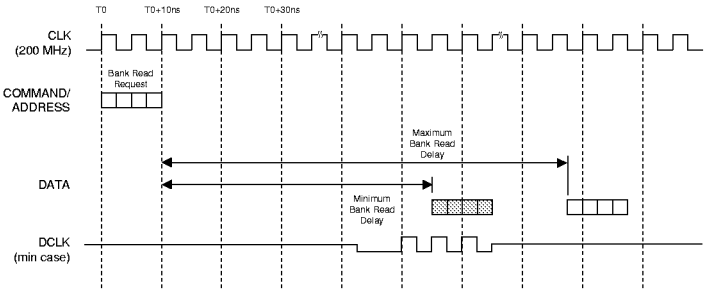


Figure 68
BANK READ ACCESS

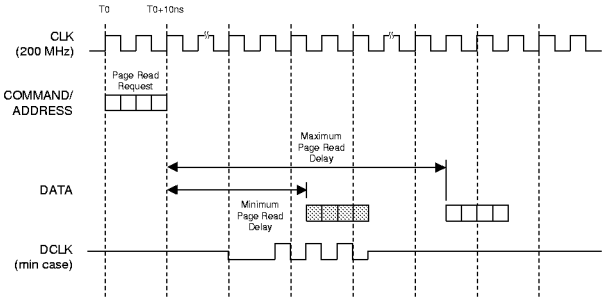


Figure 69
PAGE READ ACCESS

WRITEs

WRITE accesses are initiated with a WRITE packet request, as shown in Figures 70 and 71.

When accessing an idle bank (bank write access), the request packet includes the bank, row, and column addresses, the burst length, and a bit indicating whether or not to close the row after the access. When accessing the open row in an active bank (a page write access), the same is true, except that the row address will be ignored.

During a WRITE access, the first of four (or eight) data words in the data packet is driven by the controller, aligned with the selected DCLK, and after a delay (Bank Write Delay or Page Write Delay) programmed into the SLDRAM registers. The remaining three (or seven) data words will follow, one each, every 2.5ns later. Figure 70 shows the minimum and maximum delay before arrival of data at the SLDRAM during a bank write access. Figure 71 shows the same for a page write access. For clarity, the DCLK timing is shown only for the minimum write delay data timing.

The selected DCLK signal is driven by the controller along with the data, but with a leading cycle to allow for internal sampling edge adjustment in the SLDRAM. The Data and DCLK transitions must be nominally coincident. Although the commands and data travel in the same direction for write accesses there may be routing delay differences between the command bus and data bus. The leading LOW time on the DCLK signal allows for such differences.

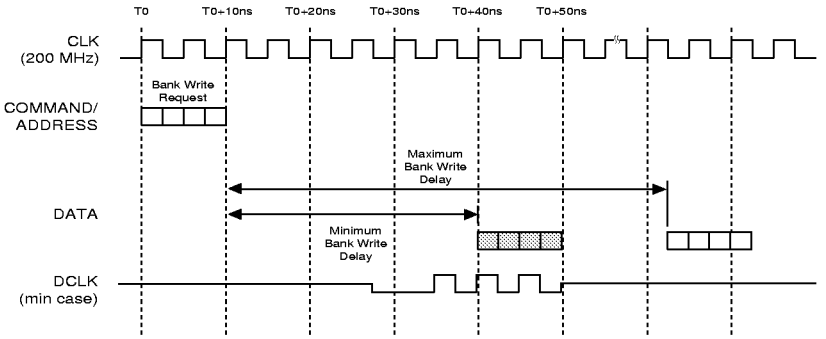


Figure 70
BANK WRITE ACCESS

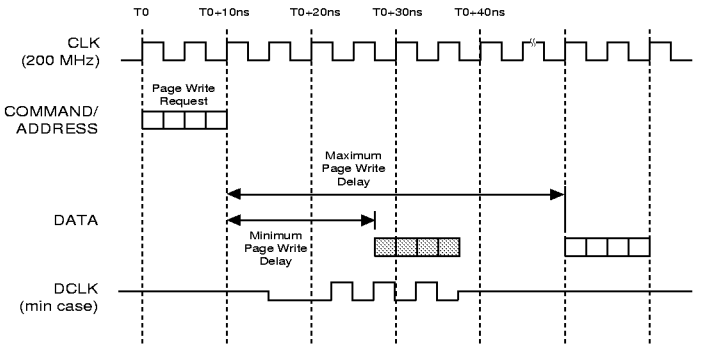


Figure 71
PAGE WRITE ACCESS

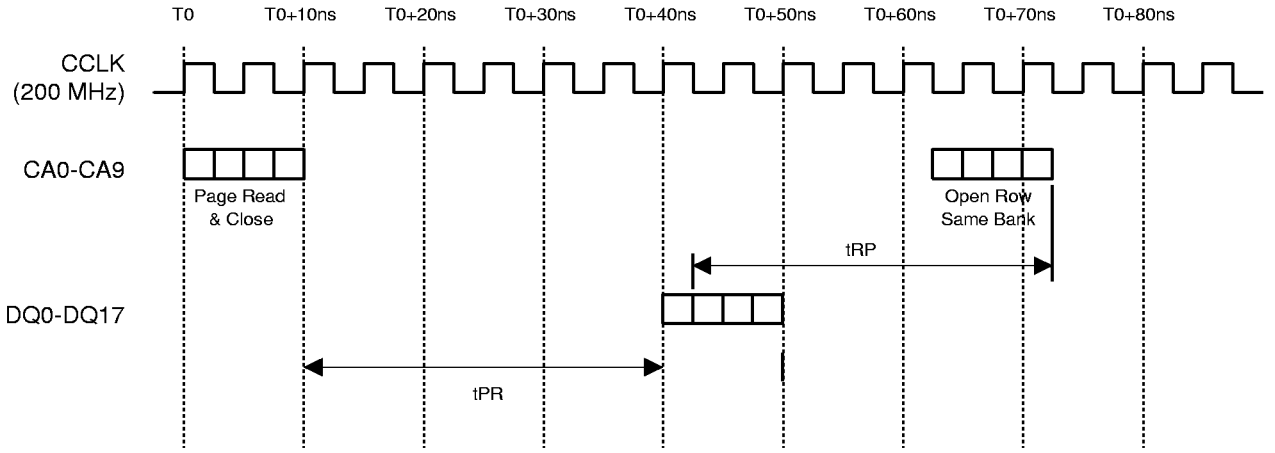


Figure 72
PAGE READ TIMING PARAMETERS

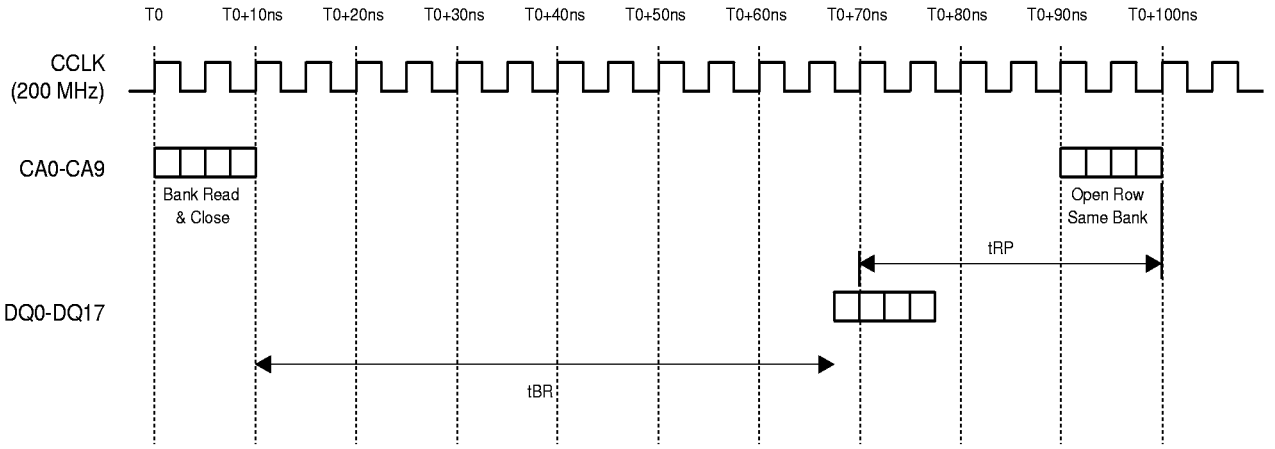


Figure 73
BANK READ TIMING PARAMETERS

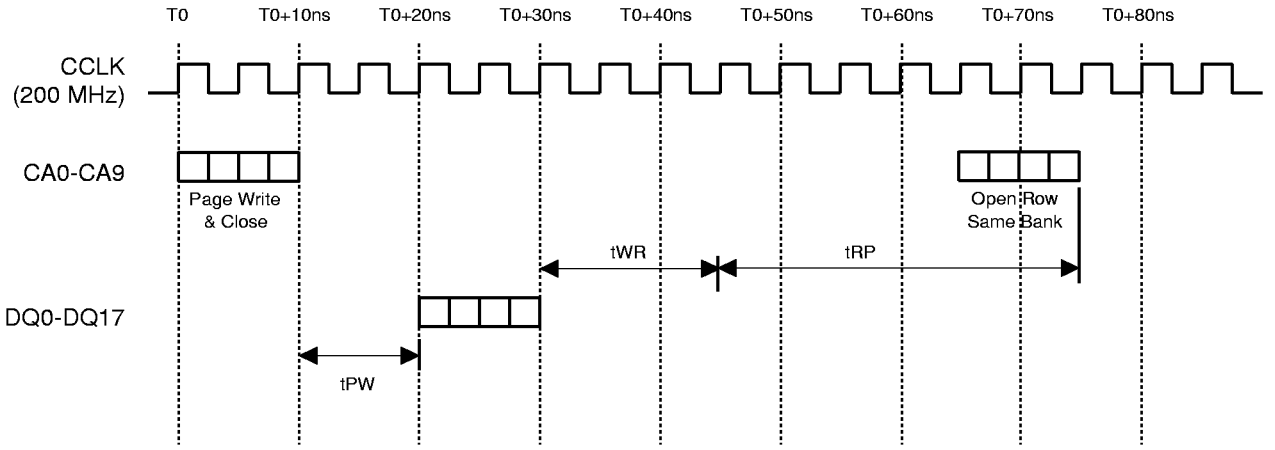


Figure 74
PAGE WRITE TIMING PARAMETERS

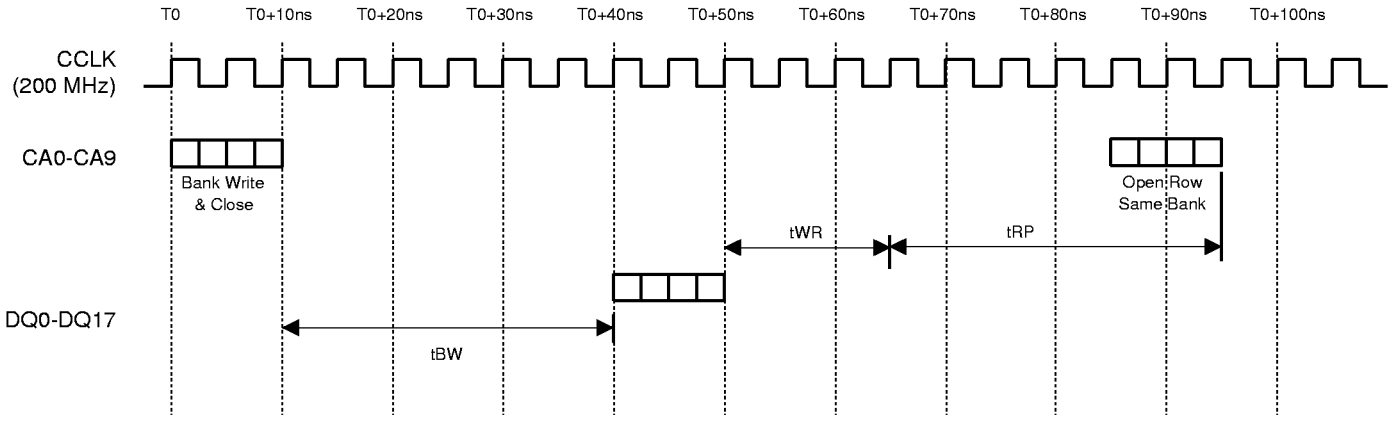


Figure 75
BANK WRITE TIMING PARAMETERS

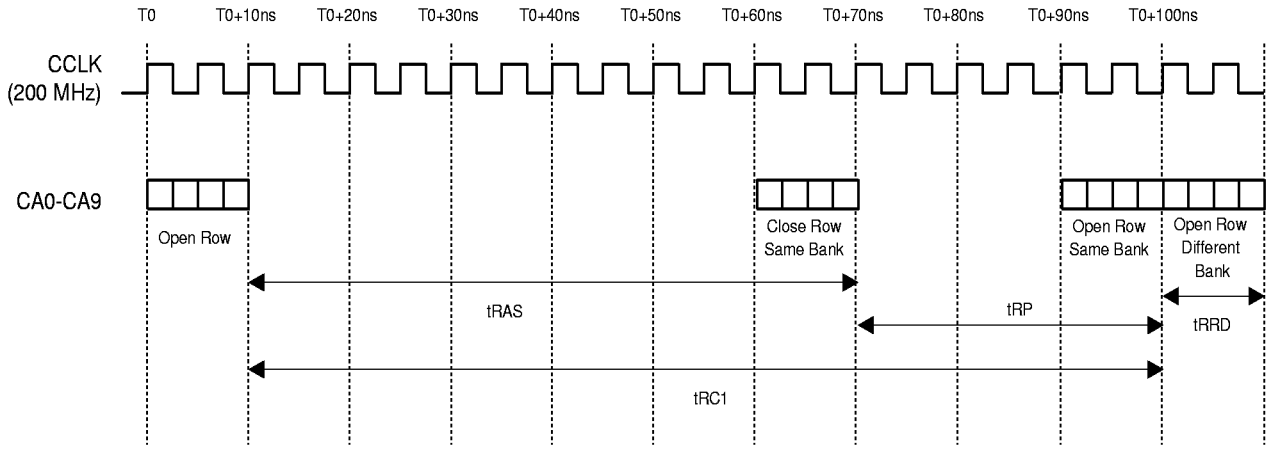


Figure 76
OPEN/CLOSE ROW TIMING PARAMETERS

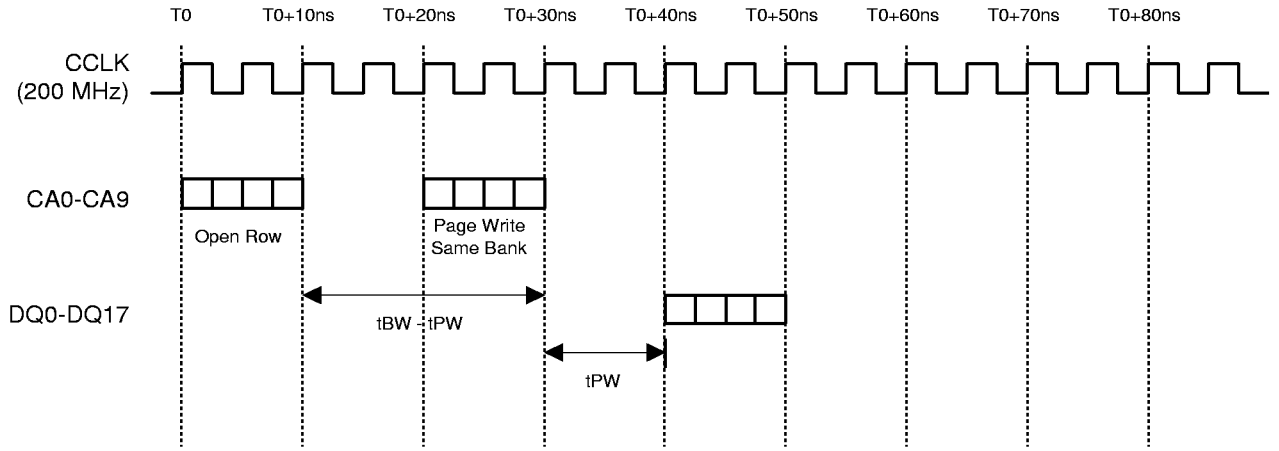


Figure 77
OPEN ROW TO PAGE WRITE TIMING PARAMETERS

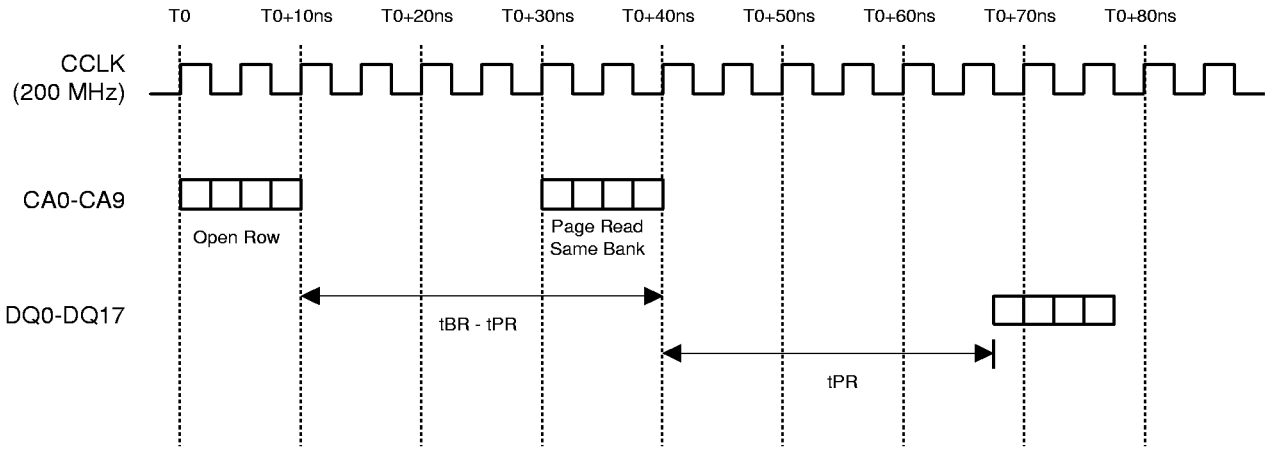


Figure 78
OPEN ROW TO PAGE READ TIMING PARAMETERS

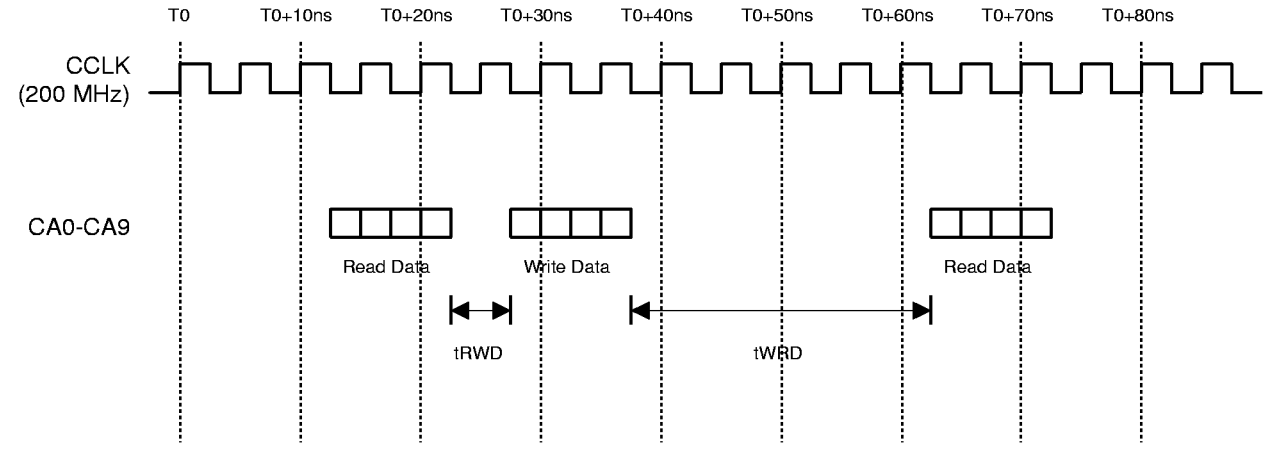


Figure 79
BUS/PIPE TURNAROUND TIMING PARAMETERS

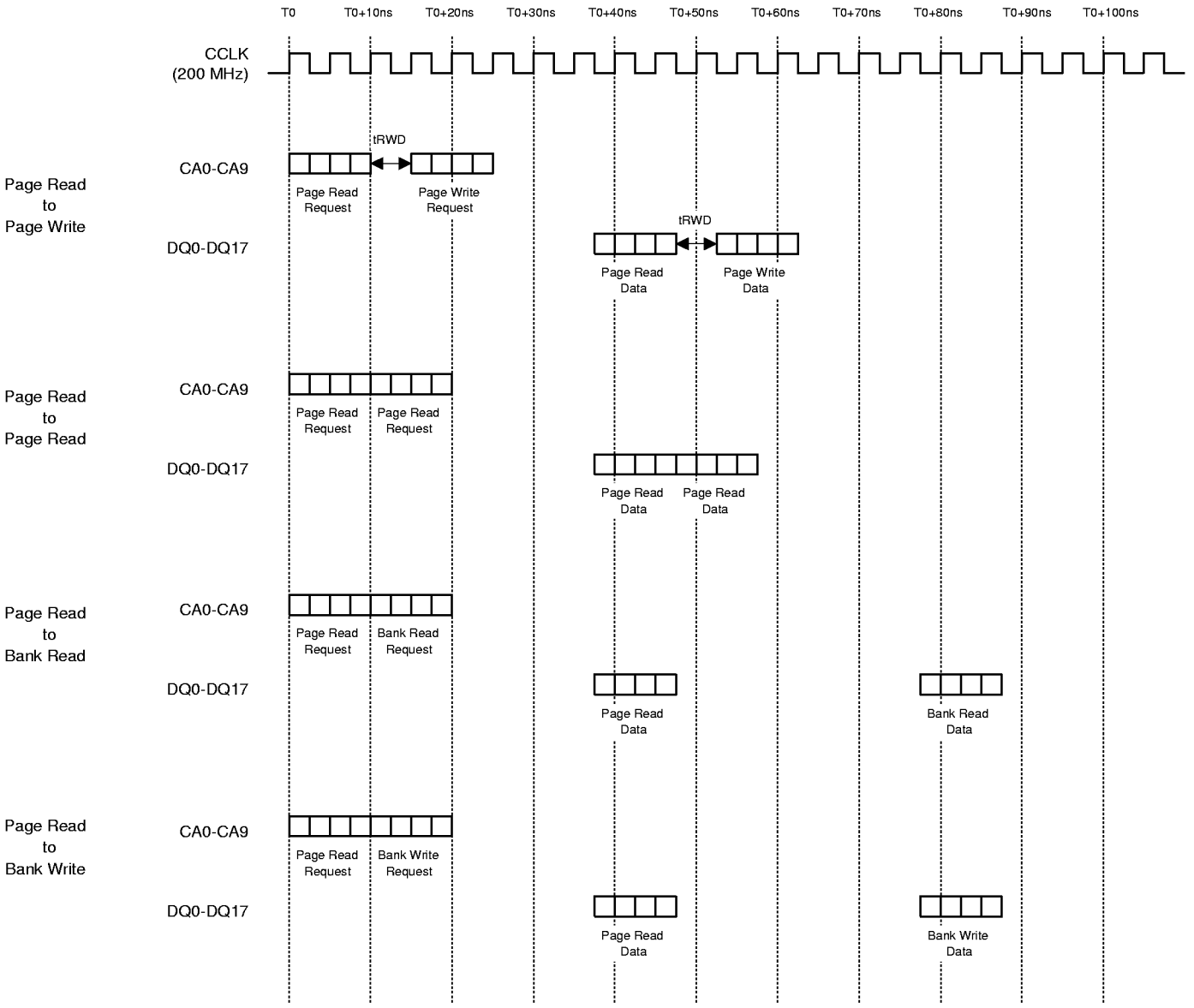


Figure 80
READ/WRITE COMMAND ISSUE RESTRICTIONS
EXAMPLE 1 - READ LATENCY = MINIMUM,
WRITE LATENCY = READ LATENCY

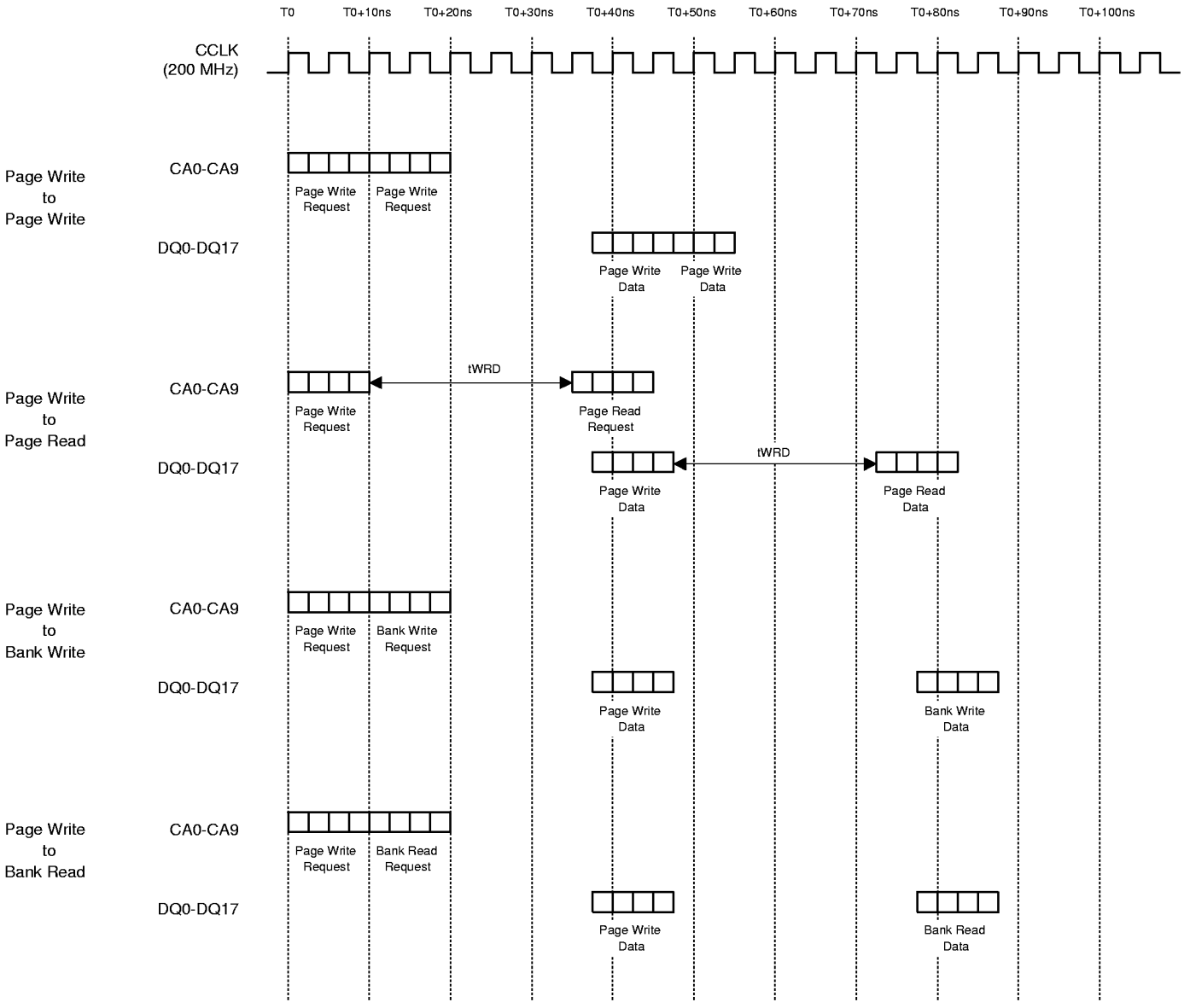


Figure 81
READ/WRITE COMMAND ISSUE RESTRICTIONS
EXAMPLE 1 - READ LATENCY = MINIMUM,
WRITE LATENCY = READ LATENCY (CONTINUED)

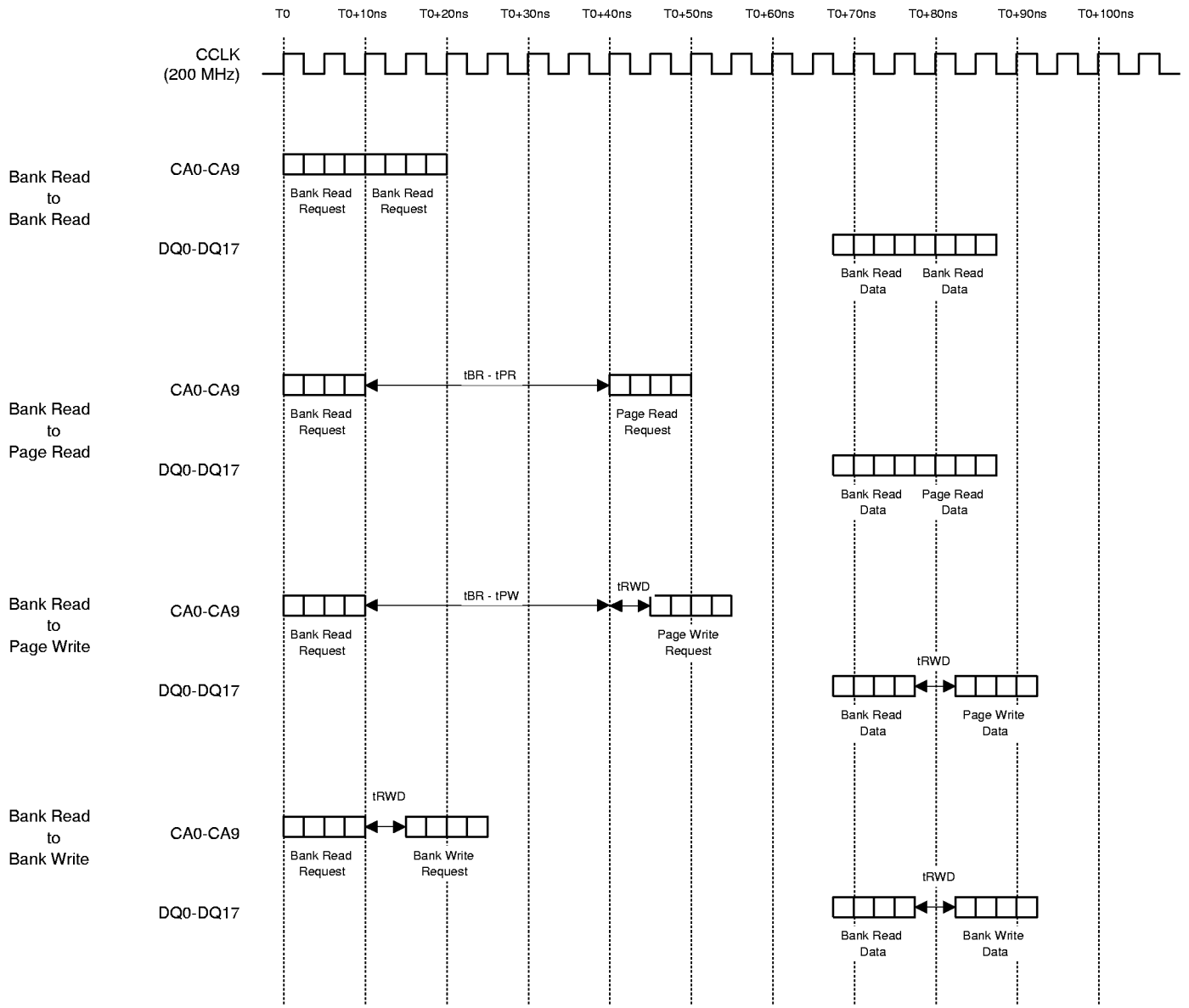


Figure 82
READ/WRITE COMMAND ISSUE RESTRICTIONS
EXAMPLE 1 - READ LATENCY = MINIMUM,
WRITE LATENCY = READ LATENCY (CONTINUED)

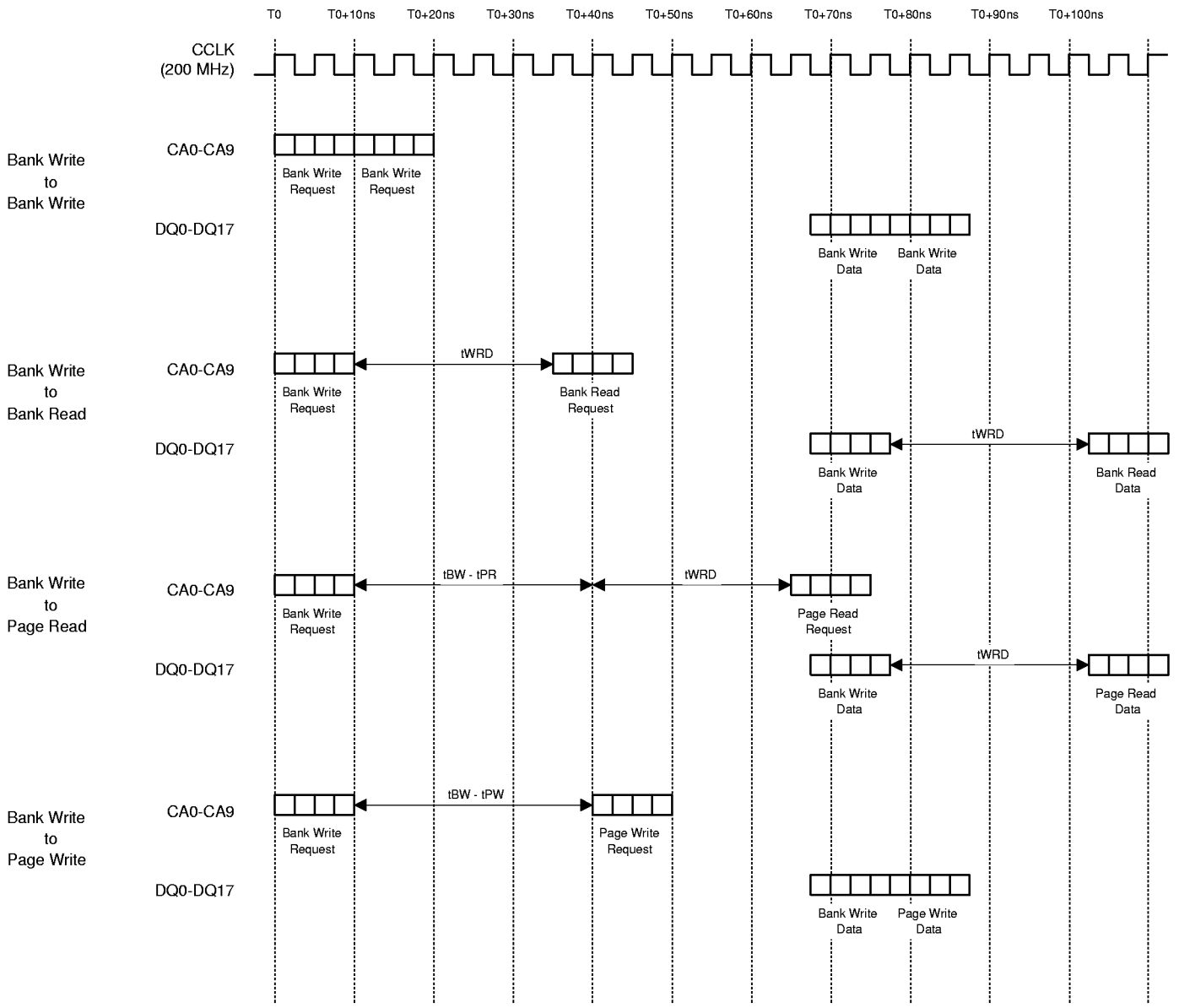


Figure 83
READ/WRITE COMMAND ISSUE RESTRICTIONS
EXAMPLE 1 - READ LATENCY = MINIMUM,
WRITE LATENCY = READ LATENCY (CONTINUED)

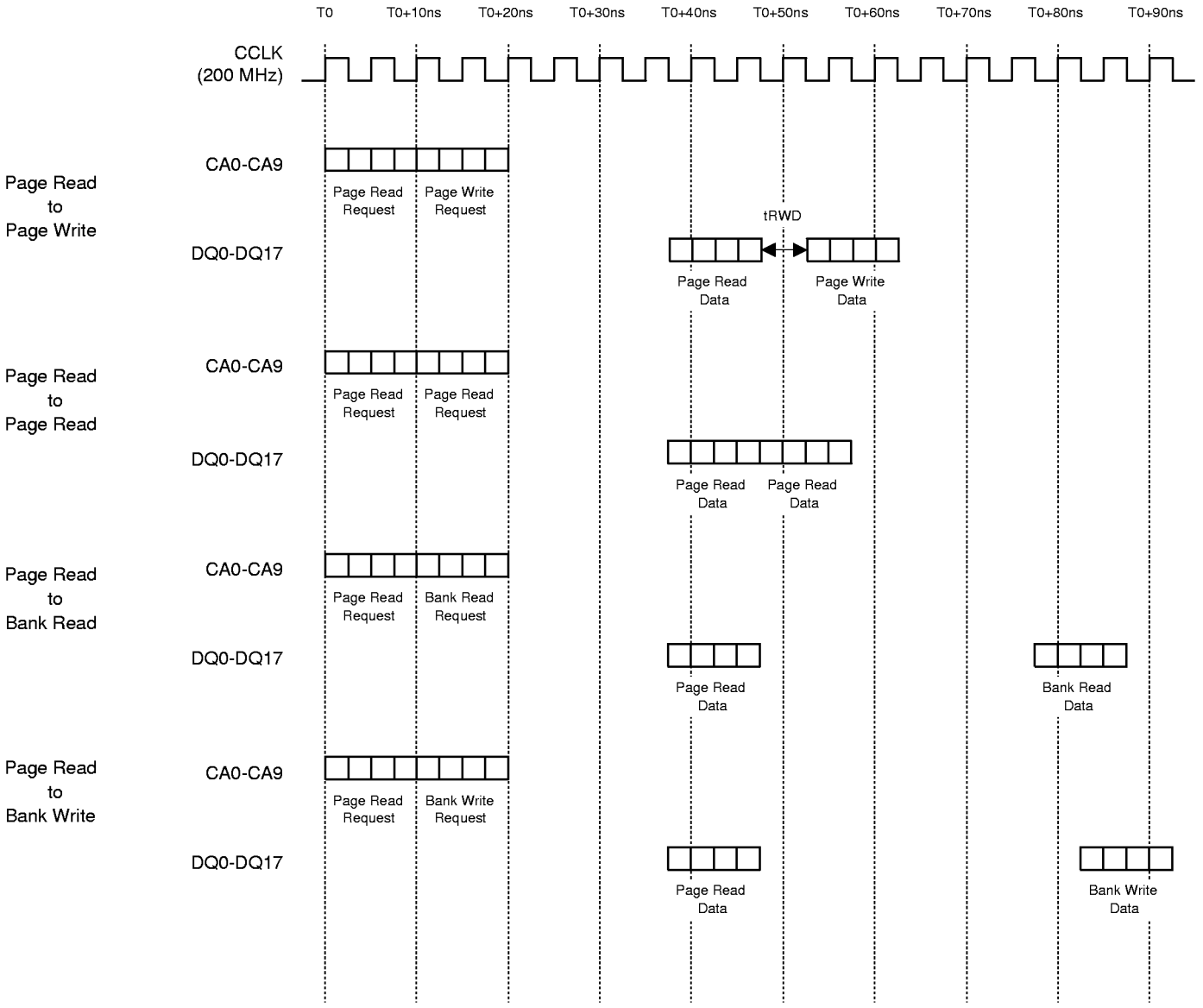


Figure 84
READ/WRITE COMMAND ISSUE RESTRICTIONS
EXAMPLE 2 - READ LATENCY = MINIMUM,
WRITE LATENCY = READ LATENCY + 2

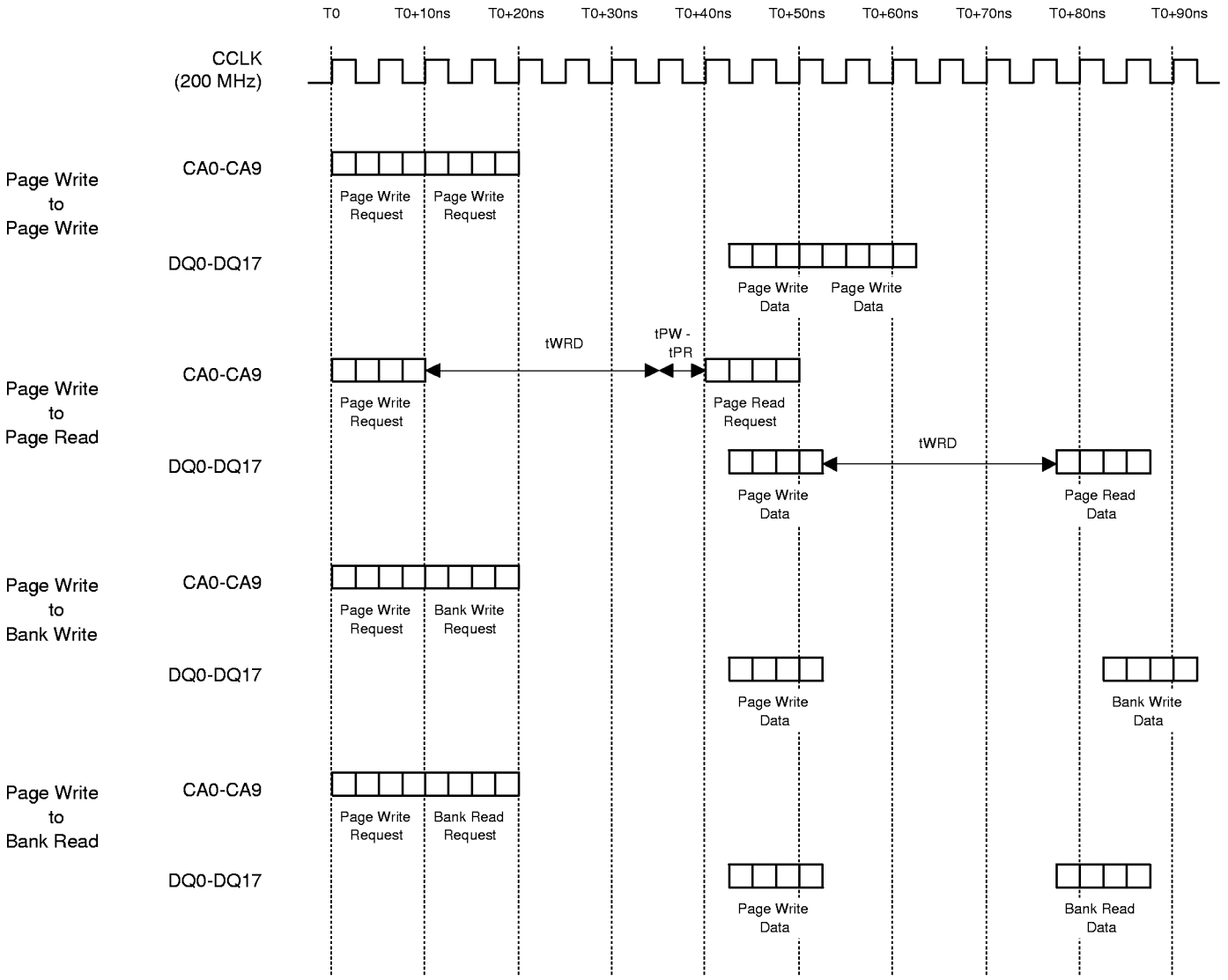


Figure 85
READ/WRITE COMMAND ISSUE RESTRICTIONS
EXAMPLE 2 - READ LATENCY = MINIMUM,
WRITE LATENCY = READ LATENCY + 2 (CONTINUED)

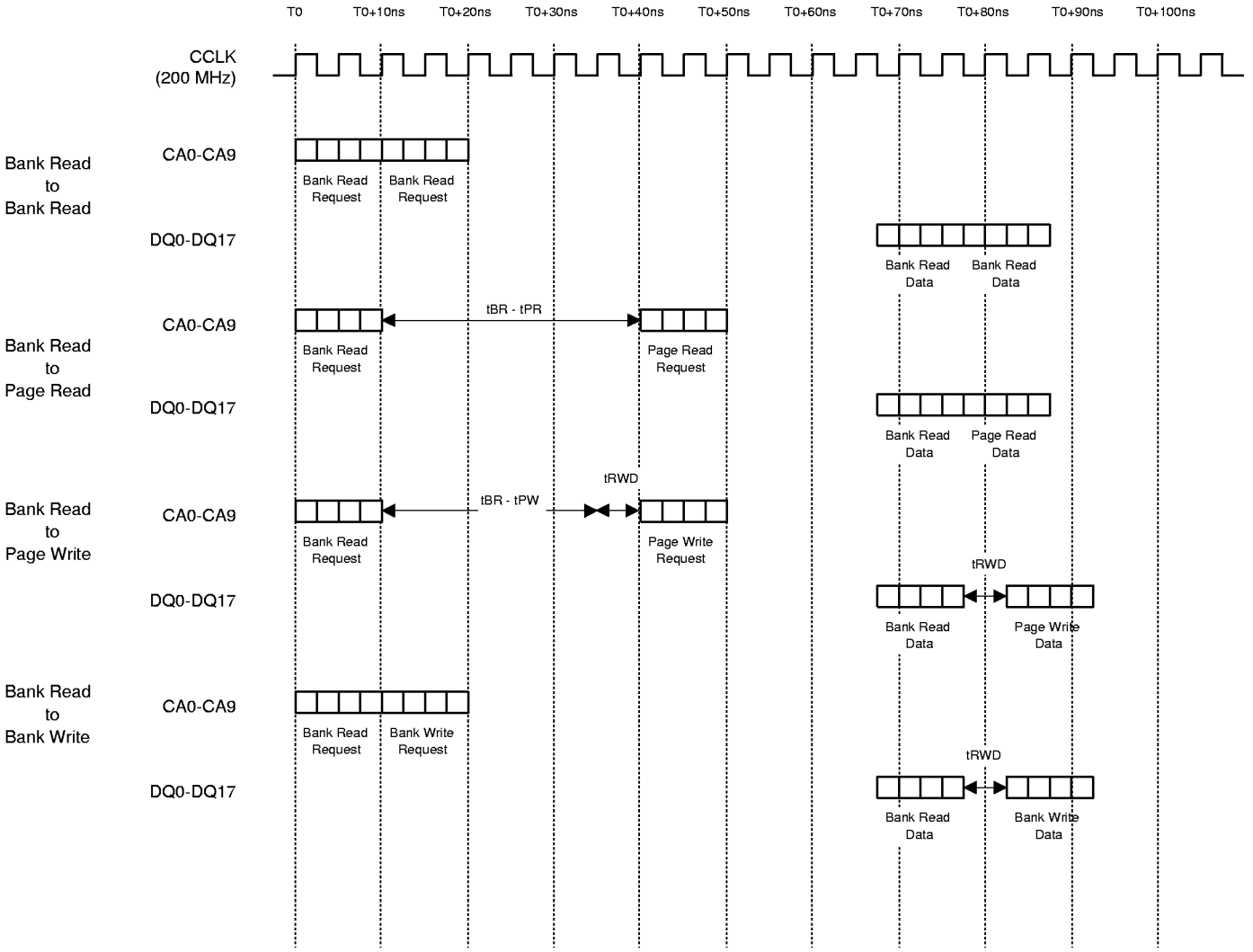


Figure 86
READ/WRITE COMMAND ISSUE RESTRICTIONS
EXAMPLE 2 - READ LATENCY = MINIMUM,
WRITE LATENCY = READ LATENCY + 2 (CONTINUED)

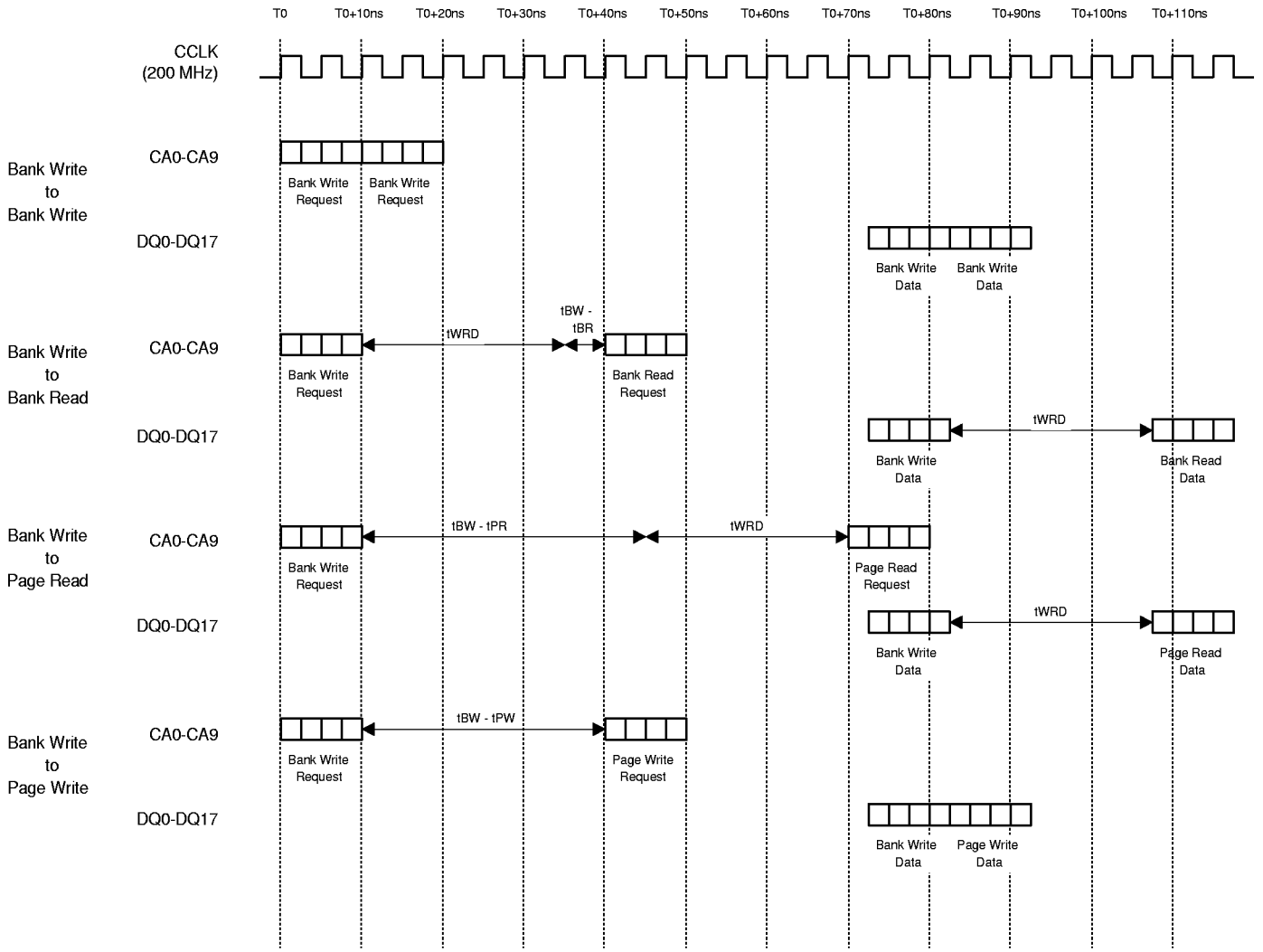


Figure 87
READ/WRITE COMMAND ISSUE RESTRICTIONS
EXAMPLE 2 - READ LATENCY = MINIMUM,
WRITE LATENCY = READ LATENCY + 2 (CONTINUED)

STANDBY MODE

In Standby Mode all output drivers are disabled and all input receivers except those for CCLK, LISTEN and LINKON are disabled. In addition, all internal circuitry that can be re-enabled within tLSC is disabled. The Standby Mode is entered by deactivating the LISTEN signal at any time except during the transfer of a request packet.

The Standby Mode may be nested within the Self Refresh Mode as shown in Figure 89.

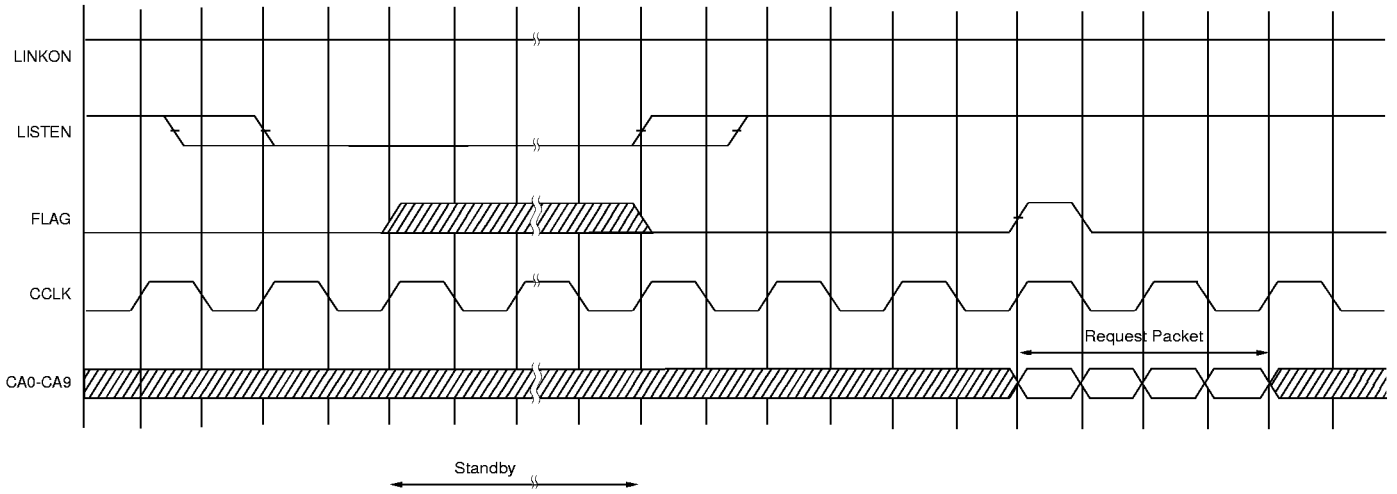


Figure 88
STANDBY MODE - GENERAL TIMING

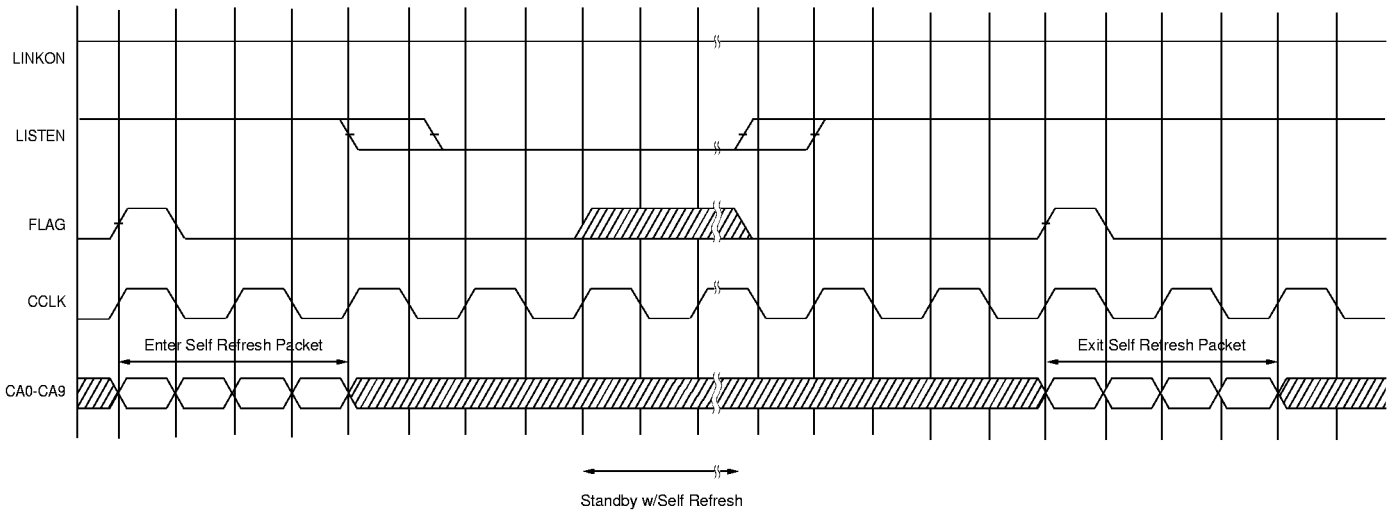


Figure 89
STANDBY MODE NESTED WITHIN SELF REFRESH MODE - GENERAL TIMING

SHUTDOWN MODE

In Shutdown Mode all internal clocks are disabled, in addition to all output drivers and all input receivers except for LINKON. The Shutdown Mode is entered by deactivating the LINKON signal while the device is already in Standby Mode.

The Shutdown Mode may be nested within the Self Refresh Mode as shown in Figure 91.

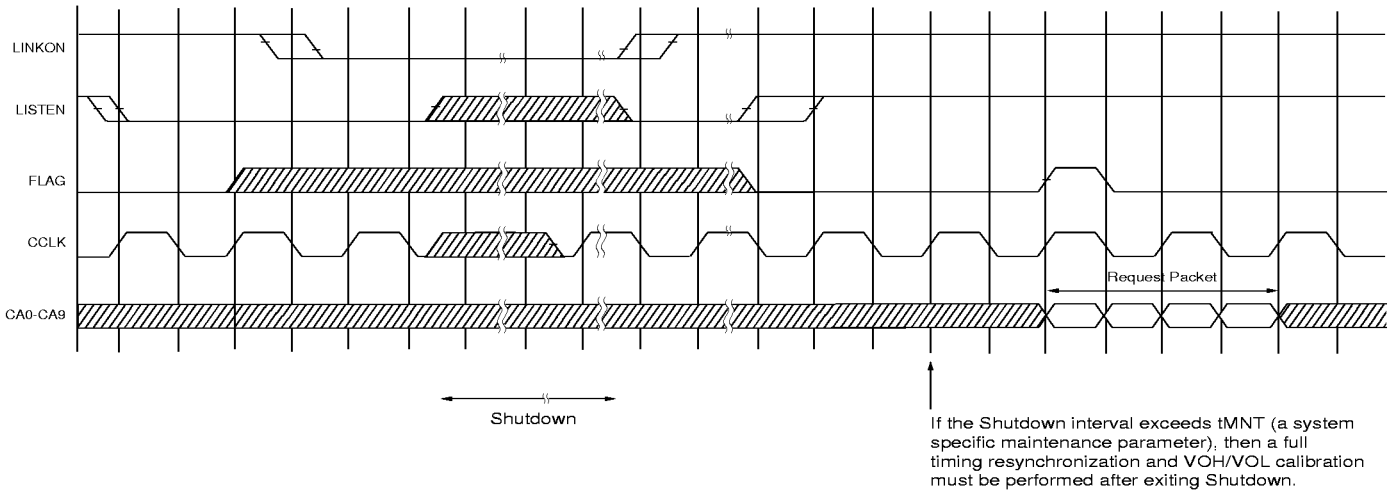


Figure 90
SHUTDOWN MODE - GENERAL TIMING

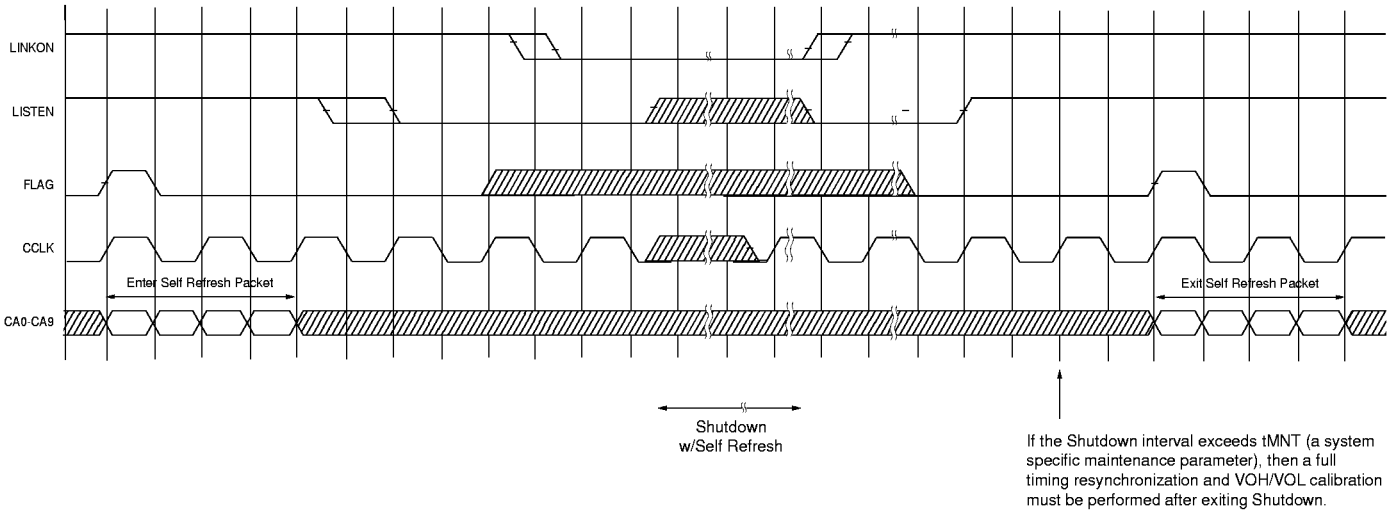


Figure 91
SHUTDOWN MODE NESTED WITHIN SELF REFRESH MODE - GENERAL TIMING

SELF-REFRESH MODE

In Self-Refresh Mode an on-chip oscillator and refresh logic are enabled, thereby suspending the requirement for periodic Auto Refresh Events initiated by the memory controller. Standy and/or Shutdown Modes may be nested within the Self-Refresh Mode. No other commands/accesses are permitted to the SLDRAM while in Self-Refresh.

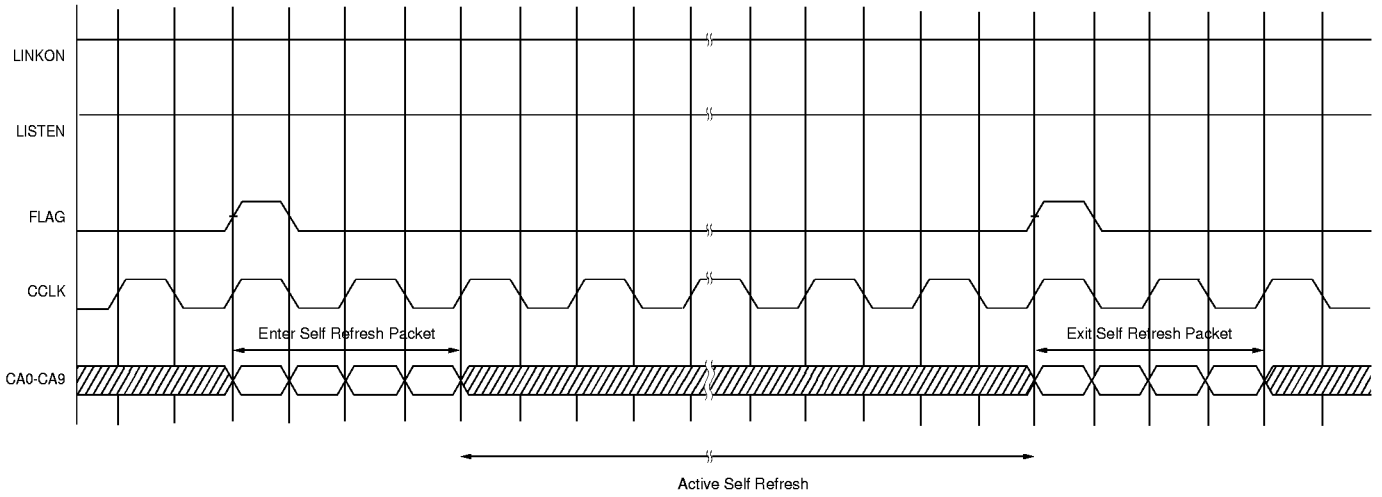


Figure 92
SELF REFRESH MODE - GENERAL TIMING

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD}/V_{DDQ} supply relative to V_{SS} ..... -0.5V to +3.6V
Voltage on Inputs relative to V_{SS} ..... -0.5V to +3.6V
Voltage on SLIO Outputs or SLIO I/O pins relative to V_{SS} ..... -0.5V to VDDQ+0.5V
Voltage on LVCMOS Outputs relative to V_{SS} ..... -0.5V to VDD+0.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.3W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note: 1, 4) (0°C≤ T_A ≤ 70°C; V_{DD}/V_{DDQ} = +2.5V ±0.125V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{DD}/V_{DDQ}	2.375	2.625	V	2
Input High (Logic 1) Voltage, SLIO	V_{IH}	V_{REF}+0.2	V_{DDQ}+0.3	V	
Input Low (Logic 0) Voltage, SLIO	V_{IL}	V_{SSQ}-0.3	V_{REF}-0.2	V	
Input High (Logic 1) Voltage, LVCMOS	V_{IH}	0.7V_{DD}	V_{DD}+0.3	V	
Input Low (Logic 0) Voltage, LVCMOS	V_{IL}	V_{SS}-0.3	0.3V_{DD}	V	
Input Reference Voltage (SLIO)	V_{REF}	0.5V_{DD}-0.05	0.5V_{DD}+0.05	V	3
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}+0.3 (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DD}Q + 0.3V LVCMOS, 0V ≤ V_{OUT} ≤ V_{DD}Q + 0.3V SLIO)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS - SLIO					
Output High Voltage	V_{OH}	1.6		V	
Output Low Voltage	V_{OL}		0.9	V	10
Calibrated Output High Voltage	V_{OH}	1.6	1.625	V	
Calibrated Output Low Voltage	V_{OL}	0.875	0.9	V	
OUTPUT LEVELS - LVCMOS					
Output High Voltage (I_{OH} = -100uA)	V_{OH}	V_{DD}-0.2		V	
Output Low Voltage (I_{OL} = 100uA)	V_{OL}		V_{SS}+0.2	V	

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: SLIO Inputs	C_{IS}	3	pF	5
Input Capacitance: LVCMOS Inputs	C_{IL}	5	pF	5
Input/Output Capacitance: SLIO I/O	C_{IOS}	3	pF	5
Input/Output Capacitance: LVCMOS I/O	C_{IOL}	6.5	pF	5

I_{DD} SPECIFICATIONS AND CONDITIONS

(Note: 1, 6, 13) (0°C≤ T_A ≤ 70°C; V_{DD}/V_{DDQ} = +2.5V ±0.125V)

		-400 MAX			
PARAMETER/CONDITION	SYMBOL	@333Mb/s/p	@400Mb/s/p	UNITS	NOTES
OPERATING CURRENT: Random Bank Reads and/or Bank Writes, Burst Length = 4, $^{t}RC1 \geq {}^{t}RC1$ MIN	I_{DD1}	TBD	TBD	mA	
OPERATING CURRENT: Page Reads and/or Page Writes to open rows, Burst Length = 4, tPR ≥ tPR MIN, tPW = tPR	I_{DD2}	TBD	TBD	mA	
AUTO REFRESH CURRENT: $^{t}RC2 \geq {}^{t}RC2$ MIN	I_{DD3}	TBD	TBD	mA	
STANDBY CURRENT: Standby mode, LISTEN ≤ V_{IL} (MAX)	I_{DD4}	TBD	TBD	mA	
STANDBY CURRENT: Shutdown mode, LINKON ≤ V_{IL} (MAX)	I_{DD5}	TBD	TBD	mA	
SELF REFRESH CURRENT:	I_{DD6}	TBD	TBD	uA	
STANDBY CURRENT: Standby-Self Refresh Mode, LISTEN ≤ V_{IL} (MAX)	I_{DD7}	TBD	TBD	uA	
STANDBY CURRENT: Shutdown-Self Refresh Mode, LINKON ≤ V_{IL} (MAX)	I_{DD8}	TBD	TBD	uA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C≤ T_A ≤ +70°C)

AC CHARACTERISTICS		-400			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
Command Input (CAn, FLAG) Valid time	^{t}CIV	950		ps	
Command Input (CAn, FLAG) Skew	^{t}CIS		775	ps	
Command Clock (CCLK) Valid time	^{t}CCV	1380		ps	
Command Clock (CCLK) Skew	^{t}CCS		560	ps	
Clock Cycle time	^{t}CK	5	10	ns	
CCLK Frequency Stability/Long Term Jitter	-		4	%	
CCLK/DCLK Short Term Jitter	-		1	%	
Command to DCLK Delay (for DCLK HIGH, LOW, TOGGLING or HIGH-Z)	^{t}DD		20	ns	
Data Input (DQn) Valid Time	^{t}DIV	950		ps	
Data Input (DQn) Skew	^{t}DIS		775	ps	
Data Clock Input (DCLKn) Valid Time	^{t}DCIV	1380		ps	
Data Clock Input (DCLKn) Skew	^{t}DCIS		560	ps	
Data Ouput (DQn) Valid Time	^{t}DOV	1900		ps	
Data Output (DQn) Skew	^{t}DOS		300	ps	
Data Clock Ouput (DCLKn) Valid Time	^{t}DCOV	2080		ps	
Data Clock Output (DCLKn) Skew	^{t}DCOS		210	ps	
Data-out high-impedance time	^{t}HZ		125	ps	6
Data-out low-impedance time	^{t}LZ	125		ps	6
Open Row to Close Row command period (same bank)	^{t}RAS	60		ns	7
Open Row to Open Row command period (same bank)	^{t}RC1	88		ns	7
Auto Refresh to Auto Refresh Command period	^{t}RC2	88		ns	7
Refresh period (8,192 cycles)	^{t}REF		64	ms	
Close Row (precharge) command period	^{t}RP	28		ns	7
Open Row to Open Row command period (different bank)	^{t}RRD	10		ns	7
Write recovery time (FIFO uncertainty portion; total Write Recovery =^{t}WR_D+^{t}WR_A)	^{t}WR_D	2		ticks	7
Write recovery time (internal write portion; total Write Recovery =^{t}WR_D+^{t}WR_A)	^{t}WR_A	10		ns	7
Exit SELF REFRESH to Open Row command	^{t}XSR	88		ns	7
Minimum Page Read Delay	^{t}PR (^{t}AA)		26-30	ns	7
Minimum Bank Read Delay	^{t}BR (^{t}RAC)		56-64	ns	7
Minimum Page Write Delay	^{t}PW	17		ns	7
Minimum Bank Write Delay	^{t}BW	30		ns	7
Maximum Page Read Delay	^{t}PR_MAX		32	ticks	
Maximum Bank Read Delay	^{t}BR_MAX		64	ticks	
Maximum Page Write Delay	^{t}PW_MAX		32	ticks	
Maximum Bank Write Delay	^{t}BW_MAX		64	ticks	
Minimum Read to Write Delay (external I/O turnaround)	^{t}RWD	5		ns	
Minimum Write to Read Delay (internal I/O and data pipeline turnaround) - FIFO Portion	^{t}WRD_D	2		ticks	7
Minimum Write to Read Delay (internal I/O and data pipeline turnaround) - Balance	^{t}WRD_A	20		ns	7,8
VDD/VDDQ to Vterm Set Up Time	^{t}VTD	2		us	
VREF to Inputs Valid Set Up Time	^{t}IV	0		ns	
Reset# Pulse Width	^{t}RST	100		ns	
Reset# Active to Output Valid Delay	^{t}RSO	80		ns	
Input Set Up Time	^{t}SI	10		ns	

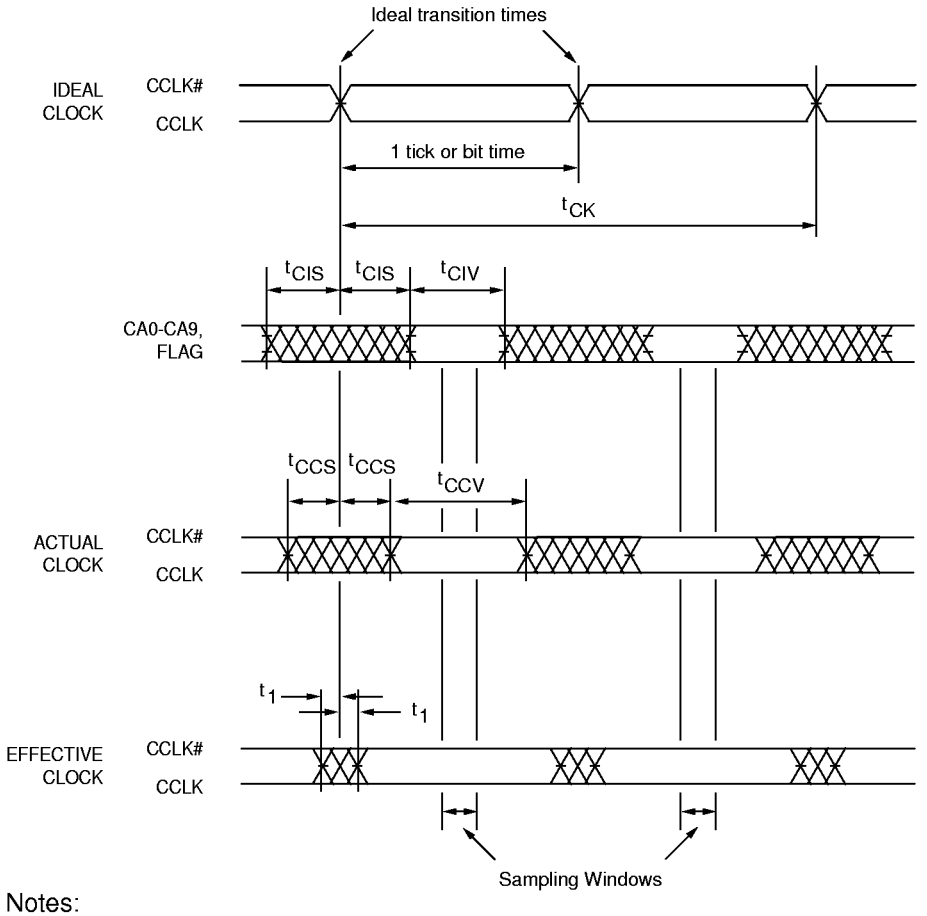
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C≤ T_A ≤ +70°C)

AC CHARACTERISTICS		-400			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
ID Write Request to SO Output Delay	^{t}ID		20	ns	
Listen to Linkon Low Set Up Time	^{t}LLS	5		ns	
Listen to Linkon Low Hold Time	^{t}LLH	5		ns	
Listen to Linkon High Set Up Time	^{t}LHS	0		ns	
Listen to Linkon High Hold Time - Cold	^{t}LHHC	500		ns	
Listen to Linkon High Hold Time - Warm	^{t}LHHW	50		ns	
Input to Listen Set Up Time	^{t}ILS	0		ns	
Input to Listen Hold Time	^{t}ILH	5		ns	
Listen to Next Command Set Up Time	^{t}LSC	10		ns	
Vernier Adjust to Output Delay (no accesses in progress)	^{t}VO		10	ns	
VOH/VOL Adjust to Output Delay (no accesses in progress)	^{t}LO		10	ns	
Control Register Write to Next Command Set Up Time (all banks closed)	^{t}CC	10		ns	
Clock Stable to Reset# Inactive Set Up Time	^{t}CSI	100		ns	9
Clock Stable to Linkon High Set Up Time	^{t}CS	1		^{t}CK	
Last Command to Listen Low Set Up Time	^{t}PLI	0		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. $V_{DDQ} \leq V_{DD}$.
3. $|V_{TERM} - V_{REF}| \leq 50mV$.
4. Variations in V_{DDQ}, V_{TERM} and V_{REF} must track each other.
5. This parameter is sampled. V_{DD}, V_{DDQ} = +2.5V ±0.125V; f = 1 MHz, tA = 25 deg C.
6. tHZ and tLZ specifications reflect the transition time between the V_{TERM} voltage to which the signal is terminated in the system and the valid input logic levels. These parameters are not tested directly, but are indirectly verified in testing the skew of the output signals.
7. The value of this parameter is also represented in a Timing Parameter register in the device.
8. This parameter includes margin to cover tAA guardband and possible rounding error.
9. An external buffer device in the system may have a more restrictive value for this parameter.
10. The output voltage is measured on the bus side of the series (stub) resistor, with a parallel resistor to V_{TERM}. The output voltages are shown for a series resistor value of 20 ohms and a parallel resistor value of 28 ohms.



Notes:

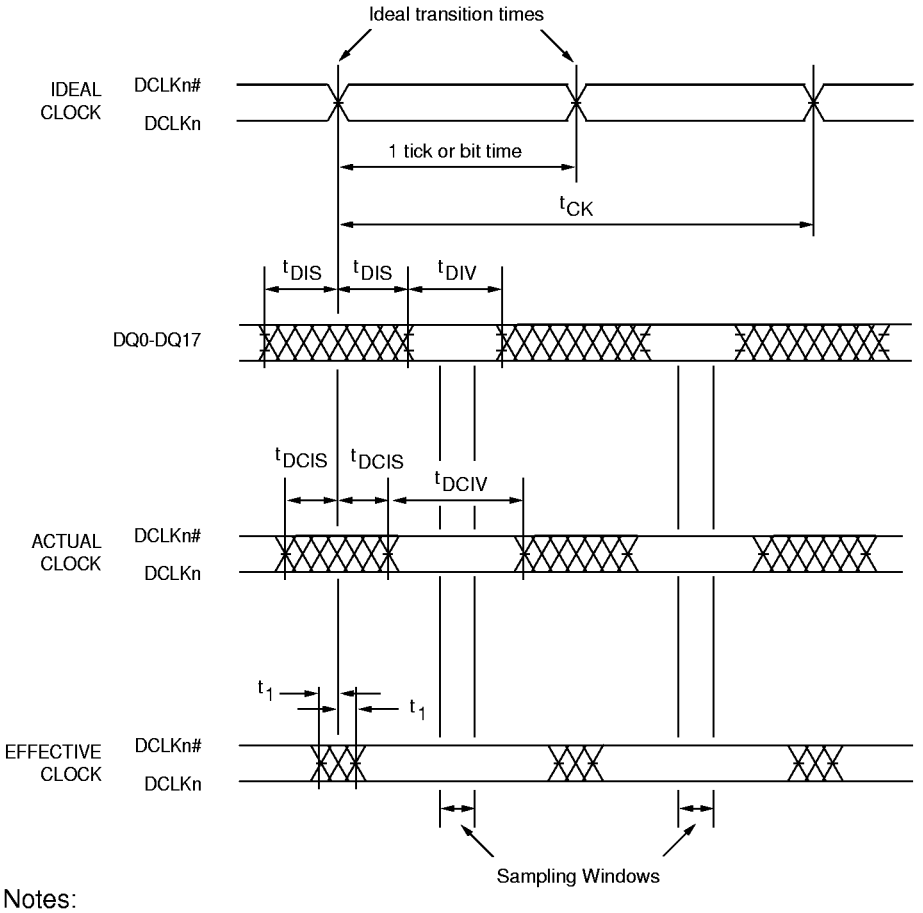
1. The Command and Actual Clock signals are shown as they are required to appear at the inputs to the receiving device. These signals are required to exhibit much less skew when leaving the transmitting device (as show for the output data in Figure 95).

2. Additional skew may occur in the input stage of the receiving device; this skew is accounted for in the device timing specifications.

3. The Effective Clock signal is shown to illustrate the effects of the timing adjustments supported by SLDRAM devices. The remaining clock skew after adjustment is equal to the resolution of the input sampling vernier (the same resolution as the Data Offset vernier, tCK/32) plus the budgeted system dynamic skew. Parameter t1 represents one-half this amount and is defined to show the total skew centered on the imaginary ideal transition. The internal sampling occurs within the same size window, located one-half bit time later (in the center of the data eye).

4. Details related to the system level analysis and timing budget will be provided in separate documentation.

Figure 93
COMMAND INPUT TIMING



Notes:

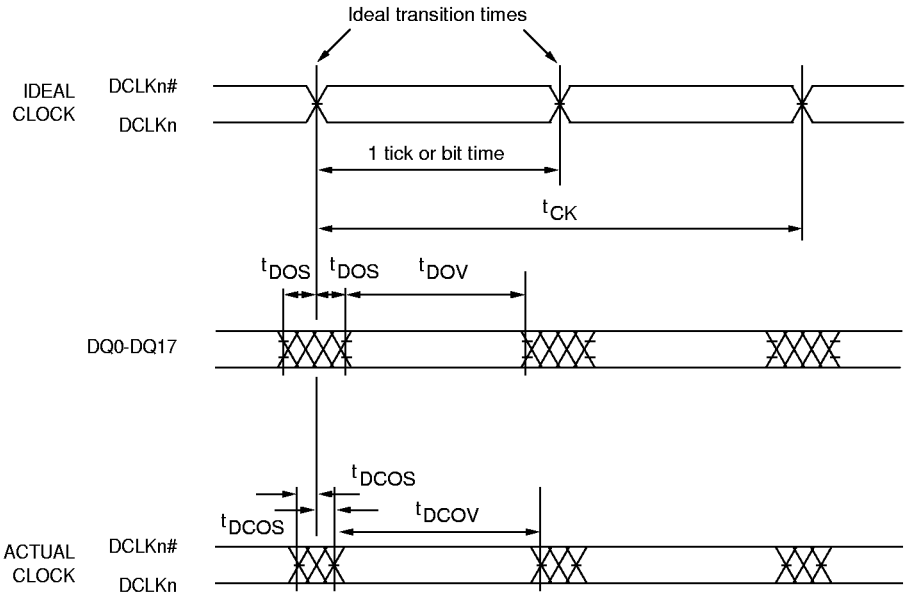
1. The Input Data and Actual Data Clock signals are shown as they are required to appear at the inputs to the receiving device. These signals are required to exhibit much less skew when leaving the transmitting device (as show for the output data in Figure 95).

2. Additional skew may occur in the input stage of the receiving device; this skew is accounted for in the device timing specifications.

3. The Effective Clock signal is shown to illustrate the effects of the timing adjustments supported by SLDRAM devices. The remaining clock skew after adjustment is equal to the resolution of the input sampling vernier (the same resolution as the Data Offset vernier, tCK/32) plus the budgeted system dynamic skew. Parameter t1 represents one-half this amount and is defined to show the total skew centered on the imaginary ideal transition. The internal sampling occurs within the same size window, located one-half bit time later (in the center of the data eye).

4. Details related to the system level analysis and timing budget will be provided in separate documentation.

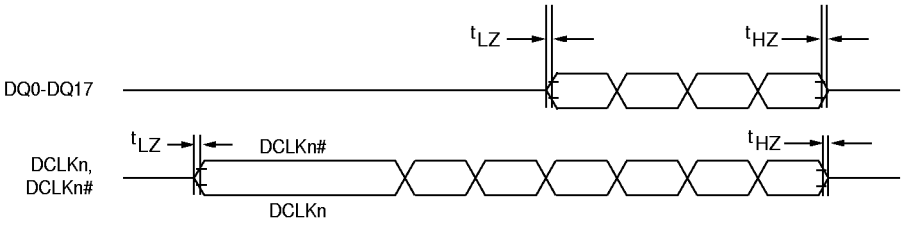
Figure 94
DATA INPUT TIMING



Notes:
1. The Output Data and Data Clock signals are shown as they are required to appear at the outputs of the receiving device. These signals will incur additional skew in the system before reaching the receiving device; this skew is accounted for in the device timing specifications.

2. Details related to the system level analysis and timing budget will be provided in separate documentation.

Figure 95
DATA OUTPUT TIMING

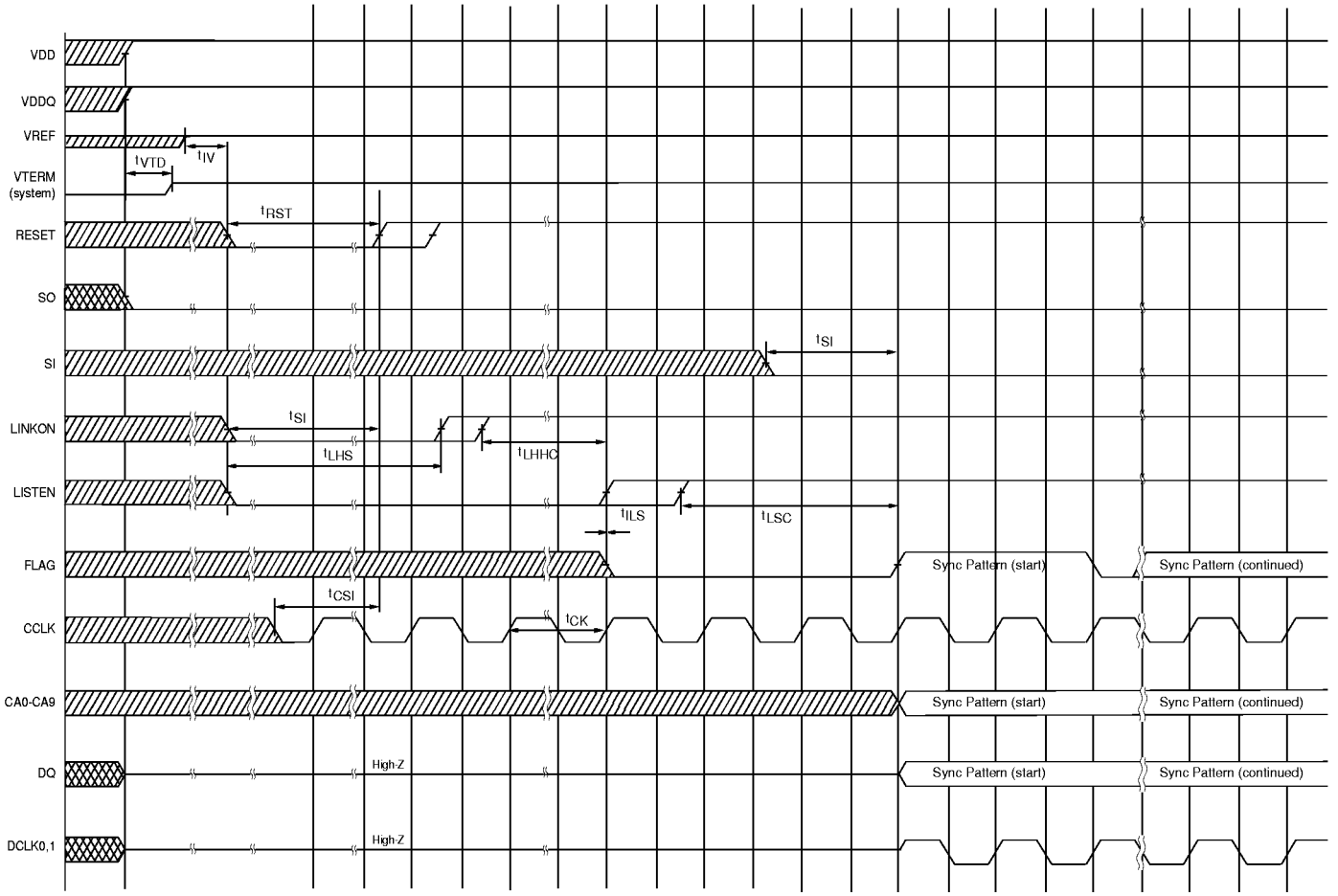


Notes:
1. The High-Z to Low-Z edge on the DQs (tLZ) is subject to the same skew requirements as other DQ transitions relative to the nominally coincident DCLK transition.

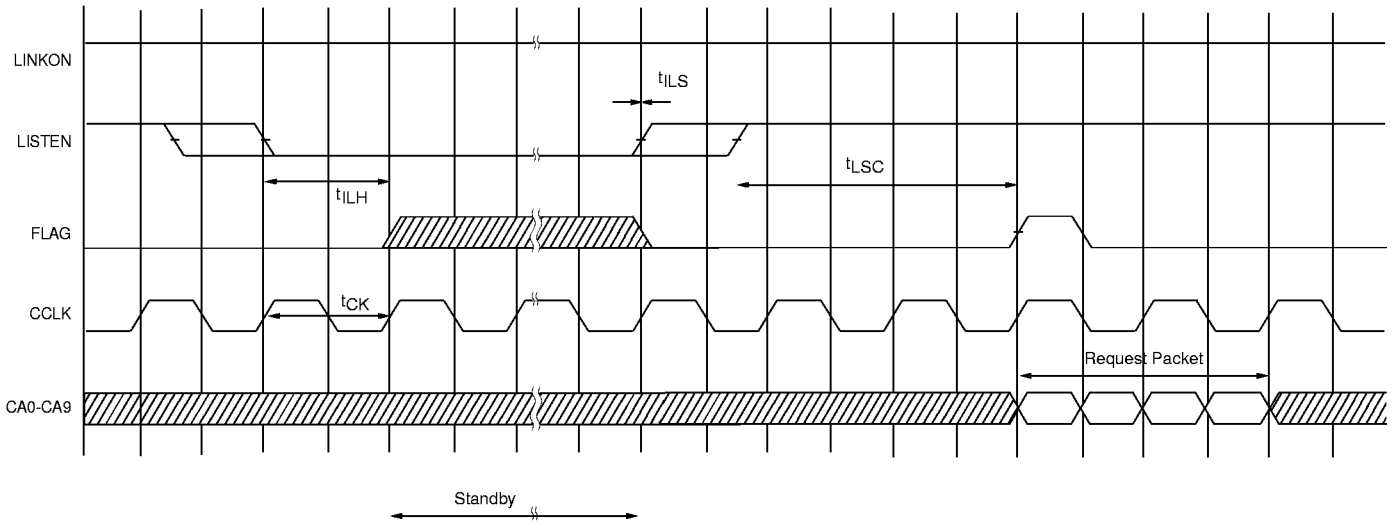
2. The tLZ and tHZ parameters values for the DCLK signals need not meet the same specification as for the DQs, but will be similar by design.

Figure 96
DATA OUTPUT ENABLE/DISABLE TIMING

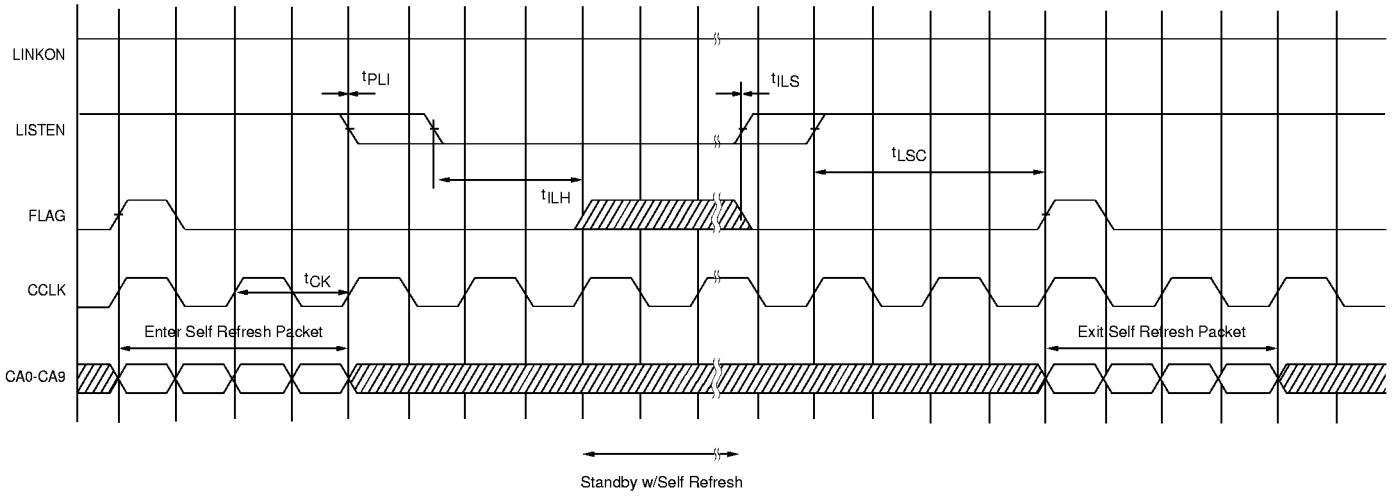
INITIALIZATION TIMING



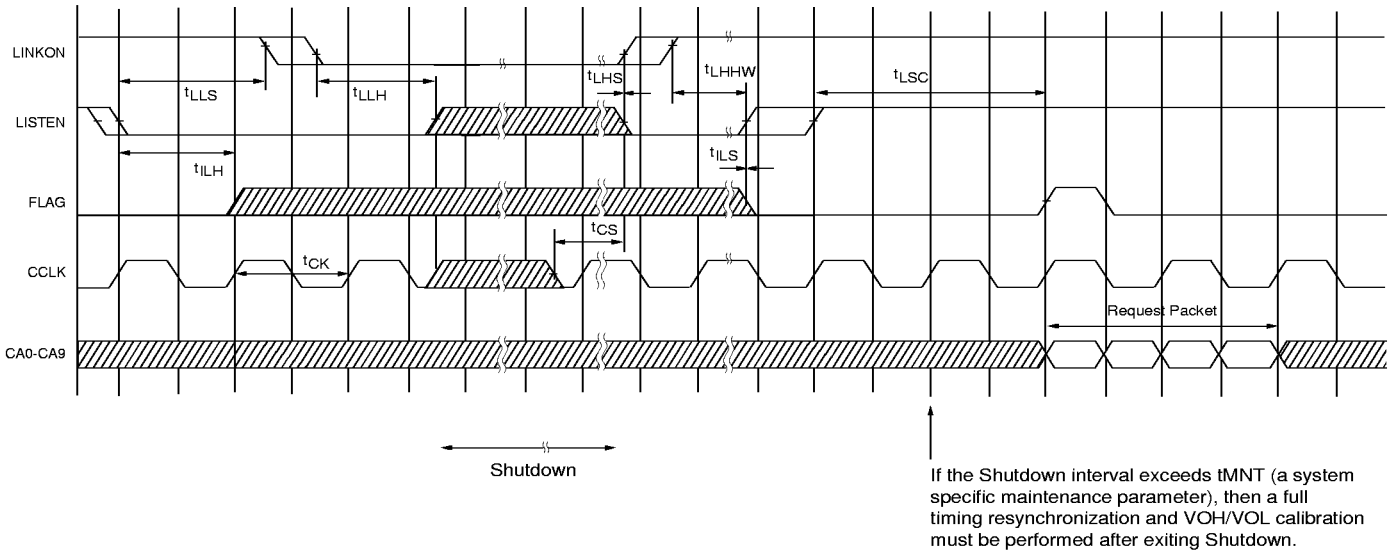
STANDBY MODE TIMING



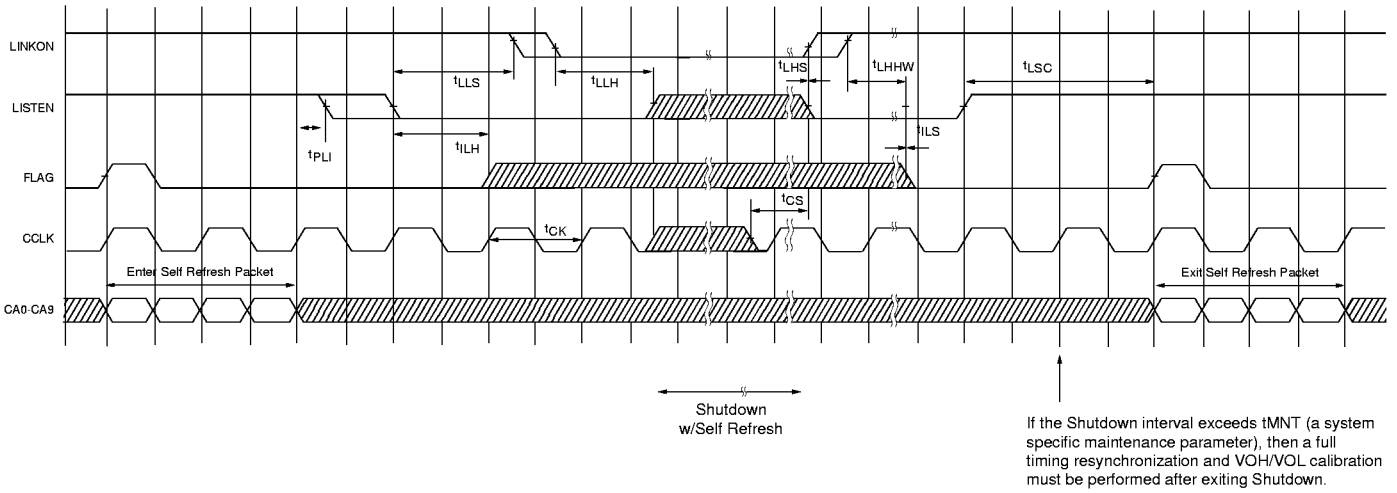
STANDBY WITH SELF REFRESH MODE TIMING



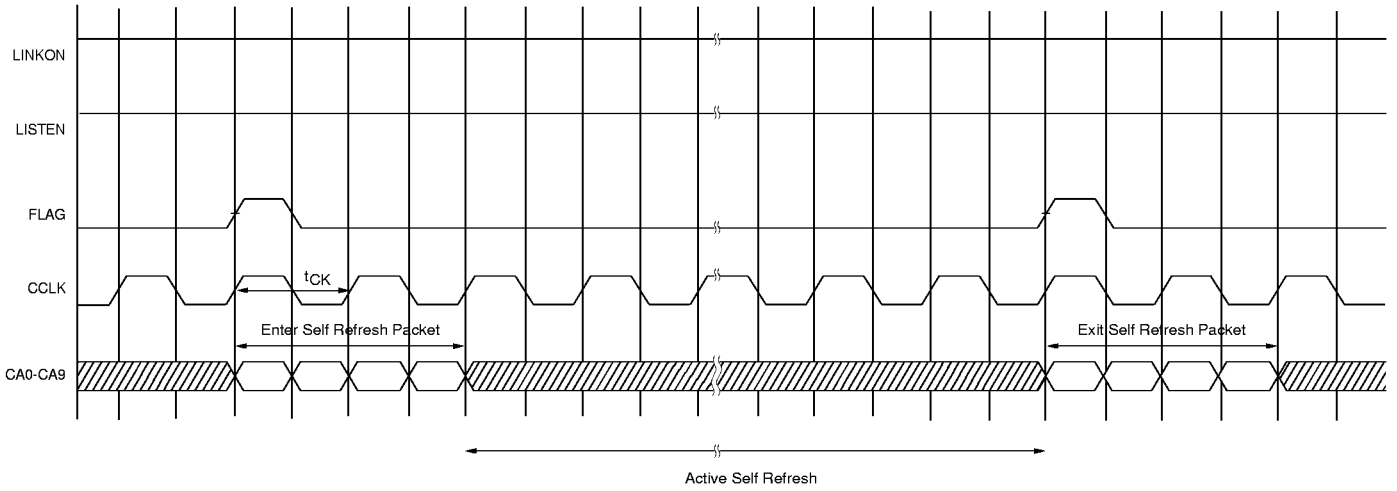
SHUTDOWN MODE TIMING



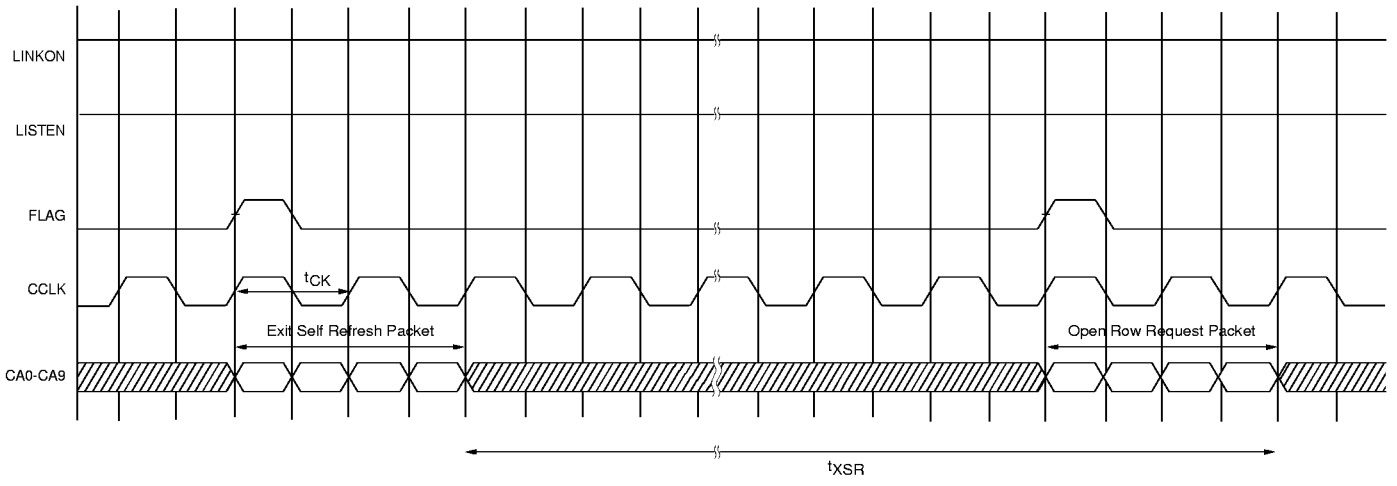
SHUTDOWN WITH SELF REFRESH MODE TIMING



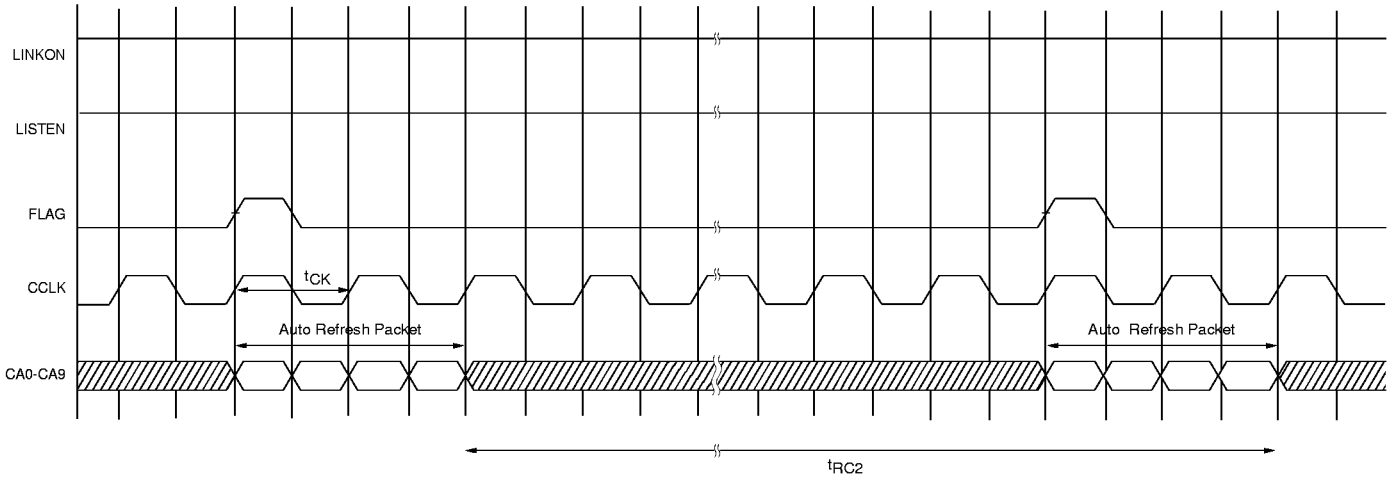
SELF REFRESH MODE TIMING



EXIT SELF REFRESH MODE TIMING



AUTO REFRESH TIMING



Revision History

9/22/97 - Corrected skew and valid timing parameter values; moved timing parameter notes to appropriate location, and added reference to note 9; edited parameter symbols for write recovery to be consistent.