CY2909A
CY2911A

CMOS Micro Program Sequencers

Features

- **Fast**
  - **— CY2909A/11A has a 40-ns (min.) clock-to-output cycle time (commercial)**
  - **— CY2909/11 has a 40-ns (min.) clock-to-output cycle time (military)**
- **Low power**
  - **— I_{CC} (max.) = 70 mA (commercial)**
  - **— I_{CC} (max.) = 90 mA (military)**
- **V_{CC} margin**
  - **— 5V ±10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **Infinitely expandable in 4-bit increments**
- **Capable of withstanding >2001V static discharge voltage**
- **Pin compatible and functional equivalent to AMD AM2909A/AM2911A**

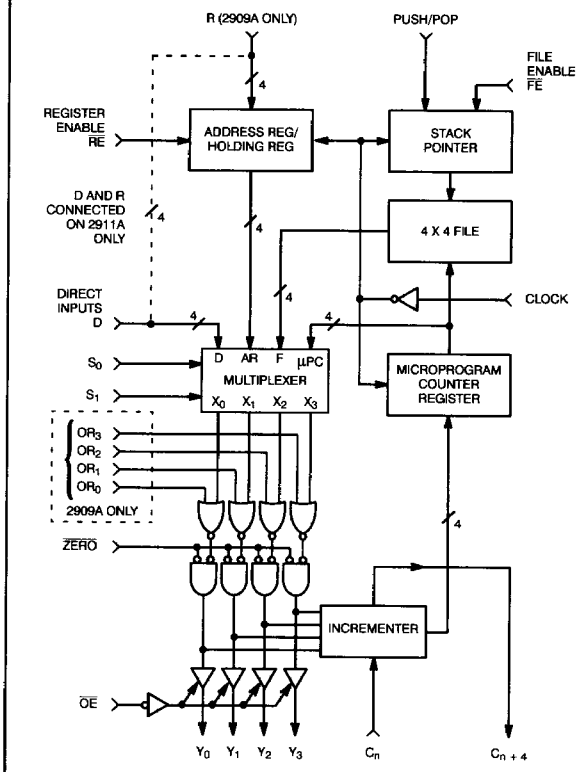
Functional Description

The CY2909A and CY2911A are high-speed, four-bit-wide address sequencers intended to control the sequence of execution of micro-instructions contained in microprogram memory. They may be connected in parallel to expand the address width in 4-bit increments. Both devices are implemented in high-performance CMOS for optimum speed and power.

The CY2909A can select an address from any of four sources. They are: (1) a set of four external direct inputs (D_i); (2) external data stored in an internal register (R_i); (3) a four-word-deep push/pop stack; or (4) a program counter register (which usually contains the last address plus one). The push/pop stack includes control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs (Y_i) can be ORed with an external input for conditional skip or branch instructions. A $\overline{ZERO}$ input line forces the outputs to all zeros. The outputs are tri-state, controlled by the output enable ($\overline{OE}$) input.

The CY2911A is an identical circuit to the CY2909A, except the four OR inputs are removed and the D and R inputs are tied together. The CY2911A is available in a 20-pin, 300-mil package. The CY2909A is available in a 28-pin, 600-mil package.

Logic Block Diagram



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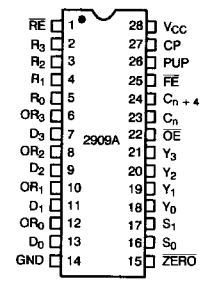
Pin Configurations



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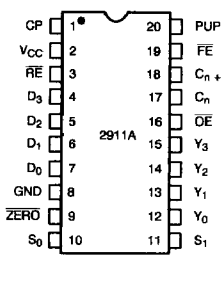
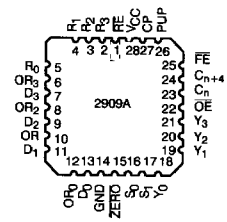


2909A–3



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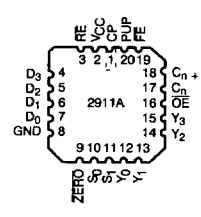

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current, into Outputs (LOW) ..... 30 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA	Commercial	2.4		V
		V_{CC} = Min., I_{OH} = – 1.0 mA	Military	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			– 2.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		– 20	+20	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		– 30	– 85	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		70	mA
			Military		90	

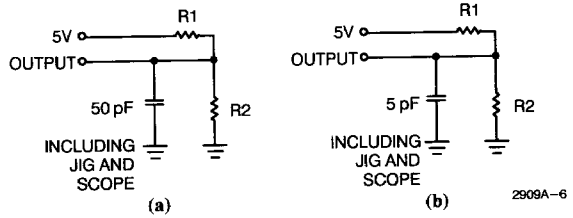
Capacitance[4]

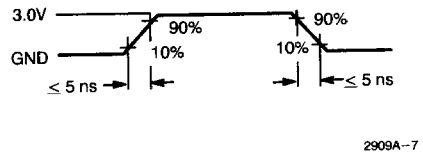
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





	Commercial	Military
R1	254Ω	258Ω
R2	187Ω	216Ω

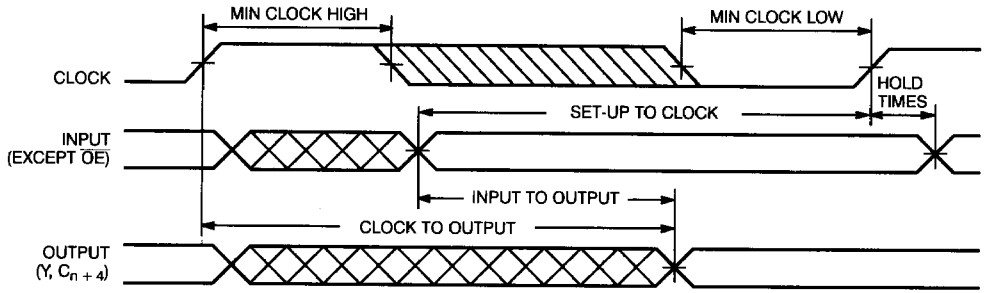
Switching Characteristics Over the Operating Range[2]

	Commercial		Military		Units
Minimum Clock LOW Time	20		20		ns
Minimum Clock HIGH Time	20		20		ns
MAXIMUM COMBINATORIAL PROPAGATION DELAYS					
From Input To:	Y	C_{n+4}	Y	C_{n+4}	ns
D_i	17	22	20	25	ns
S_0, S_1	29	34	29	34	ns
OR_i (CY2909A)	17	22	20	25	ns
C_n	—	14	—	16	ns
$\overline{ZERO}$	29	34	30	35	ns
$\overline{OE}$ LOW to Output	25	—	25	—	ns
$\overline{OE}$ HIGH to High Z[5]	25	—	25	—	ns
Clock HIGH, S_0, S_1 = LH	39	44	45	50	ns
Clock HIGH, S_0, S_1 = LL	39	44	45	50	ns
Clock HIGH, S_0, S_1 = HL	44	49	53	58	ns
MINIMUM SET-UP AND HOLD TIMES (All Times Relative to Clock LOW-to-HIGH Transition)					
From Input	**Set-Up**	**Hold**	**Set-Up**	**Hold**	
$\overline{RE}$	19	4	19	5	ns
R_i[6]	10	4	12	5	ns
Push/Pop	25	4	27	5	ns
$\overline{FE}$	25	4	27	5	ns
C_n	18	4	18	5	ns
D_i	25	0	25	0	ns
OR_i (CY2909A)	25	0	25	0	ns
S_0, S_1	25	0	29	0	ns
$\overline{ZERO}$	25	0	29	0	ns

Notes:

5. Output Loading as in part (b) of AC Test Loads and Waveforms.
6. R_i and D_i are internally connected on the CY2911A. Use R_i set-up and hold times for D_i inputs.

Switching Waveforms



Ordering Information

Ordering Code	Package Type	Operating Range
CY2909ADC	D16	Commercial
CY2909ALC	L64	
CY2909APC	P15	
CY2909ADMB	D16	Military
CY2909ALMB	L64	

Ordering Code	Package Type	Operating Range
CY2911ADC	D6	Commercial
CY2911ALC	L61	
CY2911APC	P5	
CY2911ADMB	D6	Military
CY2911ALMB	L61	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
Minimum Clock LOW Time	7, 8, 9, 10, 11
Minimum Clock HIGH Time	7, 8, 9, 10, 11
MAXIMUM COMBINATORIAL PROPAGATION DELAYS	
D_i to Y	7, 8, 9, 10, 11
D_i to C_{n+4}	7, 8, 9, 10, 11
S_0, S_1 to Y	7, 8, 9, 10, 11
S_0, S_1 to Cn_{+4}	7, 8, 9, 10, 11
OR_i (2909A) to Y	7, 8, 9, 10, 11
OR_i (2909A) to C_{n+4}	7, 8, 9, 10, 11
C_n to C_{n+4}	7, 8, 9, 10, 11
$\overline{ZERO}$ to C_{n+4}	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = LH to Y	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = LH to C_{n+4}	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = LL to Y	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = LL to C_{n+4}	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = HL to Y	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = HL to C_{n+4}	7, 8, 9, 10, 11

Parameters	Subgroups
MINIMUM SET-UP AND HOLD TIMES	
$\overline{RE}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{RE}$ Hold Time	7, 8, 9, 10, 11
Push/Pop Set-Up Time	7, 8, 9, 10, 11
Push/Pop Hold Time	7, 8, 9, 10, 11
$\overline{FE}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{FE}$ Hold Time	7, 8, 9, 10, 11
C_n Set-Up Time	7, 8, 9, 10, 11
C_n Hold Time	7, 8, 9, 10, 11
D_i Set-Up Time	7, 8, 9, 10, 11
D_i Hold Time	7, 8, 9, 10, 11
OR_i (2909A) Set-Up Time	7, 8, 9, 10, 11
OR_i (2909A) Hold Time	7, 8, 9, 10, 11
S_0, S_1 Set-Up Time	7, 8, 9, 10, 11
S_0, S_1 Hold Time	7, 8, 9, 10, 11
$\overline{ZERO}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{ZERO}$ Hold Time	7, 8, 9, 10, 11

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