ML7C960A

VME Slave Controller

The ML7C960 is a VME slave controller, pin-compatible with the now-discontinued CY7C960. Together with the ML7C964 VME data path component, the ML7C960 provides a simple VME interface solution.

Feature Summary

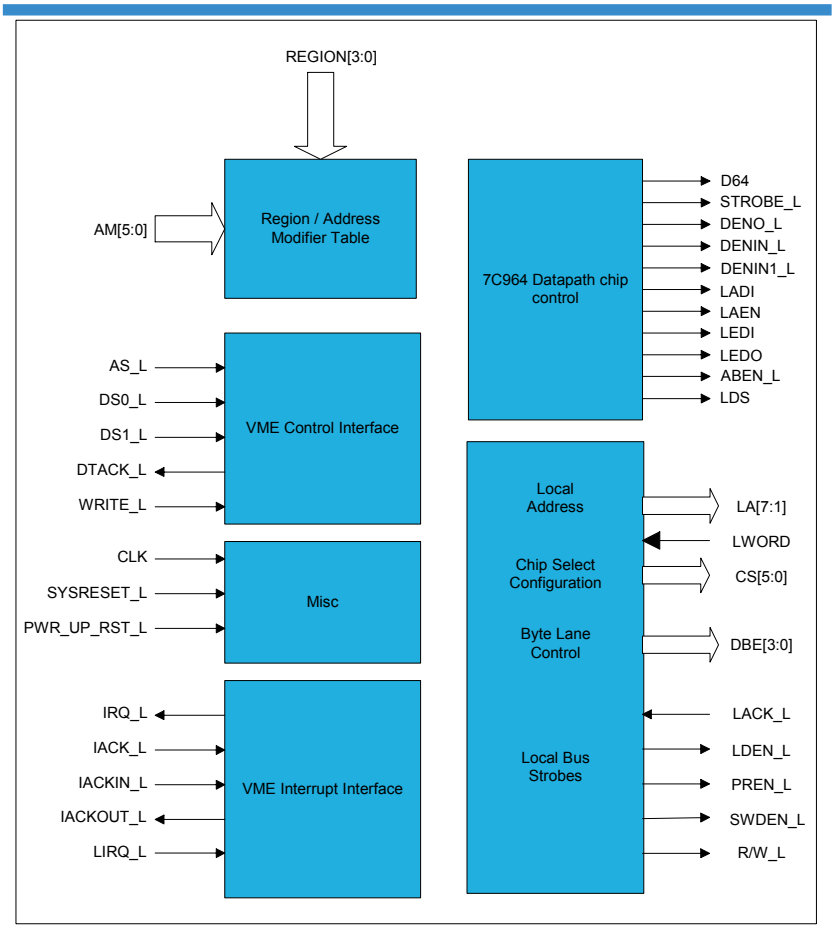
- Supports all standard (Rev. C) VMEbus transactions
- 80-Mbyte-per-second block transfer rates
- Supports VME64 transactions, including A64/D64, A40/MD32 transfers
- User-configured VMEbus response, configurable from serial PROM
- High-current drivers for direct connection to VME bus
- 64 pin PLCC package

Applications

VME64 has been widely used in industrial and military applications. The ML7C960 provides an integrated solution for VME and VME64 Slave devices.

The Millogic synthesizable core for the ML7C960 has been widely used to generate functional replacements for the Cypress CY7C960. The ML7C960 now provides a direct chip level replacement, requiring no printed circuit board changes.

Block Diagram



General Description

The ML7C960 provides control for the Cypress CY7C964 VME Datapath chips. Millogic also provides the ML7C964, a pin compatible replacement device for the CY7C964 chips. The ML7C960 together with the ML7C964 provide a complete VME slave interface solution.

The ML7C960 supports D8, D16, D32 (including UAT), MD32 and D64 data transfers. It can also support A16, A24, A32, A40, A64 addressing modes. Single-cycle and block-transfer reads and write cycles,Read-Modify-Write cycles (incl. multiplexed), and Address-only (with or without Handshake) cycles are all supported.

General Description

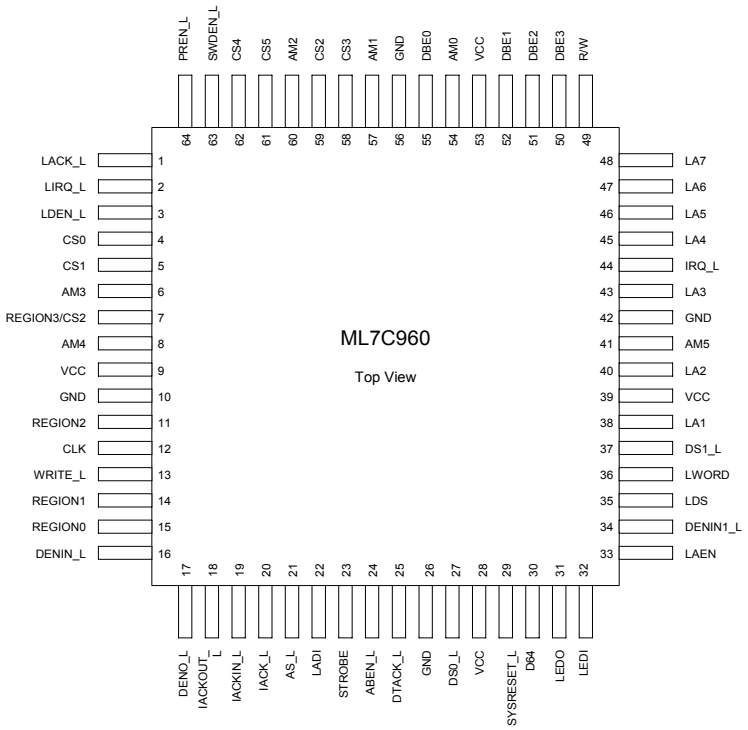
(continued)

The ML7C960 connects directly to the VME control signals, while the ML7C964 connects to the VME address and data signals. Together, they generate a local bus for connecting to the user logic. The local bus strobes are configurable to minimize on-board logic. Interrupts are supported with an integrated VMEbus Interrupter.

Similar to the CY7C960, the ML7C960 configures itself from a serial prom on power up. Configuration defines which VME cycles the device will respond to, the address and data widths, and how the Chip Selects will operate. The configuration also defines timing options.

The ML7C960 utilizes a free-running 80MHz clock to control internal operations. The ML7C960 handles VME timing automatically when using either the CY7C64 or ML7C964 VME data path chips.

Pin Configuration



Package - 64 pin PQFP

ML7C960—CY7C960 A Comparison

Some differences exist between the ML7C960 and the CY7C960.

- The ML7C960 does not support the DRAM control function of the CY7C960.
- The ML7C960 only supports master-serial mode for the configuration PROM.

Pin Description

Signal	Signal Direction	Description
REGION[3:0]	Input	VME address region
AM[5:0]	Input	VME address modifier
AS_L	Input	Address strobe
DS0_L	Input	Data strobe 0
DS1_L	Input	Data strobe 1
DTACK_L	Bidir	Data Acknowledge – Open Drain output
WRITE_L	Input	VME write input
LIRQ_L	Input	Local interrupt request
IRQ_L	Output	VME interrupt request – Open Drain output
IACK_L	Input	VME interrupt acknowledge
IACKIN_L	Input	Interrupt acknowledge input
IACKOUT_L	Output	Interrupt acknowledge output
D64	Output	ML7C964 interface - Informs external hardware D64 VME block transfer in progress
STROBE_L	Output	ML7C964 interface - Used during INIT to load 964 registers
DENO_L	Output	ML7C964 interface - Data Enable Out - Enables VME data drivers
DENIN_L	Output	ML7C964 interface - Data Enable In; used with DENIN1_L and SWDEN_L
DENIN1_L	Output	ML7C964 interface - Data Enable In; used with DENIN1_L and SWDEN_L
LADI	Bidir	ML7C964 interface - Latch Address In
LAEN	Bidir	ML7C964 interface - Local Address Enable
LEDI	Output	ML7C964 interface - Latch Enable Data In
LEDO	Output	ML7C964 interface - Latch Enable Data Out
ABEN_L	Output	ML7C964 interface - Address Bus Enable; enables data onto VME address bus for D64 cycles
LDS	Output	Local Data Select; used during muxed data VME transactions and INIT
LA[7:3]	Bidir	Local Address
LA2_PDATA	Bidir	Local Address(2); PROM data during INIT
LA1_PCLK	Bidir	Local Address(1); PROM clk during INIT
LA0_LWORD	Bidir	Local Address(0); LWORD_L from VME except during BLT
CS[5:0]	Output	Programmable Chip Select outputs
DBE[3:0]	Output	Data Byte Enables; programmable polarity
LACK_L	Input	Local Acknowledge/Local Bus Holdoff
LDEN_L	Output	Latch Data Enable; signals Interrupt Status/ID cycle in progress
PREN_L	Output	R/OE and CE for power-up configuration PROM
SWDEN_L	Output	Controls a local swap buffer
R_W_L	Output	Local READ/WRITE control; LOW for write
SYSRESET_L	Input	Asynchronous VME reset
CLK	Input	Freerunning 80MHz clock

Recommended Operating Conditions

Operating Conditions

Parameter	Description	Test Conditions	Value	Units
V_{CC}	Operating power supply		5 +/- 10%	V
T_J	Junction Temperature		-40—125	°C

DC Specifications—All Inputs

Parameter	Description	Test Conditions	Value	Units
V_{IH}	Minimum High-level Input Voltage		2.2	V
V_{IL}	Maximum Low-level Input Voltage		0.8	V
$I_{IH\text{-}max}$	Maximum High-level Input Current	V_{IN} = Vcc	10	µA
		V_{IN} = Vcc; 50K pulldown	250	µA
$I_{IH\text{-}min}$	Minimum High-level Input Current	V_{IN} = Vcc; 50K pulldown	20	µA
$I_{IL\text{-}max}$	Maximum Low-level Input Current	V_{IN} = GND	-10	µA
		V_{IN} = GND; 50K pullup	-250	µA
$I_{IL\text{-}min}$	Minimum Low-level Input Current	V_{IN} = GND; 50K pullup	-20	µA

DC Specifications—DTACK_L

Parameter	Description	Test Conditions	Value	Units
V_{OH}	Minimum High-level Output Voltage	Vcc = Min, I_{OH} = -3ma	2.4	V
V_{OL}	Maximum Low-level Output Voltage	Vcc = Min, I_{OH} = 48ma	0.6	V

DC Specifications—IRQ_L

Parameter	Description	Test Conditions	Value	Units
V_{OH}	Minimum High-level Output Voltage	N/A—Open Drain Output		
V_{OL}	Maximum Low-level Output Voltage	Vcc = Min, I_{OH} = 40ma	0.6	V

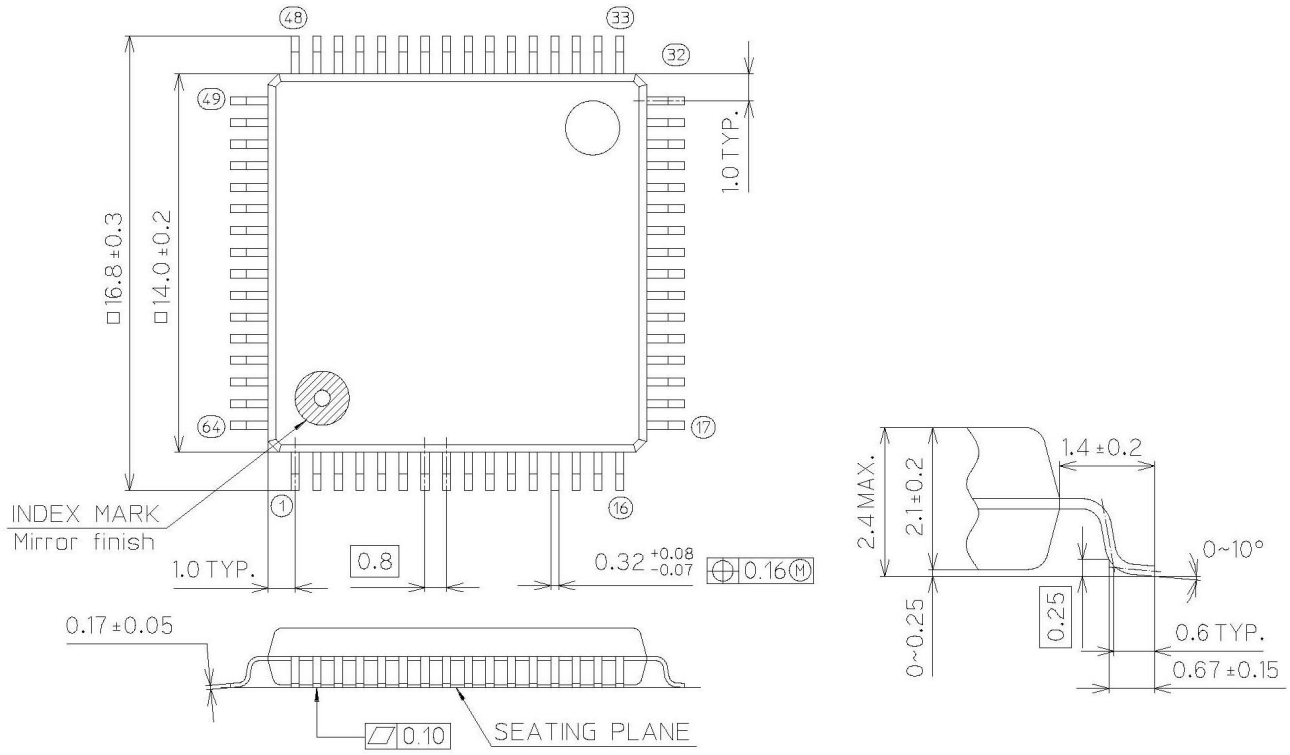
DC Specifications—All Other Outputs

Parameter	Description	Test Conditions	Value	Units
V_{OH}	Minimum High-level Output Voltage	Vcc = Min, I_{OH} = -12ma	2.8	V
V_{OL}	Maximum Low-level Output Voltage	Vcc = Min, I_{OH} = 12ma	0.4	V

DC Specifications—All Tristate Outputs—Leakage currents

Parameter	Description	Test Conditions	Value	Units
$I_{OZH\text{-}max}$	Max high-level leakage current	V_{IN} = Vcc	10	µA
		V_{IN} = Vcc; 50K pulldown	250	µA
$I_{OZH\text{-}min}$	Minimum pulldown current	V_{IN} = Vcc; 50K pulldown	20	µA
$I_{OZL\text{-}max}$	Max low-level leakage current	V_{IN} = GND	-10	µA
		V_{IN} = GND; 50K pullup	-250	µA
$I_{OZL\text{-}min}$	Minimum pullup current	V_{IN} = GND; 50K pullup	-20	µA

Package Outline



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