

Am29C323

CMOS 32-Bit Parallel Multiplier

PRELIMINARY

Am29C323

DISTINCTIVE CHARACTERISTICS

- **32-Bit Three-Bus Architecture**
 - The device has two 32-bit input ports and one 32-bit output port with clocked multiply time of 100 ns
- **Speed Selects**
 - 80- and 55-ns speed-select parts
- **Single Clock with Register Enables**
 - The Am29C323 is controlled by one clock with individual register enables
- **Supports Multiprecision Multiplication**
 - The device has dual 32-bit registers on each data input port to perform multiprecision multiplication
- **Registers can be made transparent**
 - Input and output registers can be made transparent independently to eliminate unwanted pipeline delay
- **Supports Two's Complement, Unsigned or Mixed Numbers**
- **Data Integrity Through Master-Slave Mode and Parity Check/Generate**
 - Parity check/generate catches inter-device connection errors and master/slave mode provides complete function check

GENERAL DESCRIPTION

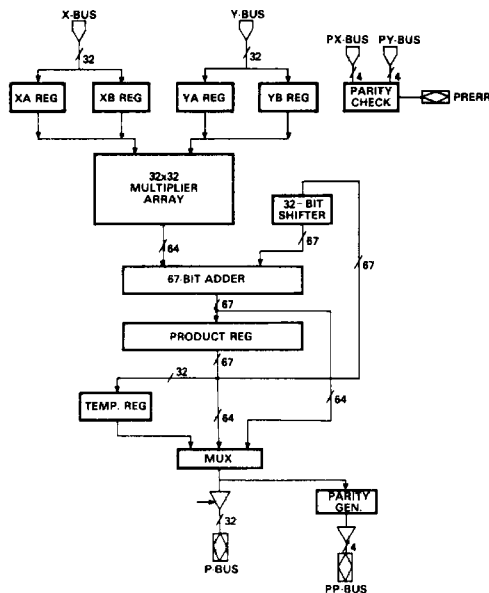
The Am29C323 is a high-speed 32 x 32-bit CMOS Parallel Multiplier with 67-Bit Accumulator. The part is designed to maximize system level performance by providing a 32-bit three bus architecture and a single clock with register enables.

The Am29C323 further enhances system throughput by providing individual register feedthrough controls, byte parity checking on both input ports and generation on the output port, and dual input registers on each data input bus to support multiprecision multiplication. The Am29C323 can manage a wide variety of data types, including two's

complement, unsigned, or mixed mode input formats. A 64 x 64-bit multiplication can be performed in seven clock cycles, including input and output. Additional features provided are a format adjust control allowing for standard output or left shifted output suitable for fractional two's complement arithmetic, rounding, and master/slave operation.

The Am29C323 is designed in low-power, high-speed CMOS with TTL-compatible I/O. The device is housed in a 169-lead pin-grid-array package.

SIMPLIFIED BLOCK DIAGRAM

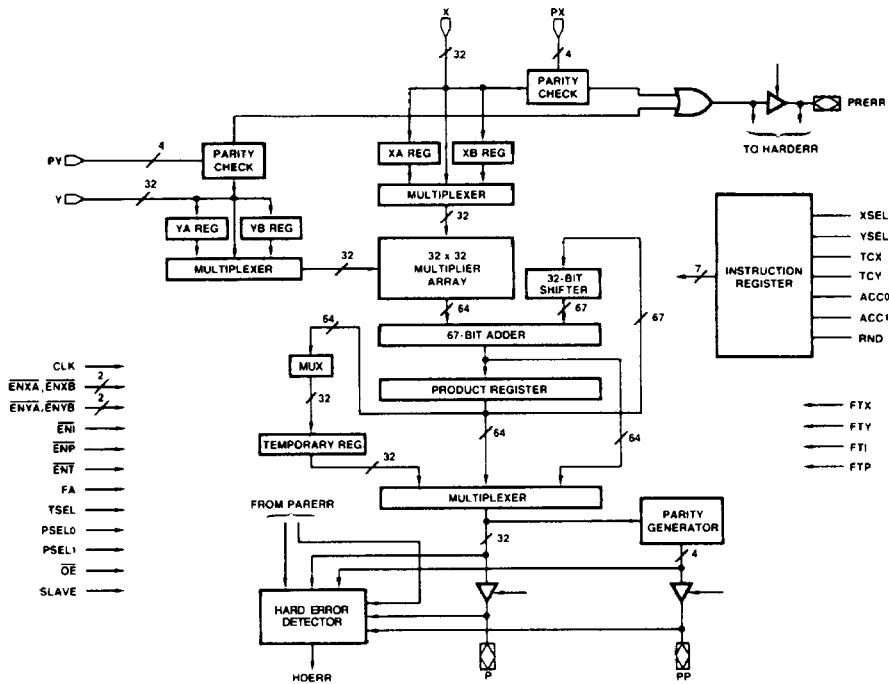


BD005255

RELATED AMD PRODUCTS

Part No.	Description
Am29C01	CMOS 4-Bit Microprocessor Slice
Am29C10A	CMOS 12-Bit Sequencer
Am29C101	CMOS 16-Bit Microprocessor
Am29112	8-Bit Cascadable Microprogram Sequencer
Am29114	Real-Time Interrupt Controller
Am29C116	CMOS 16-Bit Microcontroller
Am29325	32-Bit Floating Point Processor
Am29C325	CMOS 32-Bit Floating Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29C331	CMOS 16-Bit Microprogram Sequencer
Am29332	32-Bit Extended Function ALU
Am29C332	CMOS 32-Bit Extended Function ALU
Am29334	64 x 18 Four-Port Dual Access Register File
Am29C334	CMOS 64 x 18 Four-Port Dual Access Register File
Am29337	16-Bit Bounds Checker
Am29338	32-Bit Byte Queue
Am29C516	CMOS 16 x 16 Multiplier
Am29C517	CMOS 16 x 16 Multiplier with Separate I/O

DETAILED BLOCK DIAGRAM



BD003049

CONNECTION DIAGRAM
169-Lead PGA
Bottom View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	PY ₃	Y ₃₁	Y ₃₀	Y ₂₆	Y ₂₄	Y ₂₃	Y ₂₀	Y ₁₉	Y ₁₅	Y ₁₀	Y ₁₁	Y ₇	Y ₅	Y ₃	GND	$\overline{\text{ENYA}}$	PX ₃
2	GND	NC	Y ₂₉	Y ₂₇	PY ₂	Y ₂₁	Y ₁₈	Y ₁₆	PY ₁	Y ₁₂	Y ₀₉	PY ₀	Y ₄	Y ₂	Y ₀	$\overline{\text{ENVB}}$	X ₃₁
3	NC	PRERR	NC	Y ₂₈	Y ₂₅	Y ₂₂	V _{CC}	Y ₁₇	Y ₁₄	Y ₁₃	GND	Y ₈	Y ₆	Y ₁	FTY	X ₃₀	GND
4	V _{CC}	PP ₃	NC	*											X ₂₉	X ₂₈	X ₂₇
5	P ₃₀	P ₃₁	P ₂₉												X ₂₆	X ₂₄	X ₂₅
6	GND	P ₂₈	P ₂₇												PX ₂	X ₂₃	X ₂₂
7	P ₂₅	P ₂₆	GND												V _{CC}	X ₁₉	X ₂₁
8	V _{CC}	P ₂₄	PP ₂												X ₁₈	X ₁₇	X ₂₀
9	NC	NC	P ₂₃												X ₁₅	X ₁₆	PX ₁
10	GND	P ₂₂	P ₂₁												X ₁₄	X ₁₃	X ₁₁
11	P ₁₉	P ₂₀	V _{CC}												GND	X ₁₀	X ₁₂
12	P ₁₆	P ₁₈	P ₁₇												X ₉	X ₈	PX ₀
13	V _{CC}	HDERR	FTP												X ₇	X ₅	X ₆
14	NC	$\overline{\text{ENP}}$	NC												X ₂	X ₃	X ₄
15	$\overline{\text{ENT}}$	$\overline{\text{OE}}$	SLAVE	P ₁₅	P ₁₁	P ₁₂	GND	P ₇	P ₆	P ₃	V _{CC}	P ₁	FTI	TCY	FTX	X ₁	X ₀
16	PSEL1	FA	PP ₁	P ₁₄	P ₁₃	P ₉	GND	PP ₀	P ₅	P ₄	V _{CC}	$\overline{\text{ENI}}$	CLK	ACC1	TCX	$\overline{\text{ENXB}}$	$\overline{\text{ENXA}}$
17	PSEL0	TSEL	GND	NC	V _{CC}	P ₁₀	GND	P ₈	GND	P ₂	V _{CC}	P ₀	V _{CC}	RND	ACCO	YSEL	XSEL

CD011030

*Pinout observed from pin side of package.

**Pin 169 for reference only.

PIN DESIGNATIONS

(Sorted by Pin Number)

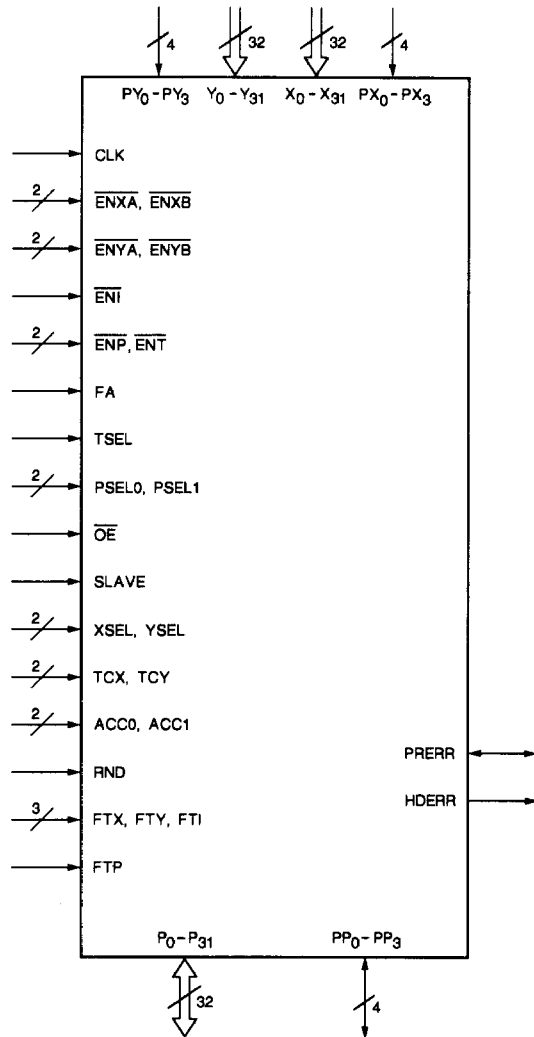
PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME
1	A1	PY ₃	75	C9	P ₂₃	55	J15	P ₆	117	R10	X ₁₄
168	A2	GND	72	C10	P ₂₁	51	J16	P ₅	116	R11	GND
83	A3	NC	74	C11	V _{CC}	135	J17	GND	36	R12	X ₉
81	A4	V _{CC}	153	C12	P ₁₇	14	K1	Y ₁₀	121	R13	X ₇
80	A5	P ₃₀	151	C13	FTP	13	K2	Y ₁₂	40	R14	X ₂
79	A6	GND	66	C14	NC	96	K3	Y ₁₃	125	R15	FTX
160	A7	P ₂₅	146	C15	SLAVE	50	K15	P ₃	128	R16	TCX
77	A8	V _{CC}	145	C16	PP ₁	134	K16	P ₄	45	R17	ACCO
157	A9	NC	61	C17	GND	133	K17	P ₂	105	T1	ENYA
71	A10	GND	4	D1	Y ₂₆	97	L1	Y ₁₁	21	T2	ENYB
154	A11	P ₁₉	87	D2	Y ₂₇	98	L2	Y ₉	107	T3	X ₃₀
69	A12	P ₁₆	3	D3	Y ₂₈	95	L3	GND	108	T4	X ₂₈
68	A13	V _{CC}	62	D15	P ₁₅	53	L15	V _{CC}	110	T5	X ₂₄
67	A14	NC	144	D16	P ₁₄	53	L16	V _{CC}	111	T6	X ₂₃
65	A15	ENT	60	D17	NC	53	L17	V _{CC}	113	T7	X ₁₉
148	A16	PSEL1	5	E1	Y ₂₄	16	M1	Y ₇	114	T8	X ₁₇
64	A17	PSEL0	89	E2	PY ₂	99	M2	PY ₀	31	T9	X ₁₆
85	B1	Y ₃₁	88	E3	Y ₂₅	15	M3	Y ₈	34	T10	X ₁₃
84	B2	NC	142	E15	P ₁₁	132	M15	P ₁	119	T11	X ₁₀
166	B3	PRERR	143	E16	P ₁₃	47	M16	ENI	120	T12	X ₈
165	B4	PP ₃	57	E17	V _{CC}	48	M17	P ₀	122	T13	X ₅
164	B5	P ₃₁	6	F1	Y ₂₃	17	N1	Y ₅	123	T14	X ₃
162	B6	P ₂₈	7	F2	Y ₂₁	101	N2	Y ₄	124	T15	X ₁
161	B7	P ₂₆	90	F3	Y ₂₂	100	N3	Y ₆	42	T16	ENXB
76	B8	P ₂₄	59	F15	P ₁₂	130	N15	FTI	127	T17	YSEL
73	B9	NC	141	F16	P ₉	131	N16	CLK	22	U1	PX ₃
156	B10	P ₂₂	58	F17	P ₁₀	49	N17	V _{CC}	106	U2	X ₃₁
155	B11	P ₂₀	91	G1	Y ₂₀	18	P1	Y ₃	23	U3	GND
70	B12	P ₁₈	92	G2	Y ₁₈	102	P2	Y ₂	25	U4	X ₂₇
152	B13	HDERR	11	G3	V _{CC}	19	P3	Y ₁	26	U5	X ₂₅
150	B14	ENP	137	G15	GND	44	P15	TCY	28	U6	X ₂₂
149	B15	OE	137	G16	GND	129	P16	ACC1	112	U7	X ₂₁
63	B16	FA	137	G17	GND	46	P17	RND	29	U8	X ₂₀
147	B17	TSEL	8	H1	Y ₁₉	20	R1	GND	115	U9	PX ₁
2	C1	Y ₃₀	93	H2	Y ₁₆	103	R2	Y ₀	35	U10	X ₁₁
86	C2	Y ₂₉	9	H3	Y ₁₇	104	R3	FTY	118	U11	X ₁₂
167	C3	NC	139	H15	P ₇	24	R4	X ₂₉	37	U12	PX ₀
82	C4	NC	56	H16	PP ₀	109	R5	X ₂₆	38	U13	X ₆
163	C5	P ₂₉	140	H17	P ₈	27	R6	PX ₂	39	U14	X ₄
78	C6	P ₂₇	94	J1	Y ₁₅	32	R7	V _{CC}	41	U15	X ₀
158	C7	GND	10	J2	PY ₁	30	R8	X ₁₈	126	U16	ENXA
159	C8	PP ₂	12	J3	Y ₁₄	33	R9	X ₁₅	43	U17	XSEL

PIN DESIGNATIONS

(Sorted by Pin Name)

PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME
45	R17	ACC0	50	K15	P ₃	89	E2	PY ₂	110	T5	X ₂₄
129	P16	ACC1	134	K16	P ₄	1	A1	PY ₃	26	U5	X ₂₅
131	N16	CLK	51	J16	P ₅	46	P17	RND	109	R5	X ₂₆
47	M16	ENI	55	J15	P ₆	146	C15	SLAVE	25	U4	X ₂₇
150	B14	ENP	139	H15	P ₇	128	R16	TCX	108	T4	X ₂₈
65	A15	ENT	140	H17	P ₈	44	P15	TCY	24	R4	X ₂₉
126	U16	ENX _A	141	F16	P ₉	147	B17	TSEL	107	T3	X ₃₀
42	T16	ENX _B	58	F17	P ₁₀	68	A13	VCC	106	U2	X ₃₁
105	T1	ENY _A	142	E15	P ₁₁	81	A4	VCC	43	U17	XSEL
21	T2	ENY _B	59	F15	P ₁₂	77	A8	VCC	103	R2	Y ₀
63	B16	FA	143	E16	P ₁₃	74	C11	VCC	19	P3	Y ₁
130	N15	FTI	144	D16	P ₁₄	57	E17	VCC	102	P2	Y ₂
151	C13	FTP	62	D15	P ₁₅	11	G3	VCC	18	P1	Y ₃
125	R15	FTX	69	A12	P ₁₆	53	L15	VCC	101	N2	Y ₄
104	R3	FTY	153	C12	P ₁₇	53	L16	VCC	17	N1	Y ₅
71	A10	GND	70	B12	P ₁₈	53	L17	VCC	100	N3	Y ₆
168	A2	GND	154	A11	P ₁₉	49	N17	VCC	16	M1	Y ₇
79	A6	GND	155	B11	P ₂₀	32	R7	VCC	15	M3	Y ₈
61	C17	GND	72	C10	P ₂₁	41	U15	X ₀	98	L2	Y ₉
158	C7	GND	156	B10	P ₂₂	124	T15	X ₁	14	K1	Y ₁₀
137	G15	GND	75	C9	P ₂₃	40	R14	X ₂	97	L1	Y ₁₁
137	G16	GND	76	B8	P ₂₄	123	T14	X ₃	13	K2	Y ₁₂
137	G17	GND	160	A7	P ₂₅	39	U14	X ₄	96	K3	Y ₁₃
135	J17	GND	161	B7	P ₂₆	122	T13	X ₅	12	J3	Y ₁₄
95	L3	GND	78	C6	P ₂₇	38	U13	X ₆	94	J1	Y ₁₅
20	R1	GND	162	B6	P ₂₈	121	R13	X ₇	93	H2	Y ₁₆
116	R11	GND	163	C5	P ₂₉	120	T12	X ₈	9	H3	Y ₁₇
23	U3	GND	80	A5	P ₃₀	36	R12	X ₉	92	G2	Y ₁₈
152	B13	HDERR	164	B5	P ₃₁	119	T11	X ₁₀	8	H1	Y ₁₉
157	A9	NC	166	B3	PRERR	35	U10	X ₁₁	91	G1	Y ₂₀
60	D17	NC	56	H16	PP ₀	118	U11	X ₁₂	7	F2	Y ₂₁
73	B9	NC	145	C16	PP ₁	34	T10	X ₁₃	90	F3	Y ₂₂
82	C4	NC	159	C8	PP ₂	117	R10	X ₁₄	6	F1	Y ₂₃
83	A3	NC	165	B4	PP ₃	33	R9	X ₁₅	5	E1	Y ₂₄
84	B2	NC	64	A17	PSEL0	31	T9	X ₁₆	88	E3	Y ₂₅
66	C14	NC	148	A16	PSEL1	114	T8	X ₁₇	4	D1	Y ₂₆
167	C3	NC	37	U12	PX ₀	30	R8	X ₁₈	87	D2	Y ₂₇
67	A14	NC	115	U9	PX ₁	113	T7	X ₁₉	3	D3	Y ₂₈
149	B15	OE	27	R6	PX ₂	29	U8	X ₂₀	86	C2	Y ₂₉
48	M17	P ₀	22	U1	PX ₃	112	U7	X ₂₁	2	C1	Y ₃₀
132	M15	P ₁	99	M2	PY ₀	28	U6	X ₂₂	85	B1	Y ₃₁
133	K17	P ₂	10	J2	PY ₁	111	T6	X ₂₃	127	T17	YSEL

LOGIC SYMBOL



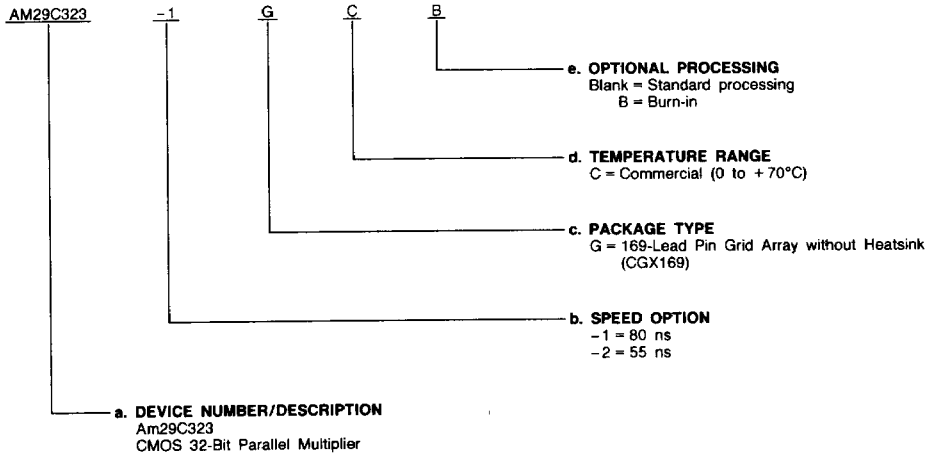
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

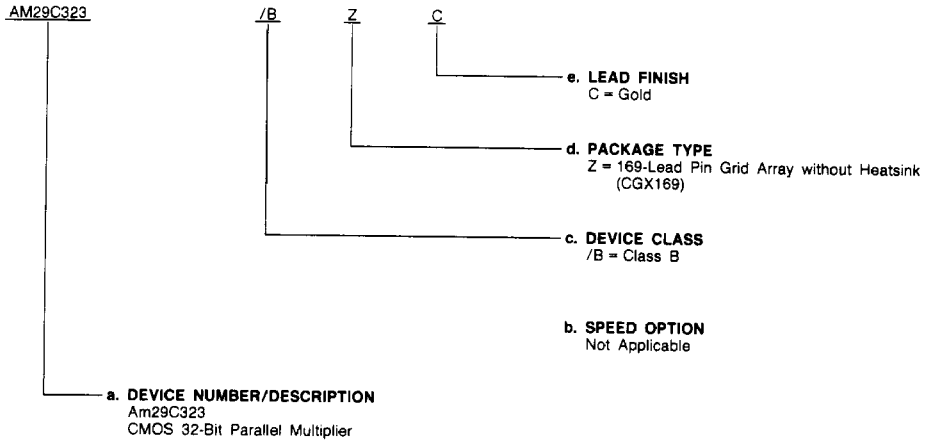
Valid Combinations	
AM29C323	GC, GCB
AM29C323-1	
AM29C323-2	

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM29C323	/BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

ACC0, ACC1 Accumulator Control (Input)

Accumulator control lines used to determine accumulator function; PASS, ACCUMULATE, and SHIFT and ACCUMULATE.

CLK Clock (Input)

Clock input for all registers.

ENI Instruction Register Enable (Input; Active LOW)

Register enable for instruction register I.

ENP Accumulator Register Enable (Input; Active LOW)

Register enable for product register P.

ENT Temporary Register Enable (Input; Active LOW)

Register enable for temporary register T.

ENXA, ENXB Multiplicand Register Enable (Input; Active LOW)

Register enables for multiplicand data input registers XA and XB.

ENYA, ENYB Multiplier Register Enable (Input; Active LOW)

Register enables for multiplier data input registers YA and YB.

FA Format Adjust (Input)

Format adjust selects either a full 64-bit product (HIGH) or a left shifted 63-bit product suitable for fractional two's complement arithmetic (LOW).

FTP Feedthrough Control (Input; Active HIGH)

Feedthrough control for product register.

FTX, FTY, FTI Feedthrough Control (Input; Active HIGH)

Feedthrough control lines for X, Y, and I registers.

HDERR Hard Error Flag (Output)

Used when two Am29C323s are configured as master and slave to indicate hardware errors.

OE Output Enable Control (Input; Active LOW)

Used to enable (LOW) or disable (HIGH) the P output port.

P0 - P31 Product Output (Input/Output; Three State)

Product output for P port.

PRRER Parity Error Flag (Input/Output; Three State)

Indicates a parity error on the input buses.

PP0 - PP3 Byte Parity (Input/Output; Three State)

Byte parity generated on P output port (even parity).

PSEL0, PSEL1 Product Control (Input)

Used to select desired output including disabling P and PP output ports.

PX0 - PX3 Byte Parity (Input)

Byte parity inputs on X input port (even parity).

PY0 - PY3 Byte Parity (Input)

Byte parity inputs on Y input port (even parity).

RND Round Control (Input; Active HIGH)

Round control for rounding the most significant product.

SLAVE Master/Slave Control (Input)

Used to determine mode of operation.

TCX, TCY Mode Control (Input)

Mode control inputs for each input data word; LOW for unsigned data and HIGH for two's complement format.

TSEL Select Control (Input)

Used to route the most significant product register (HIGH) or the least significant product register (LOW) into the temporary register.

X0 - X31 Multiplicand Data (Input)

Multiplicand data input for X port.

XSEL X Register Select (Input)

Control line used to route the contents of either the XA register (HIGH) or XB register (LOW) into the multiplier array.

Y0 - Y31 Multiplier Data (Input)

Multiplier data input for Y port.

YSEL Y Register Select (Input)

Control line used to route the contents of either the YA register (HIGH) or YB register (LOW) into the multiplier array.

FUNCTIONAL DESCRIPTION

Architecture

The Am29C323 comprises a high speed 32 by 32-bit multiplier array, a 67-bit accumulator, and a 32-bit data path.

Multiplier Array

The multiplier is a 32 by 32-bit array that produces a 64-bit product. This product is then fed to the accumulator section.

Accumulator

The accumulator is 67 bits wide. It performs accumulation for sum of product operations and multiprecision multiplication operations. The accumulator can perform three operations: store product without accumulation, accumulate product, and shift accumulator value and accumulate with product.

The shift and accumulate shifts the value in the product register 32 bits to the right (effectively moving the most significant 32 bits to the least significant 32 bits) and sign extends to a full 64 bits. This shifted value is then accumulated with the output of the multiplier array.

The 67-bit width is necessary to contain overflows in internal accumulations. These overflows are maintained and used when the product register is right shifted in the multiprecision multiplies. The lower 64 bits contain the 64-bit output while the upper 3 bits contain the overflow.

Data Path

The 32-bit data path consists of X and Y input buses; the P output bus; data registers XA, XB, YA, YB, and the product accumulator; two multiplier input multiplexers; byte parity input checkers; byte parity output generators; and master/slave comparators. Input operands enter the device through the two 32-bit input buses, X₀ - X₃₁ and Y₀ - Y₃₁. These operands may then be stored in one of the two registers for each bus (XA or XB for X, YA or YB for Y) or they may be fed directly through to the multiplier array. Input parity checking is performed as soon as the operands are put on the input buses. The signals used for output parity generation are taken from the input side of the output translator. In case of parity error, PRRER is enabled HIGH.

Operational Modes

The Am29C323 can perform signed, unsigned, or mixed mode multiplication. These different numerical representations are controlled by TCX and TCY. A HIGH input on one of these lines indicates to the device that the respective input should be treated as a two's complement number; a LOW, an unsigned number. The output format is unsigned when both inputs are unsigned. The output format is two's complement when either or both inputs are two's complement.

Slave Mode

Each output has an associated comparator which compares the signal on the output pin with the signal provided to the output driver. If any of these outputs do not agree, the HDERR is asserted. When not in slave mode, this enables the multiplier to check for contention and bus shorts. However, when in slave mode, one multiplier can be used to detect faults in both internal functions and interconnections of the other multiplier. This is accomplished through the master/slave configuration, where the two multipliers operate in parallel. One multiplier is the master and operates normally; the other operates in slave mode.

In slave mode all outputs are turned into inputs from the master, except for the HDERR signal. Since the slave is operated in parallel with the master, it can compare the results it generates to those of the master and signal an error if they differ.

Command Description and Formats

The accumulator is controlled by ACC0 and ACC1. These lines are used to select any of the three operations that the accumulator can perform. This instruction set is described in Table 1.

The temporary output register is controlled by TSEL and FA. These lines are used to select any of the four different sets of data that can be stored in the temporary register. This instruction set is described in Table 2.

The output multiplexer is controlled by PSEL0, PSEL1, and FA. These lines are used to select any of the five different sets of data that can be output through the P port. PSEL0 and PSEL1 can also be used to disable the outputs. (This instruction is independent of OE.) This instruction set is described in Table 3.

Format Adjust (FA) is used to select either a full 64-bit product or a left-shifted 63-bit product suitable for fractional two's complement arithmetic. This shifting increases the precision of the upper half of the product word by eliminating the redundant sign bit. Output Data Formats show the effect of FA.

Round (RND) is used to round the upper 32 bits of the 64-bit product. If only the upper 32 bits of the product are being used, then the lower 32 bits are truncated when rounding is not used (RND = 0). If rounding is used (RND = 1), then a "1" is added to the most significant of the lower 32 bits. This

results in a smaller possible error. This should only be used when the lower 32 bits are to be truncated.

User Visible Register Descriptions

The Am29C323 contains seven different register sets, each with its own clock enable. Two 32-bit registers are attached to each of the input data buses. These registers are differentiated by the suffix A or B. For example, the X bus has registers XA and XB. The 67-bit accumulator register can be used as a regular product register when the part is used as a multiplier only or as the register part of the accumulator section. The 32-bit temporary output register is included to aid in the pipelining of multiprecision operations. An instruction register is also provided.

All of these registers can be made transparent with the exception of the accumulator register and the temporary register. The product from the multiplier can be fed directly to the output by using the FTP control line.

TABLE 1. ACCUMULATOR OPERATION INSTRUCTIONS

ACC1	ACC0	Accumulator Operation
0	0	PASS
0	1	ACCUMULATE
1	0	INVALID
1	1	SHIFT AND ACCUMULATE

TABLE 2. INPUT SELECT INSTRUCTIONS FOR TEMPORARY (T) REGISTER

TSEL	FA	Temp Reg Input
0	0	P_{i-1}
0	1	P_i
1	0	P_{i+31}
1	1	P_{i+32}

TABLE 3. OUTPUT SELECT INSTRUCTIONS FOR PRODUCT (P) PORT

PSEL1	PSEL0	FA	P Port Output
0	0	X	TEMP REGISTER
0	1	0	P_{i-1}
0	1	1	P_i
1	0	0	P_{i+31}
1	0	1	P_{i+32}
1	1	X	DISABLE

Am29C323 X AND Y INPUT DATA FORMATS

Fractional Two's Complement

TCX, TCY = 1

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}						2^{-28}	2^{-29}	2^{-30}	2^{-31}

Integer Two's Complement

TCX, TCY = 1

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

Unsigned Fractional

TCX, TCY = 0

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}						2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer

TCX, TCY = 0

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

Am29C323 P-PORT OUTPUT DATA FORMATS

Fractional Two's Complement (Shifted)*

FA = 0, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}						2^{-28}	2^{-29}	2^{-30}	2^{-31}

FA = 0, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
2^{-32}	2^{-33}	2^{-34}	2^{-35}	2^{-36}	2^{-37}						2^{-60}	2^{-61}	2^{-62}	2^{-63}^{**}

Fractional Two's Complement

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
-2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}						2^{-27}	2^{-28}	2^{-29}	2^{-30}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
2^{-31}	2^{-32}	2^{-33}	2^{-34}	2^{-35}	2^{-36}						2^{-59}	2^{-60}	2^{-61}	2^{-62}

Integer Two's Complement

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
-2^{63}	2^{62}	2^{61}	2^{60}	2^{59}	2^{58}						2^{35}	2^{34}	2^{33}	2^{32}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

Unsigned Fractional

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}						2^{-29}	2^{-30}	2^{-31}	2^{-32}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
2^{-33}	2^{-34}	2^{-35}	2^{-36}	2^{-37}	2^{-38}						2^{-61}	2^{-62}	2^{-63}	2^{-64}

Unsigned Integer

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
2^{63}	2^{62}	2^{61}	2^{60}	2^{59}	2^{58}						2^{35}	2^{34}	2^{33}	2^{32}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	-	-	-	-	-	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

*In this format, an overflow occurs in the attempted multiplication of the two's complement number -1.000 with itself, yielding a product of $+1.000$ which cannot be represented in this format. **This bit position (2^{-63}) equals zero in this format.

64 x 64 Multiplication

To perform a 64 x 64-bit multiplication using the Am29C323, each 64-bit input must be split into two 32-bit inputs; a most significant half and a least significant half (XW1 and XW0 or YW1 and YW0, respectively). These 32-bit inputs are then used to perform the four multiplications needed to obtain the 128-bit product. This product is represented in four 32-bit words, PW₃ - PW₀, the least significant word being PW₀. The product is output 32 bits at a time through the product (P) port. The following equation shows the required multiplications:

$$X \cdot Y = ((XW1 \cdot YW1) \cdot 2^{64}) + ((XW0 \cdot YW1) \cdot 2^{32}) + ((XW1 \cdot YW0) \cdot 2^{32}) + ((XW0 \cdot YW0) \cdot 2^0)$$

$$P = (PW3 \cdot 2^{96}) + (PW2 \cdot 2^{64}) + (PW1 \cdot 2^{32}) + (PW0 \cdot 2^0)$$

The Am29C323 uses an internal accumulator to sum these intermediate products. The previous equation, in a slightly

different form, is shown with the necessary instructions below:

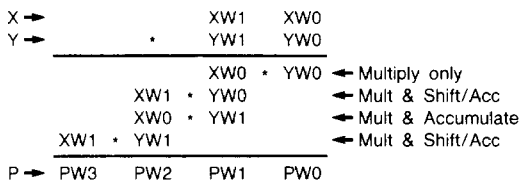


Table 4 details the movement of the input operands through the Am29C323. Table 5 defines the microcode required to perform a signed 64 x 64-bit multiplication. For an unsigned multiplication, TCX and TCY are LOW for all cycles. The operations and data movement are scheduled to produce a single product in seven clock cycles or a new pipelined product every four clock cycles.

TABLE 4. BUS AND REGISTER CONTENTS FOR A 64 x 64-BIT SIGNED MULTIPLICATION WITH ONE COMPLETE EXTENDED MULTIPLICATION SHOWN IN THE UNSHADED CYCLES

Cycle	0	1	2	3	4	5	6
X BUS	XW0	XW1			XW0	XW0	XW0
XA REG	XW0	XW0	XW0	XW0	XW0	XW0	XW0
XB REG	XW1	XW1	XW1	XW1	XW1	XW1	XW1
Y BUS	YW0	YW1			YW0	YW1	
YA REG	YW0	YW0	YW0	YW0	YW0	YW0	YW0
YB REG	YW1	YW1	YW1	YW1	YW1	YW1	YW1
MPY OP	XW1·YW1	XW0·YW0	XW1·YW0	XW0·YW1	XW1·YW1	XW0·YW0	XW1·YW0
ACC OP	S/A	PASS	S/A	ACC	S/A	PASS	S/A
T REG		PW3	PW0			PW3	
P BUS	PW1	PW2	PW3	PW0	PW1	PW2	PW3

Note: MPY OP = Operation of multiplier array (X·Y)
 ACC OP = Operation of internal accumulator
 PASS = Pass through multiplier product
 ACC = Add previous result to current product
 S/A = Shift previous result then add to current product

TABLE 5. INSTRUCTION MICROCODE FOR 64 x 64-BIT SIGNED MULTIPLICATION WITH ONE COMPLETE EXTENDED MULTIPLICATION SHOWN IN THE UNSHADED CYCLES

Cycle	0	1	2	3	4	5	6	7	8	9	A	B	C	D
ENXA	0	1	1	1	0	1	1	1	0	1	1	1	0	1
ENXB	1	0	1	1	1	0	1	1	1	0	1	1	1	0
TCX	0	1	0	1	0	1	0	1	0	1	0	1	0	1
XSEL	1	0	1	0	1	0	1	0	1	0	1	0	1	0
ENYA	0	1	1	1	0	1	1	1	0	1	1	1	0	1
ENYB	1	0	1	1	1	0	1	1	1	0	1	1	1	0
TCY	0	0	1	1	0	0	1	1	0	0	1	1	0	0
YSEL	1	1	0	0	1	1	0	0	1	1	0	0	1	1
ENI	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ENT	1	0	0	1	1	0	0	1	1	0	0	1	1	0
TSEL	X	1	0	X	X	1	0	X	X	1	0	X	X	1
ACC0	0	1	1	1	0	1	1	1	0	1	1	1	0	1
ACC1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
ENP	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PSEL0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
PSEL1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient Temperature Under Bias	-55 to +125°C
Supply Voltage to Ground Potential	
Continuous	-0.3 to +7.0 V
DC Voltage Applied to Outputs For	
High Output State	-0.3 to +V _{CC} + 0.3 V
DC Input Voltage	-0.3 to +V _{CC} + 0.3 V
DC Output Current, Into LOW Outputs	30 mA
DC Input Current	-10 to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Temperature (T _A)	0 to +70°C
Supply Voltage (V _{CC})	+4.75 to +5.25 V
Military* (M) Devices	
Temperature (T _A)	-55 to +125°C
Supply Voltage (V _{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_A = +25°C, +125°C, and -55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} , I _{OH} = -0.4 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} , I _{OL} = 4 mA		0.5	V
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)	2.0		V
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)		0.8	V
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = 0.4 V		-10	μA
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC} - 0.5 V		10	μA
I _{OZH} I _{OZL}	Off State (High Impedance) Output Current	V _{CC} = Max.		10	μA
				-10	
I _{CC}	Static Power Supply Current	V _{CC} = Max., V _{IN} = V _{CC} or GND, I _O = 0 μA		25	mA
				25	
C _{PD}	Power Dissipation Capacitance (Note 3)	V _{CC} = 5.0 V, T _A = 25°C, No Load	3000 pF Typical		

- Notes: 1. V_{CC} conditions shown as Min. or Max., refer to the military or commercial V_{CC} limits.
 2. These input levels provide zero noise immunity and should only be statically tested in a noise-free environment (not functionally tested).
 3. C_{PD} determines the no-load dynamic current consumption:
 $I_{CC}(\text{Total}) = I_{CC}(\text{Static}) + C_{PD} V_{CC} f$, where f is the switching frequency of the majority of the internal nodes, normally one-half of the clock frequency. This specification is not tested.

SWITCHING CHARACTERISTICS over **COMMERCIAL** operating range

No.	Parameter Symbol	Parameter Description	Test Conditions	29C323		29C323-1		29C323-2		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
UNLOCKED MODE										
1	t _{MUC}	Unlocked Multiply Time X ₀ - X ₃₁ , Y ₀ - Y ₃₁ to P ₀ - P ₃₁	FTX/Y/P = HIGH		120		100		70	ns
2	t _{MUCPP}	Unlocked Multiply Time X ₀ - X ₃₁ , Y ₀ - Y ₃₁ to PP ₀ - PP ₃	FTX/Y/P = HIGH		125		105		75	ns
3	t _{IP}	Instruction to P ₀ - P ₃₁ (Note 1)	Output Taken From Adder FTI = HIGH		120		100		70	ns
4	t _{IPP}	Instruction to PP ₀ - PP ₃	Output Taken From Adder FTI = HIGH		125		105		75	ns
CLOCKED MODE										
5	t _{MC}	Clocked Multiply Time	FTX/Y/P = LOW		100		80		55	ns
6	t _{PDP}	Clock to P ₀ - P ₃₁	Output Taken from Temp or Product Reg.		38		30		25	ns
7	t _{PDPP}	Clock to PP ₀ - PP ₃	Output Taken from Temp or Product Reg.		43		35		30	ns
8	t _{PAP}	Clock to P ₀ - P ₃₁	Output Taken from Adder, FTX/Y/I = LOW		135		115		80	ns
9	t _{PAPP}	Clock to PP ₀ - PP ₃	Output Taken from Adder, FTX/Y/I = LOW		140		120		85	ns
10	t _{SP}	Data to Product Register Setup Time	FTX/Y = HIGH	110		90		65		ns
11	t _{HP}	Data to Product Register Hold Time	FTX/Y = HIGH	0		0		0		ns
12	t _{SIPT}	Instruction to Product Register Setup Time	FTI = HIGH	110		90		65		ns
13	t _{HIPT}	Instruction to Product Register Hold Time	FTI = HIGH	0		0		0		ns
14	t _{PWH}	Clock Pulse Width HIGH		20		20		15		ns
15	t _{PWL}	Clock Pulse Width LOW		20		20		15		ns
SETUP AND HOLD TIMES										
16	t _{SXY}	Register XA, XB, YA, YB Setup Time		21		18		15		ns
17	t _{HXY}	Register XA, XB, YA, YB Hold Time		0		0		0		ns
18	t _{SI}	Instruction Register Setup Time		18		15		10		ns
19	t _{HI}	Instruction Register Hold Time		0		0		0		ns
20	t _{SEN}	Register Enable Setup Time		18		15		10		ns
21	t _{HEN}	Register Enable Hold Time		0		0		0		ns
22	t _{STS}	TSEL Setup Time		18		15		10		ns
23	t _{HTS}	TSEL Hold Time		0		0		0		ns
COMMON PARAMETERS										
24	t _{PP}	PSEL0 - PSEL1 to P ₀ - P ₃₁	To Active State Only		35		30		25	ns
25	t _{PPP}	PSEL0 - PSEL1 to PP ₀ - PP ₃	To Active State Only		35		30		25	ns
26	t _{OE1}	OE to P ₀ - P ₃₁ , PP ₀ - PP ₃ Output Enable			35		30		25	ns
27	t _{OD}	OE or PSEL0 - PSEL1 to P ₀ - P ₃₁ , PP ₀ - PP ₃ Output Disable			35		30		25	ns
28	t _{DPE}	Data to PRERR			35		35		30	ns
29	t _{DHE}	Data to HDERR	Slave = HIGH		40		40		35	ns

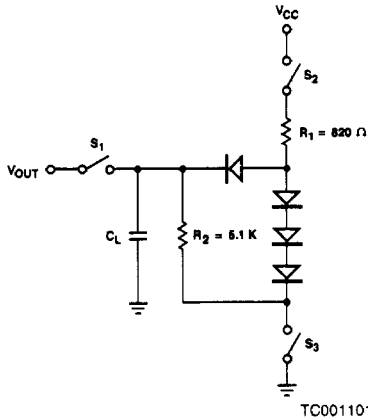
Notes: 1. Instruction signals are XSEL, YSEL, TCX, TCY, ACC0, ACC1, and RND.

SWITCHING CHARACTERISTICS over **MILITARY** operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

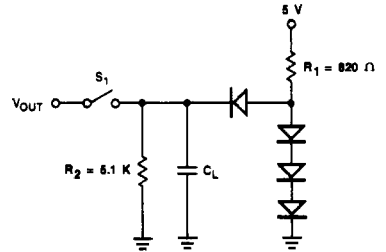
No.	Parameter Symbol	Parameter Description	Test Conditions	29C323		Unit
				Min.	Max.	
UNLOCKED MODE						
1	t _{MUC}	Unlocked Multiply Time X ₀ - X ₃₁ , Y ₀ - Y ₃₁ to P ₀ - P ₃₁	FTX/Y/P = HIGH		140	ns
2	t _{MUCPP}	Unlocked Multiply Time X ₀ - X ₃₁ , Y ₀ - Y ₃₁ to PP ₀ - PP ₃	FTX/Y/P = HIGH		145	ns
3	t _{IP}	Instruction to P ₀ - P ₃₁ (Note 1)	Output Taken From Adder FTI = HIGH		140	ns
4	t _{IPP}	Instruction to PP ₀ - PP ₃	Output Taken From Adder FTI = HIGH		145	ns
CLOCKED MODE						
5	t _{MC}	Clocked Multiply Time	FTX/Y/P = LOW		120	ns
6	t _{PDP}	Clock to P ₀ - P ₃₁	Output Taken from Temp or Product Reg.		45	ns
7	t _{PDPP}	Clock to PP ₀ - PP ₃	Output Taken from Temp or Product Reg.		50	ns
8	t _{PAP}	Clock to P ₀ - P ₃₁	Output Taken from Adder, FTX/Y/I = LOW		150	ns
9	t _{PAPP}	Clock to PP ₀ - PP ₃	Output Taken from Adder, FTX/Y/I = LOW		155	ns
10	t _{SP}	Data to Product Register Setup Time	FTX/Y = HIGH	135		ns
11	t _{HP}	Data to Product Register Hold Time	FTX/Y = HIGH	0		ns
12	t _{SIPT}	Instruction to Product Reg. Setup Time	FTI = HIGH	135		ns
13	t _{HIPT}	Instruction to Product Reg. Hold Time	FTI = HIGH	0		ns
14	t _{PWH}	Clock Pulse Width HIGH		20		ns
15	t _{PWL}	Clock Pulse Width LOW		20		ns
SETUP AND HOLD TIMES						
16	t _{SXY}	Register XA, XB, YA, YB Setup Time		24		ns
17	t _{HXY}	Register XA, XB, YA, YB Hold Time		0		ns
18	t _{SI}	Instruction Register Setup Time		20		ns
19	t _{HI}	Instruction Register Hold Time		0		ns
20	t _{SEN}	Register Enable Setup Time		20		ns
21	t _{HEN}	Register Enable Hold Time		0		ns
22	t _{STS}	TSEL Setup Time		20		ns
23	t _{HTS}	TSEL Hold Time		0		ns
COMMON PARAMETERS						
24	t _{PP}	PSEL0 - PSEL1 to P ₀ - P ₃₁	To Active State Only		40	ns
25	t _{PPP}	PSEL0 - PSEL1 to PP ₀ - PP ₃	To Active State Only		40	ns
26	t _{OEPI}	OE to P ₀ - P ₃₁ , PP ₀ - PP ₃ Output Enable			40	ns
27	t _{OD}	OE or PSEL0 - PSEL1 to P ₀ - P ₃₁ , PP ₀ - PP ₃ Output Disable			40	ns
28	t _{DPE}	Data to PRERR			40	ns
29	t _{DHE}	Data to HDERR	Slave = HIGH		45	ns

Notes: 1. Instruction signals are XSEL, YSEL, TCX, TCY, ACC0, ACC1, and RND.

SWITCHING TEST CIRCUITS



A. Three-State Outputs








B. Normal Outputs

- Notes:
1. $C_L = 50$ PF includes scope probe, wiring and stray capacitances without device in test fixture.
 2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
 3. S_1 and S_3 are closed while S_2 is open for tp_{ZH} test.
 S_1 and S_2 are closed while S_3 is open for tp_{ZL} test.
 4. $C_L =$ TBD for output disable tests.

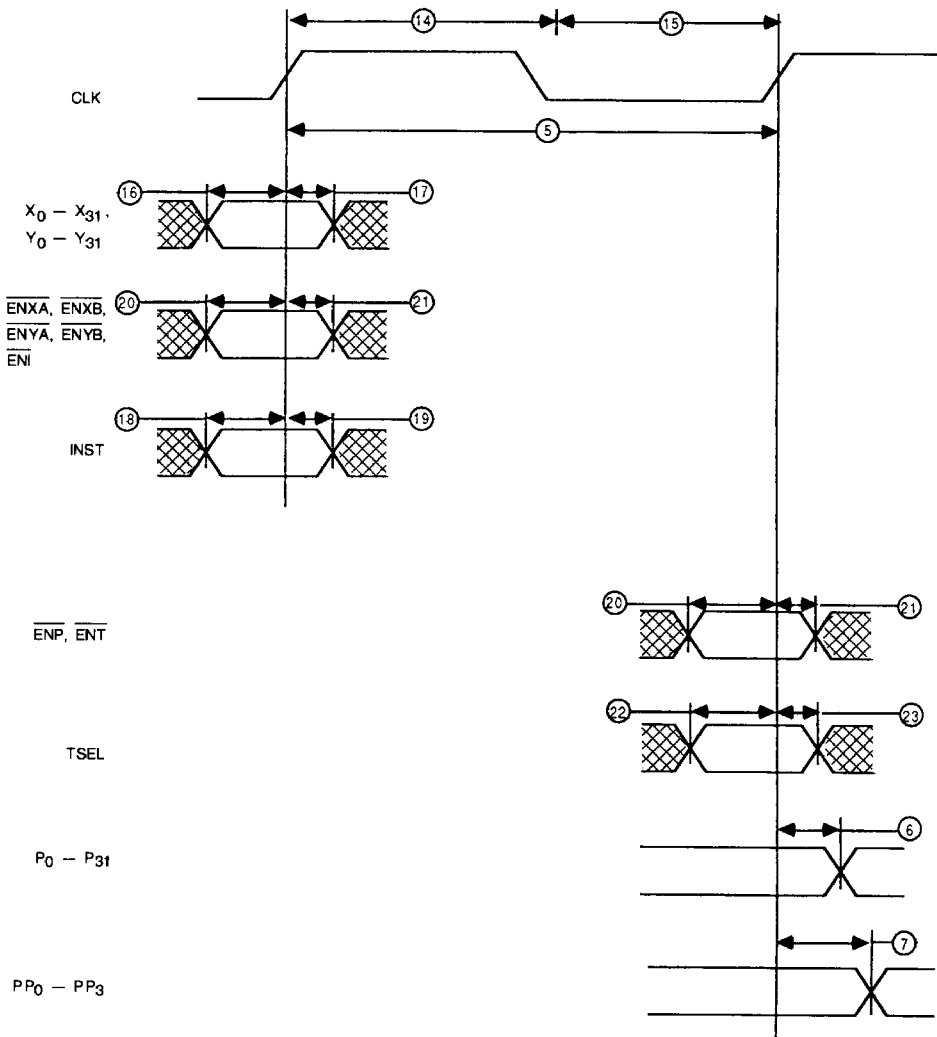
SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

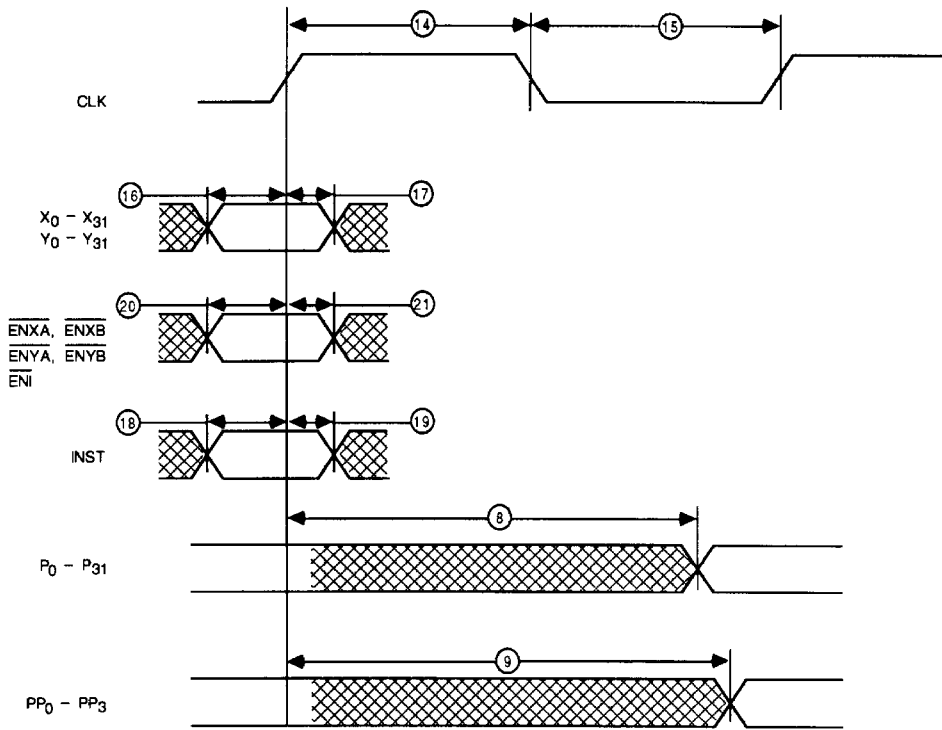
SWITCHING WAVEFORMS (Cont'd.)



WF022971

Clocked Operation: FTX, Y, P, I = LOW

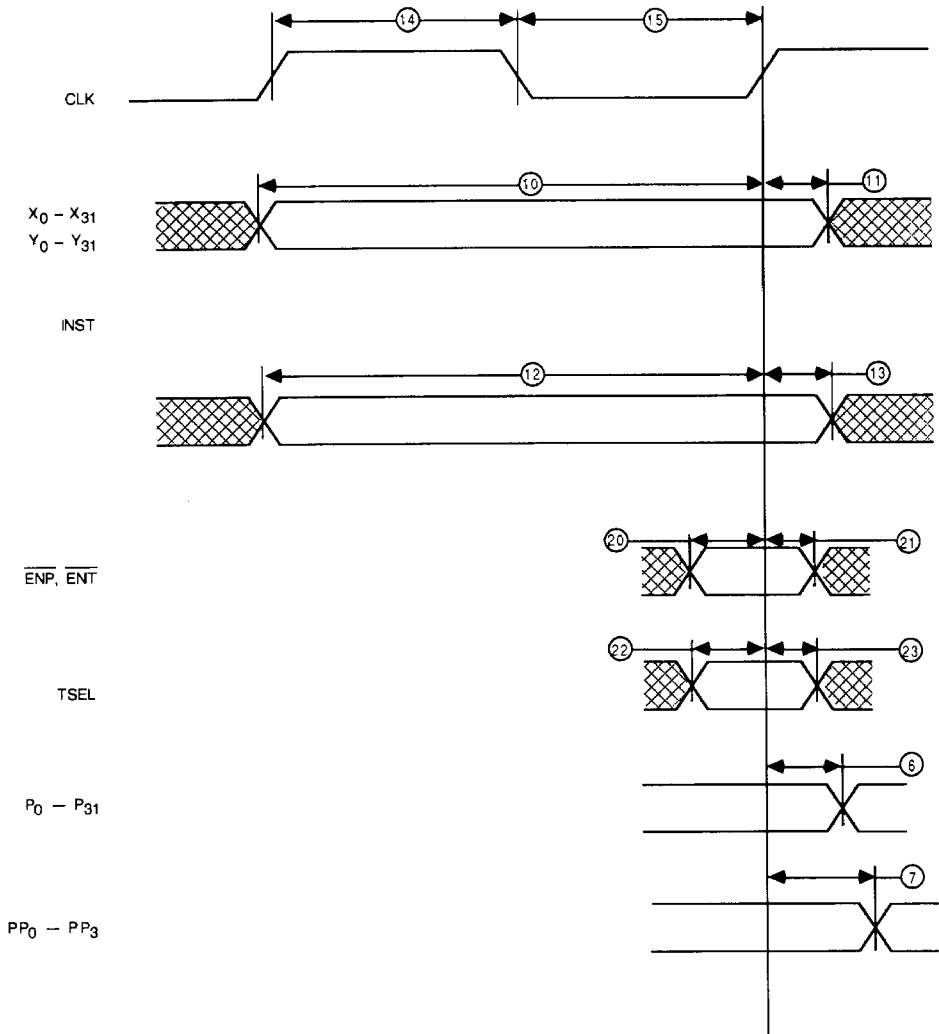
SWITCHING WAVEFORMS (Cont'd.)



WF022960

**Clocked Operation: Output Taken from Adder
(FTX, Y, I = LOW; FTP = HIGH; PSEL1 ≠ PSEL0)**

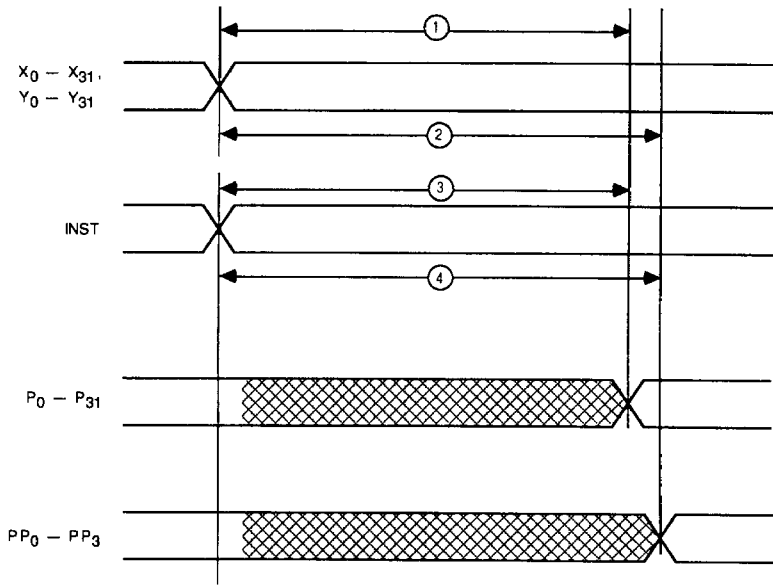
SWITCHING WAVEFORMS (Cont'd.)



WF022983

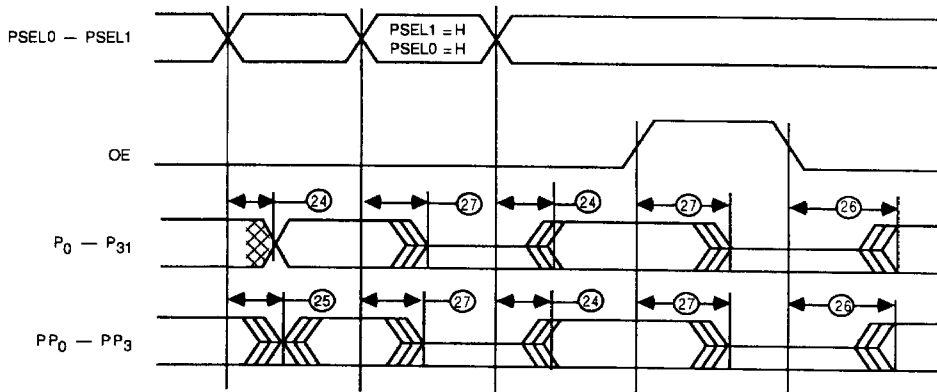
**Clocked Operation: Input Registers Bypassed
(FTX, Y, I = HIGH; FTP = LOW)**

SWITCHING WAVEFORMS (Cont'd.)



WF022990

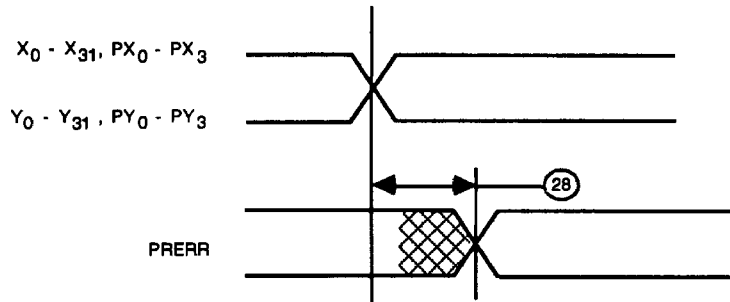
Unlocked Mode: FTX, Y, I, P = HIGH



WF023001

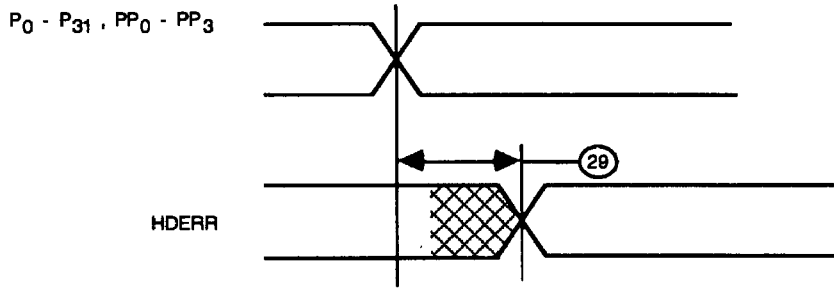
Output Select Timing

SWITCHING WAVEFORMS (Cont'd.)



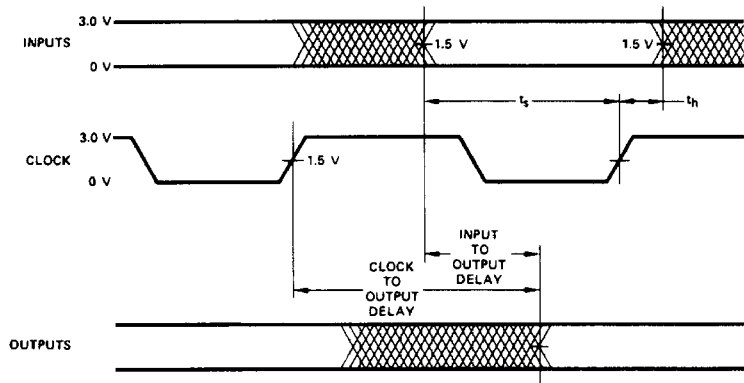
WF023013

PRERR Timing



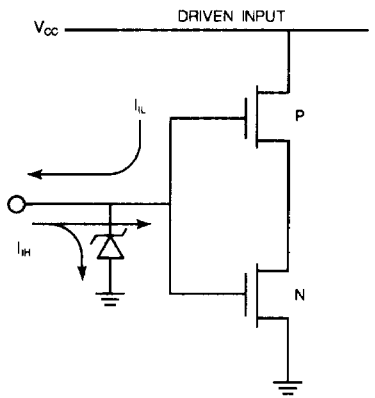
WF023024

Slave Mode Timing



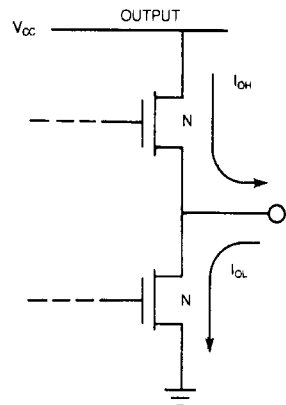
WFR02990

INPUT/OUTPUT CURRENT INTERFACE DIAGRAMS



IC000861

$C_I \approx 5.0$ pF, all inputs



IC000870

$C_O \approx 5.0$ pF, all outputs