HYM532120A W-Series

1M x 32-bit CMOS DRAM MODULE

DESCRIPTION

The HYM532120A is a 1M x 32-bit Fast page mode CMOS DRAM module consisting of two HY5118160B in 42/42 pin SOJ or TSOPII on a 72 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM.
The HYM532120AW/ASLW/ATW/ASLTW are Tin-Lead plated and HYM532120AWG/ASLWG /ATWG/ASLTWG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 4M byte memory.

FEATURES

- **Low power dissipation**
  Max. self-refresh 3.85mW (SL-part)
  Max. battery back-up 4.95mW (SL-part)
  Max. CMOS standby 3.3mW (SL-part)
  11.0mW
  Max. TTL standby 22.0mW
  Max. operating

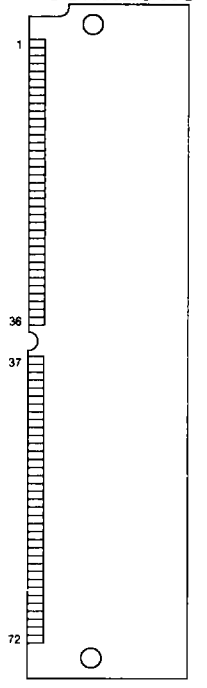
Speed	Power
60	1.76W
70	1.65W
80	1.54W

- **Single power supply of 5V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tPC
60	70ns	15ns	45ns
70	80ns	20ns	50ns
80	100ns	20ns	60ns

- **Fast page mode operation**
- **CAS-before-RAS, RAS-only, Hidden refresh, Self-refresh**
- **1024 refresh cycles / 256ms (SL-part)**
  1024 refresh cycles / 16ms

PIN CONNECTION



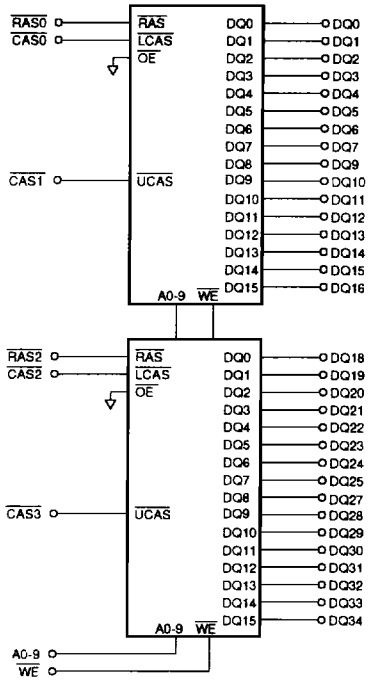
PIN DESCRIPTION

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0-A9	Address Input
DQ0-DQ34	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

PIN NAME

#	NAME	#	NAME
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	Vss
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	NC
11	NC	47	$\overline{WE}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	NC	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-60	-70	-80
PD1	Vss	Vss	Vss
PD2	Vss	Vss	Vss
PD3	NC	Vss	NC
PD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	2.0	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+ 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}$+ 1.0, All other pins not under test= V_{SS}		-20	20	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	Vcc Supply Current, Operating	t_{RC}= t_{RC} (min.)	60 70 80	- - -	320 300 280	mA	1,2,3
I_{CC2}	Vcc Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs≥ V_{SS}		-	4	mA	
I_{CC3}	Vcc Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	320 300 280	mA	1,3
I_{CC4}	Vcc Supply Current, Fast Page mode	t_{PC}= t_{PC} (min.)	60 70 80	- - -	220 200 180	mA	1,2,3
I_{CC5}	Vcc Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ Vcc–0.2V	 SL-part	- -	2 0.6	mA	 5
I_{CC6}	Vcc Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	320 300 280	mA	1,3
I_{CC7}	Vcc Supply Current, Battery Back Up (SL-part only)	t_{RC}= 250µs, $\overline{CAS}$= CBR cycling or 0.2V, $\overline{WE}$= Vcc–0.2V, A0-A9= Vcc–0.2V or 0.2V, DQ0-DQ34= Vcc–0.2V, 0.2V, or open	$t_{RAS} \le$ 300ns $t_{RAS} \le$ 1µs	- -	0.7 0.9	mA	1,4,5
I_{CC8}	Vcc Supply Current, Self Pefresh (SL-Part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤0.2v other pins same as I_{CC7}			0.7	mA	
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –5mA		2.4	-	V	

NOTE :
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading. Specified values are obtained with the output open.
3. Icc is specified as average current. for I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$= V_{IL}. for I_{CC4}, address can be changed maximum once while $\overline{CAS}$= V_{IH}.
4. Only t_{RAS}(max.)= 1µs is applied to refresh of battery backup but t_{RAS}(max.)= 10µs is applied to normal functional operation.
5. I_{CC5}(max.)= 0.6mA, I_{CC7} and I_{CC8} are applied to SL-part only (HYM532120ASLW/ASLTW/ASLWG/ASLTWG).

AC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS}= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM532120AW-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX..		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	40	-	50	-	ns	
4	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	40	-	50	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	5,10,11
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	5,10
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	5,11
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	35	-	45	ns	5
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	5
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	6
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	4
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	40	-	50	-	60	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	15	10K	15	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	45	20	50	20	60	ns	10
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	11
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	55	-	60	-	75	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	7
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	7
31	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	55	-	60	-	75	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	8
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	8
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	
		SL-part	-	256	-	256	-	256		12
40	tWCS	Write Command Set-up Time	0		0	-	0	-	ns	9

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM532120AW-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
43	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
44	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	110	-	130	-	150	-	ns	
45	tCHS	$\overline{CAS}$ Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
46	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	ns	
47	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	110	-	130	-	150	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initilization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{RAS}$= V_{SS} during power-up, the HYM532120A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
4. Refer to the HY5118160B data sheet for detailed information.
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
9. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
10. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
11. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
12. t_{REF}(max.)= 256ms is applied to SL-part only (HYM532120ASLW/ASLTW/ASLWG/ASLTWG).

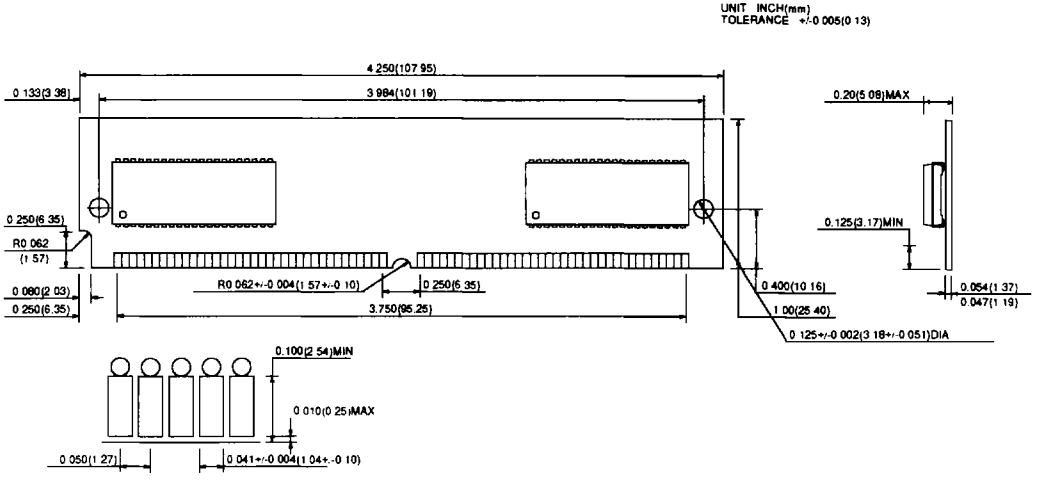
CAPACITANCE

(T_A= 25°C, V_{CC}= 5V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

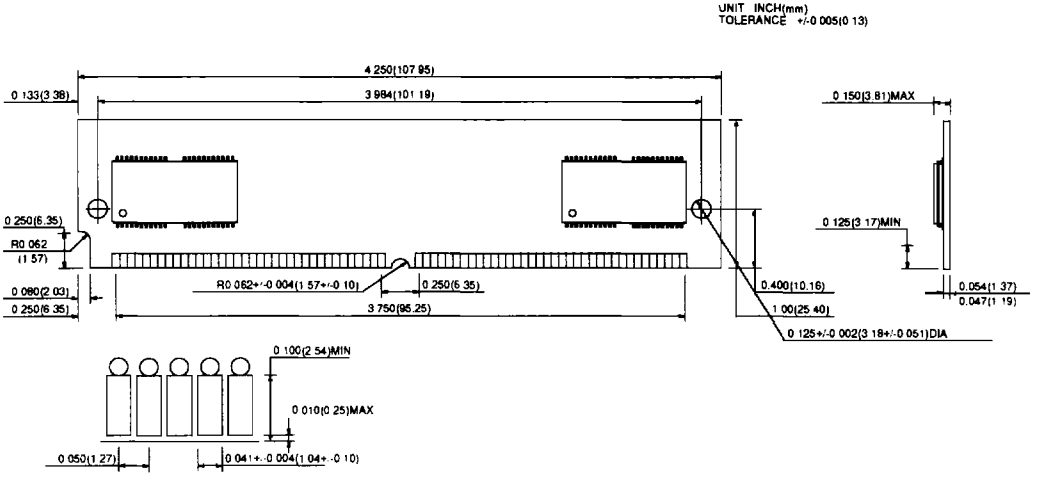
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9)	-	12	pF
C_{IN2}	Input Capacitance ($\overline{WE}$)	-	17	PF
C_{IN3}	Input Capacitance ($\overline{RAS0}$-$\overline{RAS2}$)	-	17	pF
C_{IN4}	Input Capacitance ($\overline{CAS0}$-$\overline{CAS3}$)	-	20	pF
C_{DQ}	Data Input/Output Capacitance (DQ0-DQ34)	-	17	pF

PACKAGE INFORMATION

72 pin Single In-line Memory Module (W ; Tin-Lead plated, WG ; Gold plated)
HYM532120A/ASL (SOJ Mounted)



HYM532120AT/ASLT (TSOPII Mounted)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM532120AW	60/70/80		SIMM	Tin-Lead
HYM532120ASLW	60/70/80	SL-part	SIMM	Tin-Lead
HYM532120ATW	60/70/80		SIMM	Tin-Lead
HYM532120ASLTW	60/70/80	SL-part	SIMM	Tin-Lead
HYM532120AWG	60/70/80		SIMM	Gold
HYM532120ASLWG	60/70/80	SL-part	SIMM	Gold
HYM532120ATWG	60/70/80		SIMM	Gold
HYM532120ASLTWG	60/70/80	SL-part	SIMM	Gold