CIS8204

SimpliPHY™ Gigabit Ethernet PHY Series

Quad, Low Power, 10 / 100 / 1000BASE-T PHY with GMII / MII, RGMII, TBI and RTBI MAC Interfaces

1 General Description

Ideally suited for high port density Gigabit Ethernet switches and routers, or multi-port Network Interface Cards (NICs), Cicada's single chip CIS8204 integrates four low-power, triple speed (10BASE-T, 100BASE-TX, and 1000BASE-T) Ethernet transceivers in a thermally-enhanced, 388-pin plastic Ball Grid Array (BGA) package.

The CIS8204 physical layer "PHY" IC leverages Cicada's proprietary **MicroPHY™ DSP Technology**, key to enabling a Quad-port Gigabit Ethernet PHY solution on a single chip. Cicada's highly optimized DSP architecture yields robust performance and low power, supporting 1000BASE-T over unshielded twisted pair (UTP) cable, with more than 5dB of design margin with respect to all worst case impairments (NEXT, FEXT, Echo, and system noise sources).

Each of the four independent 1000BASE-T transceivers features an industry standard GMII interface in addition to the TBI interface or the pin-efficient RGMII/RTBI, a 4D-PAM5 encoder/decoder, a scrambler/descrambler, a DSP-based receiver utilizing the optimum LMS (Least Mean Square) algorithm, echo cancellers, cross-talk elimination, as well as digital gain control and digital timing recovery. The device also integrates an innovative internal hybrid that allows the use of inexpensive 1:1 transformer modules. The on-chip GMII and RGMII series termination resistors simplify board design challenges by improving signal integrity and completely eliminating more than 50 external series termination resistors on the receive side of the MAC interface.

To enable maximum network management feedback to the host system and the user, Cicada-provided software routines, referred to as the VeriPHY™ Link Management Suite, allow extensive network and cable plant operating and status information, such as the cable length and the effective Bit Error Rate (BER), to be easily integrated with NIC or switch software, greatly simplifying Gigabit Ethernet network deployment and management.

2 System Diagram

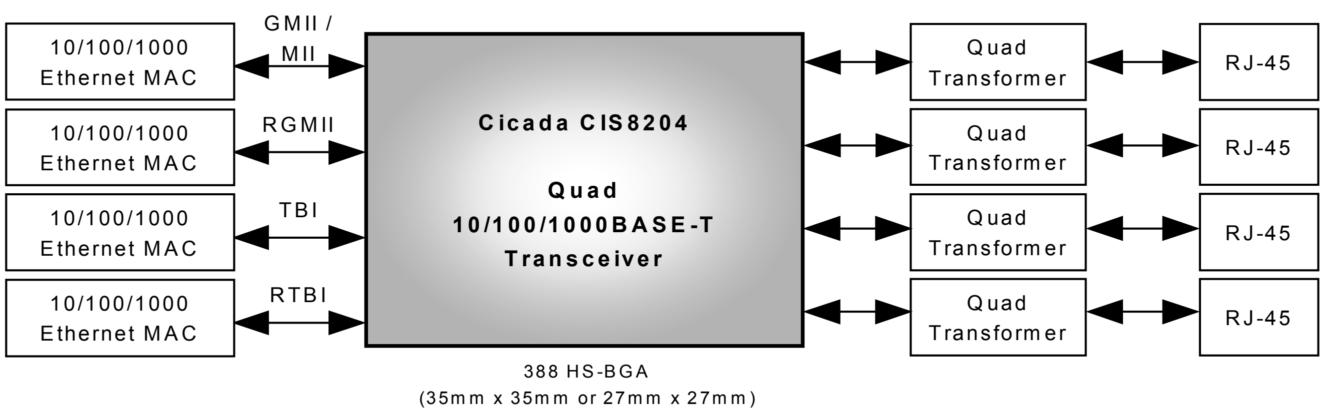


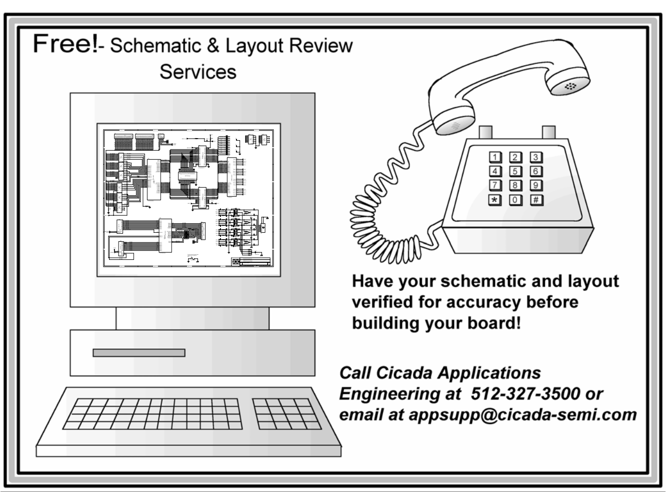
Figure 2-1. CIS8204 System Diagram

3 Features

Features	Benefits
Quad, low power, 10/100/1000BASE-T transceivers in a single, small footprint, plastic package	Catalyzes market for low-cost & high-density LAN, WAN, SAN, & MAN switches
Choice of packaging: 27mm & 35mm body, 388-pin, plastic HS-BGA packages	Enables commercial & industrial temperature range Gigabit Ethernet systems
Breakthrough power consumption of less than 1.0W per port in mainstream CMOS process	Eliminates heat sinks for Gigabit-to-the-Desktop LAN switches
Proprietary, all digital, MicroPHY™ DSP-based solution with fully adaptive equalizer, echo & crosstalk cancellers, clock recovery, & baseline wander	Unmatched performance enables lower power, higher density systems with maximum real-world noise immunity & full specification compliance
Highly tolerant of link partner frequency offsets outside of Ethernet specifications: better than ±400ppm	Allows trouble-free migration to 1000BASE-T by minimizing common interoperability problems
IEEE 802.3 (10BASE-T), 802.3u (100BASE-TX), & 802.3ab (1000BASE-T) compliant	Enables widespread Gigabit Ethernet systems deployment over existing Category 5 cable plants
Supports industry standard GMII & TBI	Connects to existing GMII & TBI-based MAC ASICs
Optional support for pin and power efficient RGMII (Reduced GMII) & RTBI (Reduced TBI)	Significantly reduces pin-count overhead on MAC & switching ASICs, from 24 (GMII) to 12 (RGMII) per port
Supports 3.3V I/O for RGMII & RTBI	Simplifies power supply design
Integrated GMII / RGMII & TBI / RTBI series termination resistors, including innovative, on-chip RGMII PCB timing compensation	Simplifies board designs, improves MAC I/F signal integrity, lowers power consumption, & eliminates >50 external termination resistors on system board
Automatic detection and correction of non-compliant 1000BASE-T PHYs, twisted pair swaps, pair skew, MDI crossover, & pair polarity at all three speeds	Works seamlessly with1st-generation 1000BASE-T PHYs & simplifies systems deployment by automatically compensating for common cable installation problems
Low EMI line drivers with extremely robust ESD & Cable-sourced ESD (CESD) performance	Reduces EMI engineering challenges & eliminates deployment risks in newer cable plant installations
Jumbo Packet support >10KB, including programmable synchronization FIFOs	Enables maximum performance flexibility in custom LAN & SAN networks
Standard JTAG and NAND Tree test interfaces	Provides unmatched IC test coverage at lowest cost
Low power, 3.3V / 1.5V, mainstream digital CMOS	Minimizes costs & enables highest integration levels

4 Applications

- High Port Density 10/100/1000BASE-T Switches
- Workgroup LAN Switches & Routers
- Gigabit Ethernet-based SAN, NAS, and MAN Systems
- High Performance Workstations & Multi-Port Server NICs



5 Device Block Diagram

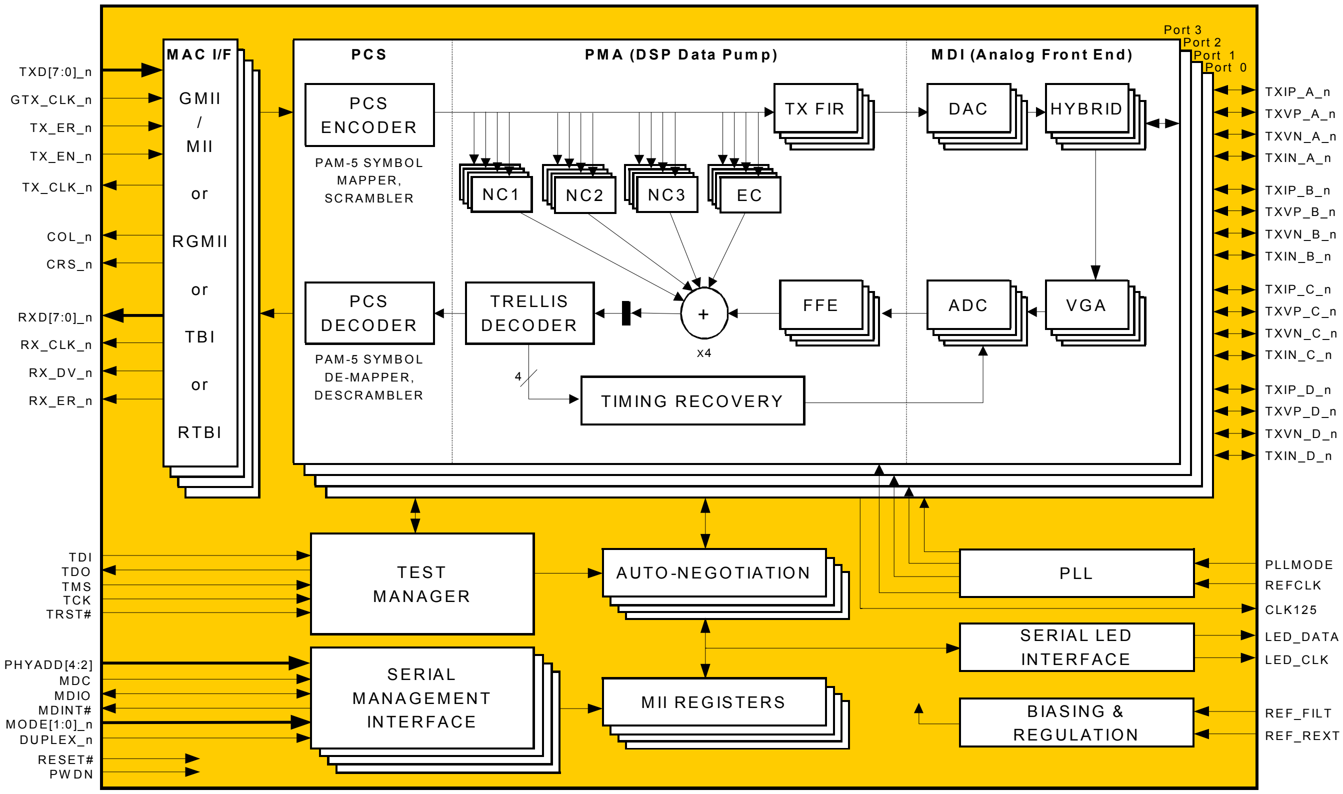


Figure 5-1. CIS8204 Block Diagram (GMII pin names shown)[1]

[1] n = port number (0, 1, 2, 3)

6 Table of Contents

1 GENERAL DESCRIPTION 2
2 SYSTEM DIAGRAM 2
3 FEATURES & BENEFITS 3
4 APPLICATIONS 3
5 DEVICE BLOCK DIAGRAM 4
6 TABLE OF CONTENTS 5
7 LIST OF FIGURES 8
8 LIST OF TABLES 10
9 RELEVANT SPECIFICATIONS & DOCUMENTATION 12
10 DOCUMENTATION TYPES 12
11 DATA SHEET CONVENTIONS 13
12 FUNCTIONAL OVERVIEW 14
12.1 MAC INTERFACE (GMII / RGMII / MII, OR TBI / RTBI) 14
12.2 TWISTED PAIR INTERFACE (TPI) 14
12.3 SERIAL MANAGEMENT INTERFACE (SMI) 15
12.4 SERIAL LED INTERFACE (SLI) 15
12.5 SYSTEM CLOCK INTERFACE (SCI) 15
12.6 TEST MODE INTERFACE (TMI) 15
12.7 ANALOG FRONT END (AFE) 15
12.8 DSP DATA PUMP CORE 16
12.9 PHYSICAL CODING SUBLAYER (PCS) 16
12.10 SYNCHRONIZATION FIFOS 17
13 PACKAGE PIN ASSIGNMENTS & SIGNAL DESCRIPTIONS 18
13.1 388 HS-BGA PACKAGE BALL DIAGRAM 18
13.2 BGA BALL TO SIGNAL NAME CROSS REFERENCE (LEFT SIDE) 19
13.3 BGA BALL TO SIGNAL NAME CROSS REFERENCE (RIGHT SIDE) 20
13.4 PIN DESCRIPTIONS 21
13.5 SIGNAL TYPE DESCRIPTIONS 21
13.6 MAC TRANSMIT INTERFACE PINS (MAC TX) 22
13.7 MAC RECEIVE INTERFACE PINS (MAC RX) 24
13.8 TWISTED PAIR INTERFACE PINS (TPI) 27
13.9 SERIAL MANAGEMENT INTERFACE PINS (SMI) 29
13.10 CONFIGURATION AND CONTROL PINS (CONFIG) 29
13.11 SYSTEM CLOCK INTERFACE PINS (SCI) 30
13.12 SERIAL LED INTERFACE PINS (SLI) 31
13.13 JTAG TEST ACCESS PORT (TAP) 31
13.14 ANALOG BIAS PINS (AP) 31
13.15 NO CONNECTS (NC) 32
13.16 DIGITAL POWER SUPPLY PINS 33
13.17 ANALOG POWER SUPPLY PINS 35
14 SYSTEM SCHEMATICS 36
14.1 GENERAL SYSTEM SCHEMATIC 36
14.2 SYSTEM SCHEMATIC - POWER SUPPLIES 37
15 MAC INTERFACES 38
15.1 GMII MAC I/F 38
15.2 MII MAC I/F 39
15.3 RGMII MAC I/F 40
15.4 TBI MAC I/F 41
15.5 RTBI MAC I/F 42
16 SERIAL MANAGEMENT INTERFACE (SMI) 43
16.1 SMI INTERRUPT 44
17 SERIAL LED INTERFACE 45
18 TEST MODE INTERFACE (JTAG) 46

18.1 SUPPORTED INSTRUCTIONS AND INSTRUCTION CODES 47
18.2 BOUNDARY-SCAN REGISTER CELL ORDER 48
18.3 NAND TREE TEST MODE 52

19 INITIALIZATION & CONFIGURATION 54
19.1 RESETS 54
19.2 POWER-UP SEQUENCE 54
19.3 MANUAL CONFIGURATION 55
19.4 MANUAL MASTER/SLAVE MODE 55
19.5 AUTO-NEGOTIATION 55
19.6 MAC I/F CONFIGURATION 57
19.7 SYSTEM CLOCK INTERFACE (SCI) 57
19.8 AUTO MDI / MDI-X FUNCTION 58
19.9 SERIAL LED I/F 59
19.10 POWER SUPPLY DECOUPLING AND BOARD LAYOUT GUIDELINES 59

20 MII REGISTER SET CONVENTIONS 60
20.1 MII REGISTER NAMES & ADDRESSES 60
20.2 MII REGISTER MAP QUICK REFERENCE (SHEET 1 OF 2) 61

21 MII REGISTER DESCRIPTIONS 63
21.1 REGISTER 0 (00H) – MODE CONTROL REGISTER 63
21.2 REGISTER 1 (01H) – MODE STATUS REGISTER 65
21.3 REGISTER 2 (02H) – PHY IDENTIFIER REGISTER #1 67
21.4 REGISTER 3 (03H) – PHY IDENTIFIER REGISTER #2 67
21.5 REGISTER 4 (04H) – AUTO-NEGOTIATION ADVERTISEMENT REGISTER 68
21.6 REGISTER 5 (05H) – AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER 69
21.7 REGISTER 6 (06H) – AUTO-NEGOTIATION EXPANSION REGISTER 70
21.8 REGISTER 7 (07H) – AUTO-NEGOTIATION NEXT-PAGE TRANSMIT REGISTER 71
21.9 REGISTER 8 (08H) – AUTO-NEGOTIATION LINK PARTNER NEXT-PAGE RECEIVE REGISTER 72
21.10 REGISTER 9 (09H) – 1000BASE-T CONTROL REGISTER 73
21.11 REGISTER 10 (0AH) – 1000BASE-T STATUS REGISTER 75
21.12 REGISTER 11 (0BH) – RESERVED REGISTER 77
21.13 REGISTER 12 (0CH) – RESERVED REGISTER 77
21.14 REGISTER 13 (0DH) – RESERVED REGISTER 77
21.15 REGISTER 14 (0EH) – RESERVED REGISTER 77
21.16 REGISTER 15 (0FH) – 1000BASE-T STATUS EXTENSION REGISTER #1 78
21.17 REGISTER 16 (10H) – 100BASE-TX STATUS EXTENSION REGISTER 79
21.18 REGISTER 17 (11H) – 1000BASE-T STATUS EXTENSION REGISTER #2 81
21.19 REGISTER 18 (12H) – BYPASS CONTROL REGISTER 83
21.20 REGISTER 19 (13H) – RECEIVE ERROR COUNTER REGISTER 87
21.21 REGISTER 20 (14H) – FALSE CARRIER SENSE COUNTER REGISTER 87
21.22 REGISTER 21 (15H) – DISCONNECT COUNTER REGISTER 87
21.23 REGISTER 22 (16H) – 10BASE-T CONTROL & STATUS REGISTER 88
21.24 REGISTER 23 (17H) – EXTENDED PHY CONTROL REGISTER #1 90
21.25 REGISTER 24 (18H) – EXTENDED PHY CONTROL REGISTER #2 92
21.26 REGISTER 25 (19H) – INTERRUPT MASK REGISTER 95
21.27 REGISTER 26 (1AH) – INTERRUPT STATUS REGISTER 97
21.28 REGISTER 27 (1BH) – SERIAL LED CONTROL REGISTER 99
21.29 REGISTER 28 (1CH) – AUXILIARY CONTROL & STATUS REGISTER 102
21.30 REGISTER 29 (1DH) – DELAY SKEW STATUS REGISTER 105
21.31 REGISTER 30 (1EH) – RESERVED REGISTER 106
21.32 REGISTER 31 (1FH) – RESERVED REGISTER 106

22 ELECTRICAL SPECIFICATIONS 107
22.1 ABSOLUTE MAXIMUM RATINGS 107
22.2 RECOMMENDED OPERATING CONDITIONS 108
22.4 PACKAGE THERMAL SPECIFICATIONS 109
22.5 CURRENT AND POWER CONSUMPTION - APPLICATION SCENARIOS 110

23 DC SPECIFICATIONS 112
23.2 TWISTED PAIR INTERFACE PINS 112

24 AC TIMING SPECIFICATIONS 113
24.1 GMII MODE TRANSMIT (FROM MAC TO PHY) TIMING (1000BASE-T) 113
24.2 GMII MODE RECEIVE (FROM PHY TO MAC) TIMING (1000BASE-T) 114
24.3 MII TRANSMIT TIMING (100MB/S) 115
24.4 MII RECEIVE TIMING (100MB/S) 115

24.5 100BASE-TX TRANSMIT PACKET DEASSERTION TIMING 116
24.6 100BASE-TX TRANSMIT TIMING (TR/F & JITTER)1 117
24.7 100BASE-TX RECEIVE PACKET LATENCY TIMING 118
24.8 100BASE-TX RECEIVE PACKET DEASSERTION TIMING 119
24.9 RGMII/RTBI MODE TIMING 120
24.10 TBI MODE TRANSMIT TIMING 123
24.11 TBI MODE RECEIVE TIMING 124
24.12 AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING 125
24.13 JTAG TIMING 126
24.14 SMI TIMING 127
24.15 MDINT# TIMING 128
24.16 POWER-DOWN AND RESET TIMING 128
24.17 LED_CLK AND LED_DATA TIMING 129
24.18 REFCLK TIMING 130
24.19 CLK125 TIMING 131
24.20 ISOLATION TIMING 132

25 MAGNETICS SPECIFICATIONS 133

26 PACKAGING SPECIFICATIONS 134

26.1 35MM HS-BGA MECHANICAL SPECIFICATION 134
26.2 27MM HS-BGA MECHANICAL SPECIFICATION 135

27 ORDERING INFORMATION 136

27.1 DEVICES 136
27.2 EVALUATION SYSTEMS 136

28 APPLICATIONS SUPPORT 137

28.1 AVAILABLE DOCUMENTS AND APPLICATION NOTES 137
28.2 CONTACT INFORMATION 137
28.3 APPLICATION SUPPORT SERVICES 137

29 DOCUMENT HISTORY & NOTICES 138

7 List of Figures

FIGURE 2-1. CIS8204 SYSTEM DIAGRAM 2
FIGURE 5-1. CIS8204 BLOCK DIAGRAM (GMII PIN NAMES SHOWN) 4
FIGURE 13-1. 388 HS_BGA PACKAGE BALL DIAGRAM (VALID FOR 27MM AND 35MM HS-BGA PACKAGES) 18
FIGURE 13-2. 388-PIN HS-BGA (27MM OR 35MM) SIGNAL MAP FOR GMII PIN NAMES (TOP LEFT SIDE OF PACKAGE) 19
FIGURE 13-3. 388-PIN HS-BGA (27MM OR 35MM) SIGNAL MAP FOR GMII PIN NAMES (TOP RIGHT SIDE OF PACKAGE) 20
FIGURE 13-4. CIS8204 TWISTED PAIR INTERFACE (PER PHY PORT) 28
FIGURE 14-1. GENERAL SYSTEM SCHEMATIC (SHOWN WITH GMII AND 3.3V I/O) 36
FIGURE 14-2. POWER SUPPLY CONNECTIONS FOR A 3.3V I/O APPLICATION 37
FIGURE 15-1. GMII MAC INTERFACE 38
FIGURE 15-2. MII MAC INTERFACE 39
FIGURE 15-3. RGMII MAC INTERFACE 40
FIGURE 15-4. TBI MAC INTERFACE 41
FIGURE 15-5. RTBI MAC INTERFACE 42
FIGURE 16-1. MDIO READ FRAME 44
FIGURE 16-2. MDIO WRITE FRAME 44
FIGURE 16-3. LOGICAL REPRESENTATION OF MDINT# PIN 44
FIGURE 18-1. TEST ACCESS PORT AND BOUNDARY SCAN ARCHITECTURE 46
FIGURE 18-2. NAND TREE LOGIC DIAGRAMS 53
FIGURE 19-1. MDI / MDI-X CROSSOVER EXAMPLE 59
FIGURE 24-1. GMII TRANSMIT AC TIMING IN 1000BASE-T MODE 113
FIGURE 24-2. GMII RECEIVE AC TIMING IN 1000BASE-T MODE 114
FIGURE 24-3. MII TRANSMIT AC TIMING (100MB/S) 115
FIGURE 24-4. MII RECEIVE AC TIMING (100MB/S) 115
FIGURE 24-5. 100BASE-TX TRANSMIT PACKET DEASSERTION AC TIMING 116
FIGURE 24-6. 100BASE-TX TRANSMIT AC TIMING (TR/F & JITTER) 117
FIGURE 24-7. 100BASE-TX RECEIVE PACKET LATENCY AC TIMING 118
FIGURE 24-8. 100BASE-TX RECEIVE PACKET DEASSERTION AC TIMING 119
FIGURE 24-1. RGMII/RTBI UNCOMPENSATED AC TIMING AND MULTIPLEXING 121
FIGURE 24-2. RGMII/RTBI COMPENSATED AC TIMING AND MULTIPLEXING 122
FIGURE 24-3. TBI TRANSMIT AC TIMING 123
FIGURE 24-4. TBI RECEIVE AC TIMING 124
FIGURE 24-5. AUTO-NEGOTIATION FLP AC TIMING 125
FIGURE 24-6. JTAG INTERFACE AC TIMING 126
FIGURE 24-7. SMI AC TIMING 127
FIGURE 24-8. POWER-DOWN AND RESET AC TIMING 128
FIGURE 24-9. LED_CLK AND LED_DATA OUTPUT AC TIMING 129
FIGURE 24-10. REFCLK AC TIMING 130
FIGURE 24-11. CLK125 AC TIMING 131
FIGURE 24-12. ISOLATION AC TIMING 132

FIGURE 25-1. PHY-TRANSFORMER CONNECTIONS 133
FIGURE 26-1. 35MM HS-BGA MECHANICAL SPECIFICATION 134
FIGURE 26-2. 35MM HS_BGA CHIP MARKINGS 134
FIGURE 26-3. 27MM HS-BGA MECHANICAL SPECIFICATION 135
FIGURE 26-4. 27MM HS_BGA CHIP MARKINGS 135

8 List of Tables

TABLE 9-1. CIS8204 RELEVANT SPECIFICATIONS 12
TABLE 10-1. DOCUMENTATION TYPES 12
TABLE 11-1. DATA SHEET CONVENTIONS 13
TABLE 12-1. SYNCHRONIZATION FIFOS 17
TABLE 13-1. SIGNAL TYPE DESCRIPTIONS 21
TABLE 13-2. MAC TX SIGNAL DESCRIPTIONS 22
TABLE 13-3. MAC RX SIGNAL DESCRIPTIONS 24
TABLE 13-4. TPI SIGNAL DESCRIPTIONS 27
TABLE 13-5. SMI SIGNAL DESCRIPTIONS 29
TABLE 13-6. CONFIG SIGNAL DESCRIPTIONS 29
TABLE 13-7. SCI SIGNAL DESCRIPTIONS 30
TABLE 13-8. SLI SIGNAL DESCRIPTIONS 31
TABLE 13-9. JTAG TAP SIGNAL DESCRIPTIONS 31
TABLE 13-10. AP SIGNAL DESCRIPTIONS 31
TABLE 13-11. NC SIGNAL DESCRIPTIONS 32
TABLE 13-12. DIGITAL POWER SUPPLY SIGNAL DESCRIPTIONS 33
TABLE 13-13. ANALOG POWER SUPPLY SIGNAL DESCRIPTIONS 35
TABLE 16-1. SMI FRAME FORMAT 43
TABLE 17-1. LED STATUS BIT ORDER 45
TABLE 17-2. SLI BIT DEFINITIONS 45
TABLE 18-1. JTAG DEVICE IDENTIFICATION REGISTER DESCRIPTION 46
TABLE 18-2. JTAG INTERFACE INSTRUCTION CODES 47
TABLE 18-3. JTAG BOUNDARY-SCAN PORT ORDER (SHEET 1 OF 3) 49
TABLE 18-4. NAND TREE CHAINS 52
TABLE 19-1. INITIALIZATION TYPES 54
TABLE 19-2. MAC I/F MODE DESCRIPTIONS 57
TABLE 19-3. ACCEPTED MDI PAIR CONNECTION COMBINATIONS 58
TABLE 20-1. MII REGISTER BIT MODES 60
TABLE 20-2. MII REGISTER NAMES & ADDRESSES 60
TABLE 21-1. 1000BASE-T TRANSMITTER/RECEIVER TEST MODES 73
TABLE 21-2. 1000BASE-T TRANSMITTER/RECEIVER TEST MODE 4 – QUINARY SYMBOLS 74
TABLE 21-3. CLK125 PIN MULTIPLEXED CLOCK SIGNALS 84
TABLE 21-4. MODE[1:0]_N AND DUPLEX_N PIN SETTINGS 104
TABLE 22-1. ABSOLUTE MAXIMUM RATINGS 107
TABLE 22-2. RECOMMENDED OPERATING CONDITIONS 108
TABLE 22-1. THERMAL APPLICATION DATA 109
TABLE 22-2. THERMAL APPLICATION DATA - 35MM PACKAGE 109
TABLE 22-3. THERMAL APPLICATION DATA - 27MM PACKAGE 109
TABLE 22-4. THERMAL SPECIFICATIONS - 388 PIN HSBGA 35MM PACKAGE 109

TABLE 22-5. THERMAL SPECIFICATIONS - 388 PIN HSBGA 27MM PACKAGE 109
TABLE 22-6. CURRENT AND POWER CONSUMPTION - APPLICATION I 110
TABLE 22-7. CURRENT AND POWER CONSUMPTION - APPLICATION II 110
TABLE 22-8. CRYSTAL SPECIFICATIONS 111
TABLE 23-1. DIGITAL PINS SPECIFICATIONS 112
TABLE 23-1. TPI TRANSMITTER DC SPECIFICATIONS 112
TABLE 24-1. GMII MODE TRANSMIT AC TIMING SPECIFICATIONS (1000BASE-T) 113
TABLE 24-2. GMII MODE RECEIVE AC TIMING SPECIFICATIONS (1000BASE-T) 114
TABLE 24-3. MII TRANSMIT AC TIMING SPECIFICATIONS (100MB/S) 115
TABLE 24-4. MII RECEIVE AC TIMING SPECIFICATIONS (100MB/S) 115
TABLE 24-5. 100BASE-TX TRANSMIT PACKET DEASSERTION AC TIMING SPECIFICATIONS 116
TABLE 24-6. 100BASE-TX TRANSMIT AC TIMING SPECIFICATIONS (TR/F & JITTER) 117
TABLE 24-7. 100BASE-TX RECEIVE PACKET LATENCY AC TIMING SPECIFICATIONS 118
TABLE 24-8. 100BASE-TX RECEIVE PACKET DEASSERTION AC TIMING SPECIFICATIONS 119
TABLE 24-1. RGMII/RTBI MODE AC TIMING SPECIFICATIONS 120
TABLE 24-1. TBI MODE TRANSMIT AC TIMING SPECIFICATIONS 123
TABLE 24-2. TBI MODE RECEIVE AC TIMING SPECIFICATIONS 124
TABLE 24-3. AUTO-NEGOTIATION FLP AC TIMING SPECIFICATIONS 125
TABLE 24-4. JTAG INTERFACE AC TIMING SPECIFICATIONS 126
TABLE 24-5. SMI AC TIMING SPECIFICATIONS 127
TABLE 24-6. MDINT# AC TIMING SPECIFICATIONS 128
TABLE 24-7. POWER-DOWN AND RESET AC TIMING SPECIFICATIONS 128
TABLE 24-8. LED_CLK AND LED_DATA OUTPUT AC TIMING SPECIFICATION 129
TABLE 24-9. REFCLK AC TIMING SPECIFICATIONS 130
TABLE 24-10. CLK125 AC TIMING SPECIFICATIONS 131
TABLE 24-11. ISOLATION AC TIMING SPECIFICATIONS 132
TABLE 25-1. MAGNETICS SPECIFICATIONS 133
TABLE 27-1. DEVICE ORDERING INFORMATION 136
TABLE 27-2. EVALUATION SYSTEM ORDERING INFORMATION 136
TABLE 29-1. DOCUMENT HISTORY & NOTICES 138

9 Relevant Specifications & Documentation

The CIS8204 conforms to the following specifications. Please refer to these documents for additional information.

Table 9-1. CIS8204 Relevant Specifications

Specification - Revision	Description
IEEE 802.3-2002	Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. IEEE 802.3-2002 consolidates and supersedes the following specifications: 802.3ab (1000BASE-T), 802.3z (1000BASE-X), 802.3u (Fast Ethernet), with references to ANSI X3T12 TP-PMD standard (ANSI X3.263 TP-PMD).
IEEE 1149.1-1990	Test Access Port and Boundary Scan Architecture[1]. Includes IEEE Standard 1149.1a-1993 and IEEE Standard 1149.1b-1994.
JEDEC EIA/JESD8-5	2.5V±0.2V (Normal Range), and 1.8V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits.
JEDEC JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). Revision of JESD22-A114-A.
JEDEC JESD22-A115-A	Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM). Revision of EIA/JESD22-A115.
JEDEC EIA/JESD78	IC Latch-Up Test Standard.
MIL-STD-883E	Miltary Test Method Standard for Microcircuits.
RGMII[2] Specification - v1.3, v2.0	Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Devices (per Hewlett Packard). Includes both RGMII and RTBI standards.
PICMG 2.16	IP Backplane for CompactPCI.

[1] Often referred to as the "JTAG" test standard.
[2] The RGMII interface is timing compatible with the RGMII v1.3 and v2.0 specifications. The CIS8204 RGMII is not electrically compatible with the v2.0 specification as this requires HSTL voltage levels which the CIS8204 does not support.

10 Documentation Types

The three types of documentation for each Cicada device, including the CIS8204, are listed in the following table by increasing order of completeness.

Table 10-1. Documentation Types

Documentation Type	Revision Number	Description
Advance Product Information	< 1.0.0	Initial product documentation.
Preliminary Data Sheet	< 1.0.0	Documentation conforms to data sheet format; incomplete and/or under review.
Data Sheet	≥ 1.0.0	Complete and approved documentation revision for production-qualified silicon.
Data Brief	≥ 1.0.0	Condensed version of a Data Sheet revision.

11 Data Sheet Conventions

Conventions used throughout this data sheet are specified in the following table.

Table 11-1. Data Sheet Conventions

Convention	Syntax	Examples	Description
Register number	RegisterNumber.Bit or RegisterNumber.BitRange	23.10 23.12:10	Register 23 (address 17h), bit 10. Register 23 (address 17h), bits 12, 11, and 10.
Signal name (active high)	SIGNALNAME[1]	PLLMODE	Signal name for PLLMODE.
Signal name (active low)	SIGNALNAME#[1]	RESET#	Active low reset signal.
Signal bus name	BUSNAME[MSB:LSB][1]	PHYADD[4:2][2]	PHY Address bus, bits 4, 3, and 2.
PHY port number	_n	_3	Denotes a specific PHY port #3. n= {3 || 2 || 1 ||0}.
PHY-specific port signal	SIGNALNAME_n[1]	CRS_3	Carrier Sense signals for PHY ports 3, 2, 1, and 0.[3]
Signal bus for a specific PHY port	SIGNALNAME[MSB:LSB]_n[1]	RXD[7:0]_3	Receive data bus, bits 7 through 0, for PHY port #3.[4]

1 All signal names are in all CAPITAL LETTERS.
2 PHYADD bus is common to entire device.
3 CRS signal is unique to each PHY.
4 RXD signal buses are unique to each PHY.

12 Functional Overview

Cicada's single chip CIS8204 integrates four, triple speed, (10BASE-T, 100BASE-TX, and 1000BASE-T), low power Ethernet transceivers. Each transceiver is based on Cicada's proprietary, MicroPHY™ DSP Technology, a highly robust DSP Data Pump architecture with a triple speed capable Analog Front End (AFE).

A number of innovative features have been engineered into the device with the primary goal of simplifying overall systems design and reducing power consumption, leading to maximum port density, reduced system complexity, and lower cost.

At the systems level, the following components are required to interface to the CIS8204:

- Four MAC devices supporting any combination of interfaces: GMII, MII, RGMII, TBI, or RTBI interfaces
- An optional Station Manager
- Minimal LED interface logic
- A single reference clock (either 25MHz or 125MHz)
- Two (or three) fixed power supplies, depending on the MAC I/F mode:
  - GMII mode: 3.3V and 1.5V
  - RGMII[1] and RTBI modes: 3.3V, 2.5V, and 1.5V
- Four 1:1 quad transformer modules[2]
- Line termination resistors (on MAC TX side only)
- Reference capacitor and resistor
- Power supply decoupling capacitors

Each of the four independently-configurable PHYs includes all the required physical layer functionality to support 1000BASE-T, 100BASE-TX, and 10BASE-T, in either half-duplex or full-duplex operation at each speed. The four PHY ports can be independently configured to connect with virtually any triple speed Ethernet MAC or Network Processor by individually selecting one of four available MAC interfaces: GMII (including MII for 10M/100Mb modes), RGMII, RTBI, or TBI.

The first two (MAC and Twisted Pair Interface) of the following interfaces are identical copies for each PHY port.

12.1 MAC Interface (GMII / RGMII / MII, or TBI / RTBI)

- Connects each CIS8204 PHY port to the appropriate layer 2 function, such as a triple speed Ethernet MAC.
- Supports operation in 100BASE-T mode via the IEEE standard Gigabit Media Independent Interface (GMII), or the more pin-efficient Reduced Gigabit Media Independent Interface (RGMII), without requiring a SERDES type interface to a MAC.
- All MAC interface output pins feature integrated, adaptively calibrated, 50 ohm series termination resistors to simplify PC board design, resulting in improved signal quality, elimination of all external series termination resistors, and lower on-chip power consumption.
- Supports operation in 10BASE-T and 100BASE-TX modes via the IEEE standard MII or the more pin-efficient RGMII.
- Supports operation in 1000BASE-T mode via the IEEE standard TBI or more pin-efficient RTBI interface.

12.2 Twisted Pair Interface (TPI)

- Connects each CIS8204 PHY port's four dual-duplex channels to an external 1:1 magnetic module.
- Implements an internal hybrid, which minimizes the number of external passive components and easily interfaces to several, readily available, quad transformer modules to support all three operating modes.

The CIS8204 also includes four shared interfaces, used for chip and board testing, in addition to configuring the PHY port's operating modes, or monitoring the status of the port.

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[1] The RGMII interface is timing compatible with the RGMII v1.3 and v2.0 specifications. The CIS8204 RGMII is not electrically compatible with the v2.0 specification as this requires HSTL voltage levels which the CIS8204 does not support.

[2] For PICMG 2.16 applications, the transformers can be removed. See *Transformerless Ethernet Applications Note* for more information.

12.3 Serial Management Interface (SMI)

- Enables communication and standards-specified configuration of each PHY port via a system controller, such as an external CPU or ASIC.
- Fully compliant with the IEEE 802.3 MII Management Interface specifications.
- Supports Management Data Clock (MDC) operating speeds from 0MHz to approximately 25MHz
- Provides a shared, open drain, interrupt pin (MDINT#) to signal the Station Manager of any change in the operating conditions of any of the four PHY ports.
- Optional configuration pins, MODE[1:0]_n and DUPLEX_n, provide an alternative, direct method for presetting the operating mode (speed, duplex, MASTER, SLAVE) on a per PHY port basis, without the need for a dedicated station manager.

12.4 Serial LED Interface (SLI)

- Enables each PHY port to communicate its operating conditions (e.g., transmit, receive, duplex, collision, link activity, and speed)[1] through external LEDs and simple shift registers. Two device pins (LED_CLK and LED_DATA) are used to provide a complete serial bit stream of status information, yet minimize the number of device pins.

12.5 System Clock Interface (SCI)

- Generates all internal and external clocks from the internal PLL, maintaining clock synchronization throughout the device with very low jitter.
- Allows either a single 25MHz or 125MHz reference clock to be used as the reference clock for the PHY.

12.6 Test Mode Interface (TMI)

- Enables IC manufacturing test and standard board-level testing through an industry standard JTAG 1149.1 Boundary Scan controller
- Facilitates the operation of several innovative analog and digital Built-in-Self-Test functions, which simplify and improve manufacturing test coverage, leading to reduced component and systems costs, as well as improved quality.

The three major sub-functions for each PHY port are described in the following sections.

12.7 Analog Front End (AFE)

The CIS8204 employs an advanced, low-power, hybrid MicroPHY architecture, utilizing a high speed AFE and an extremely gate- and power-efficient, compact DSP core.

The analog front end (AFE), performs the following functions in each operating mode:

- Receive and transmit signal separation (via on-chip hybrid circuitry)
- Transmit wave filtering and shaping (PMA Transmit Filter and AFE TX DAC)
- Automatic gain control (VGA)
- Receive signal quantization (ADC)
- Timing recovery phased locked loop (in concert with DSP Data Pump Core)
- Link pulse detection

In the receive data path, digital words quantized by each PHY port's four ADCs are supplied to the PMA for further processing by the various DSP Data Pump elements (adaptive equalization, echo cancellation, NEXT and FEXT cancellation, trellis decoder, and the digital timing recovery loop).

On the transmit data path, the digital transmit filters in the PMA provide digital transmit words in 3-bit PAM5 (1000BASE-T), 2-level MLT-3 (100BASE-TX), or Manchester-encoded format to the triple speed, pulse-shaping transmit DACs.

The AFE also includes an analog PLL, which generates all internal and externally-sourced clocks from either a 25MHz or 125MHz reference clock. The PLL also provides an optional, free-running 125MHz output clock for use as a highly accurate, low-jitter clock for use by other ICs in the system.

[1] Link quality status is available through MII Register 28.6.

12.8 DSP Data Pump Core

Due to its robust, low-power MicroPHY DSP architecture, the CIS8204 eases interoperability concerns by maintaining error-free operation in the presence of extreme noise and interference and in substandard cabling environments. It also supports link partner frequency offset tolerances well outside the Ethernet specifications (typically greater than ±450ppm of local and link partner frequency offset tolerances).

The primary Receive functions performed within the DSP Data Pump include:

- Echo cancellation
- Crosstalk cancellation (near and far end)
- Baseline wander correction and cancellation
- Adaptive receive equalization
- Receive signal decoding
- Digital timing recovery
- Cable pair skew compensation
- Trellis decoding (or forward error correction)

Other functions performed by the DSP core include:

- Automatic pair swap detection and correction
- Automatic cable pair polarity compensation
- Automatic MDI crossover for all three speeds

The primary transmit function implemented by the DSP core is:

- Transmit pulse shaping

12.9 Physical Coding Sublayer (PCS)

The PCS is responsible for controlling all transmit and receive data interchanges with external MACs. Depending on which MAC interface is enabled on each PHY port, the PCS transfers data to and from the MAC at various word widths, in conjunction with several MAC interface-specific control signals.

For example, in 1000BASE-T mode, the PCS receive path includes three primary functions:

- Trellis decoding
- Symbol descrambling
- 4D-PAM5 symbol demapping

These elements serve together to:

- Convert PAM-5 symbols from the DSP core into 8-bit receive data symbols for transmission to the MAC on the RXD[7:0] output pins (GMII mode)
- Generate the associated receive data control and status signals (RX_DV, RX_ER) for use by the MAC

In 1000BASE-T mode, the PCS transmit path includes the following functions:

- Trellis encoding
- Symbol scrambling
- 4D-PAM5 symbol encoding

From a functional perspective, these elements serve together to:

- Convert transmit data words from the MAC on the TXD[7:0] pins (GMII mode) to PAM-5 symbols, which are sent to the transmit filters and DACs in the DSP core and AFE, respectively

12.10 Synchronization FIFOs

The PCS is also ultimately responsible for managing clock domain synchronization between the various clocks within, and delivered to, the CIS8204. For this purpose, each PHY port of the 8204 contains a synchronizing transmit FIFO to absorb frequency differences between the local PHY clock and transmit clocks delivered by a MAC in TBI, GMII, and RGMII/RTBI modes. In TBI/RTBI modes, the device also includes a receive synchronization FIFO. The following table summarizes available synchronization FIFOs for the various MAC interface operating modes. See MII Register 24 (Extended PHY Control Register #2) for more information.

Table 12-1. Synchronization FIFOs

MAC I/F Mode	RX FIFO	TX FIFO
GMII	N/A	Yes
MII	N/A	N/A
RGMII	N/A	Yes
TBI	Yes	Yes
RTBI	Yes	Yes

13 Package Pin Assignments & Signal Descriptions

13.1 388 HS-BGA Package Ball Diagram

For complete specifications, refer to Section 26: "Packaging Specifications".

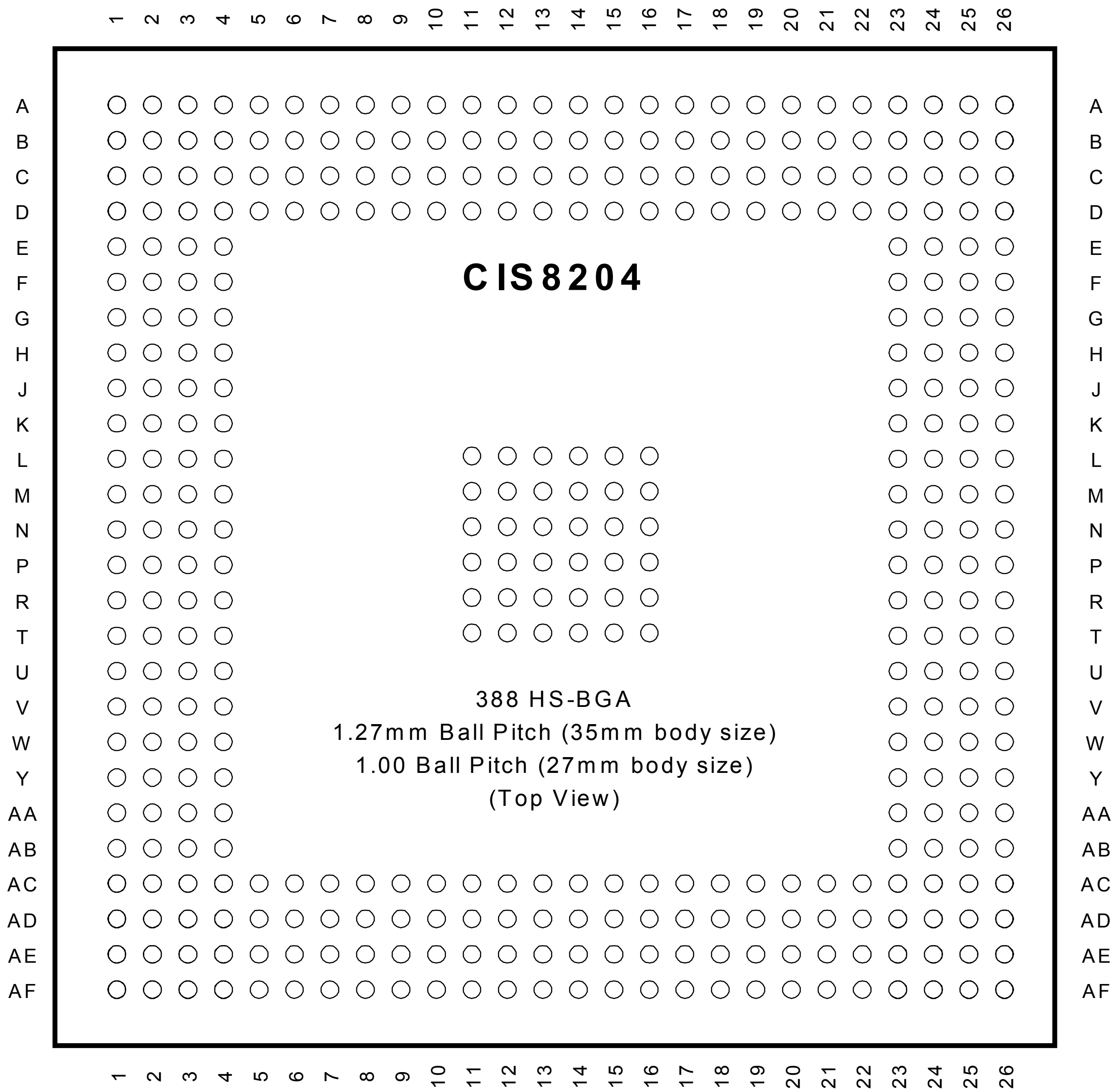

Figure 13-1. 388 HS_BGA Package Ball Diagram (valid for 27mm and 35mm HS-BGA packages)
(View from top of package with underlying BGA ball positions superimposed)

13.2 BGA Ball to Signal Name Cross Reference (LEFT side)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	TXVN_C_3	TXVP_C_3	TXVN_B_3	TXVP_B_3	TXVN_A_3	TXVP_A_3	TXVN_D_2	TXVP_D_2	TXVN_C_2	TXVP_C_2	TXVN_B_2	TXVP_B_2	TXVN_A_2
B	TXIN_C_3	TXIP_C_3	TXIN_B_3	TXIP_B_3	TXIN_A_3	TXIP_A_3	TXIN_D_2	TXIP_D_2	TXIN_C_2	TXIP_C_2	TXIN_B_2	TXIP_B_2	TXIN_A_2
C	TXVN_D_3	TXVP_D_3	VSSLD	VDDLD	VSSLD	VSSLD	VSSLD	VSSLD	VSSLD	VSSLD	VSSLD	VSSREC	VSSPLL15
D	TXIN_D_3	TXIP_D_3	VSSREC	VDDREC	VDDLD	VDDLD	VDDLD	VDDLD	VDDLD	VDDLD	VDDLD	VDDREC	VDDPLL15
E	TANA_3	TANA_2	VSSPLL33	VDDPLL33									
F	PLLMODE	REFCLK	VSS15	VDD15									
G	MODE[1]_0	MODE[0]_0	VSS15	VDD15									
H	MODE[0]_1	DUPLEX_0	VSSDIG	VDDDIG									
J	MODE[1]_1	DUPLEX_1	VSSIO	VDDIO									
K	MODE[1]_2	MODE[0]_2	VSSDIG	VDDDIG									
L	DUPLEX_2	MODE[0]_3	VSSIO	VDDIO							VSSDIG	VSSDIG	VSSDIG
M	DUPLEX_3	MODE[1]_3	VSSDIG	VDDDIG							VSSDIG	VSSDIG	VSSDIG
N	PHYADD[4]	PHYADD[3]	VSSIO	VDDIO							VSSDIG	VSSDIG	VSSDIG
P	PHYADD[2]	MDIO	VSSDIG	VDDDIG							VSSDIG	VSSDIG	VSSDIG
R	MDC	MDINT#	VSSDIG	VDDDIG							VSSDIG	VSSDIG	VSSDIG
T	RESET#	PWDN	VSSDIG	VDDDIG							VSSDIG	VSSDIG	VSSDIG
U	CRS_3	CLK125	VSSIO	VDDIO									
V	COL_3	TX_CLK_3	VSSDIG	VDDDIG									
W	RX_ER_3	RX_CLK_3	VSSIO	VDDIO									
Y	RXD[7]_3	RX_DV_3	VSSDIG	VDDDIG									
AA	RXD[6]_3	RXD[5]_3	VSSIO	VDDIO									
AB	RXD[4]_3	RXD[3]_3	VSSIO	VDDIO									
AC	RXD[2]_3	RXD[1]_3	VSSIO	VDDIO	VDDIO	VDDIO	VDDDIG	VDDIO	VDDDIG	VDDIO	VDDDIG	VDDIO	VDDDIG
AD	RXD[0]_3	GTX_CLK_3	TXD[5]_3	TXD[4]_3	TXD[1]_3	RX_CLK_2	VSSDIG	VSSIO	VSSDIG	VSSIO	VSSDIG	VSSIO	VSSDIG
AE	TX_ER_3	TXD[6]_3	TXD[3]_3	TXD[0]_3	TX_CLK_2	RX_ER_2	RXD[7]_2	RXD[5]_2	RXD[3]_2	RXD[1]_2	TX_ER_2	TX_EN_2	TXD[5]_2
AF	TX_EN_3	TXD[7]_3	TXD[2]_3	CRS_2	COL_2	RX_DV_2	RXD[6]_2	RXD[4]_2	RXD[2]_2	RXD[0]_2	GTX_CLK_2	TXD[7]_2	TXD[6]_2
	1	2	3	4	5	6	7	8	9	10	11	12	13

View is from the TOP of HS-BGA Package

Figure 13-2. 388-Pin HS-BGA (27mm or 35mm) Signal Map for GMII Pin Names (TOP LEFT side of package)

13.3 BGA Ball to Signal Name Cross Reference (RIGHT side)

View is from the TOP of HS-BGA Package

14	15	16	17	18	19	20	21	22	23	24	25	26	
TXVP_A_2	TXVN_D_1	TXVP_D_1	TXVN_C_1	TXVP_C_1	TXVN_B_1	TXVP_B_1	TXVN_A_1	TXVP_A_1	TXVN_D_0	TXVP_D_0	TXVN_C_0	TXVP_C_0	A
TXIP_A_2	TXIN_D_1	TXIP_D_1	TXIN_C_1	TXIP_C_1	TXIN_B_1	TXIP_B_1	TXIN_A_1	TXIP_A_1	TXIN_D_0	TXIP_D_0	TXIN_C_0	TXIP_C_0	B
VSSREC	VSSLD	VSSLD	VSSLD	VSSLD	VSSLD	VSSLD	VSSLD	VSSLD	NC	NC	TXVN_B_0	TXVP_B_0	C
VDDREC	VDDLD	VDDLD	VDDLD	VDDLD	VDDLD	VDDLD	VDDLD	VDDLD	NC	TANA_1	TXIN_B_0	TXIP_B_0	D
									NC	TANA_0	TXVN_A_0	TXVP_A_0	E
									VDDDIG	VSSDIG	TXIN_A_0	TXIP_A_0	F
									VDDREC	VSSIO	REF_FILT	REF_REXT	G
									VREFP	VSSREF	NC	VREFN	H
									VDD15	VSS15	TRST#	TDI	J
									VDD15	VSS15	TMS	TDO	K
VSSDIG	VSSDIG	VSSDIG							VDDIO	VSSIO	TCK	LED_CLK	L
VSSDIG	VSSDIG	VSSDIG							VDDDIG	VSSDIG	TXD[0]_0	LED_DATA	M
VSSDIG	VSSDIG	VSSDIG							VDDIO	VSSIO	TXD[1]_0	TXD[2]_0	N
VSSDIG	VSSDIG	VSSDIG							VDDDIG	VSSDIG	TXD[4]_0	TXD[3]_0	P
VSSDIG	VSSDIG	VSSDIG							VDDDIG	VSSDIG	TXD[5]_0	TXD[6]_0	R
VSSDIG	VSSDIG	VSSDIG							VDDDIG	VSSDIG	TX_EN_0	TXD[7]_0	T
									VDDIO	VSSIO	TX_ER_0	GTX_CLK_0	U
									VDDDIG	VSSDIG	RXD[1]_0	RXD[0]_0	V
									VDDIO	VSSIO	RXD[3]_0	RXD[2]_0	W
									VDDDIG	VSSDIG	RXD[5]_0	RXD[4]_0	Y
									VDDIO	VSSIO	RXD[6]_0	RXD[7]_0	AA
									VDDIO	VSSIO	RX_ER_0	RX_DV_0	AB
VDDIO	VDDDIG	VDDIO	VDDDIG	VDDIO	VDDDIG	VDDIO	VDDDIG	VDDIO	VDDIO	VSSIO	RX_CLK_0	TX_CLK_0	AC
VSSIO	VSSDIG	VSSIO	VSSDIG	VSSIO	VSSDIG	VSSIO	RXD[0]_1	TX_EN_1	TXD[6]_1	TXD[7]_1	CRS_0	COL_0	AD
TXD[4]_2	TXD[1]_2	TXD[0]_2	TX_CLK_1	RX_ER_1	RX_DV_1	RXD[5]_1	RXD[3]_1	RXD[1]_1	TX_ER_1	TXD[4]_1	TXD[2]_1	TXD[1]_1	AE
TXD[3]_2	TXD[2]_2	CRS_1	COL_1	RX_CLK_1	RXD[7]_1	RXD[6]_1	RXD[4]_1	RXD[2]_1	GTX_CLK_1	TXD[5]_1	TXD[3]_1	TXD[0]_1	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 13-3. 388-Pin HS-BGA (27mm or 35mm) Signal Map for GMII Pin Names (TOP RIGHT side of package)

13.4 Pin Descriptions

Where applicable, all electrical specifications will adhere to the GMII/MII, RGMII/RTBI, and TBI specifications found in their respective standards documents (IEEE 802.3-2002 and RGMII Specification version 1.3), unless otherwise noted.

13.5 Signal Type Descriptions

Table 13-1. Signal Type Descriptions

Symbol	Signal Type	Description
I	Digital Input	Standard digital input signal. No internal pull-up or pull-down.
I_{PU}	Digital Input with Pull-up	Standard digital input. Includes on-chip 100kΩ pull-up to VDDIO.
$I_{PU(5V)}$	5V-Tolerant Digital Input with Pull-Up	5V-tolerant digital input. Includes on-chip 100kΩ pull-up to VDDIO.
I_{PD}	Digital Input with Pull-down	Standard digital input. Includes on-chip 100kΩ pull-down to VSSIO.
O_{ZC}	Impedance Controlled Output	50Ω integrated (on-chip) source series terminated, digital output signal. Used primarily for timing-sensitive MAC I/F and 125MHz clock output pins, in addition to high speed manufacturing test mode pins.
I/O	Digital Bidirectional	Tristate-able, digital input and output signal.
I_{PU}/O	Digital Bidirectional	Tristate-able, digital input and output signal. Includes on-chip 100kΩ pull-up to VDDIO.
I_{PD}/O	Digital Bidirectional	Tristate-able, digital input and output signal. Includes on-chip 100kΩ pull-down to VSSIO.
OD	Digital Open Drain Output	Open drain digital output signal. Must be pulled to VDDIO through an external pull-up resistor.
A_{DIFF}	Analog Differential	Analog differential signal pair for twisted pair interface.
A_{BIAS}	Analog Bias	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network, as shown in System Schematic.
NC	No Connect	No connect signal. Must be left floating.

13.6 MAC Transmit Interface Pins (MAC TX)

Table 13-2. MAC TX Signal Descriptions (Sheet 1 of 2)

BGA Ball	Signal Name MAC Interface Mode					Type	Description
	TBI	RTBI	GMII	MII	RGMII		
AE3 AF3 AD5 AE4	TX[3:0]_3	TD[8:5]_3 and TD[3:0]_3	TXD[3:0]_3	TXD[3:0]_3	TD[7:4]_3 and TD[3:0]_3	I_{PD}	**Transmit Data Inputs (All modes).** Transmit code-group data is input on these pins synchronously to GTX_CLK_n in GMII mode, TXC_n in RGMII/RTBI modes, or PMA_TX_CLK_n in TBI mode. **Multiplexed Transmit Data Nibbles (RTBI mode).** Bits [3:0] are synchronously input on the rising edge of TXC_n, and bits [8:5] on the falling edge of TXC_n. **Multiplexed Transmit Data Nibbles (RGMII mode).** Bits [3:0] are synchronously input on the rising edge of TXC_n, and bits [7:4] on the falling edge of TXC_n.
AF14 AF15 AE15 AE16	TX[3:0]_2	TD[8:5]_2 and TD[3:0]_2	TXD[3:0]_2	TXD[3:0]_2	TD[7:4]_2 and TD[3:0]_2		
AF25 AE25 AE26 AF26	TX[3:0]_1	TD[8:5]_1 and TD[3:0]_1	TXD[3:0]_1	TXD[3:0]_1	TD[7:4]_1 and TD[3:0]_1		
P26 N26 N25 M25	TX[3:0]_0	TD[8:5]_0 and TD[3:0]_0	TXD[3:0]_0	TXD[3:0]_0	TD[7:4]_0 and TD[3:0]_0		
AF2 AE2 AD3 AD4	TX[7:4]_3	*Not used*	TXD[7:4]_3	*Not used*	*Tie pins to GND*	I_{PD}	**Transmit Data Inputs (TBI mode).** Transmit data is input on these pins synchronously to PMA_TX_CLK_n in TBI mode. **Transmit Data Inputs (GMII mode).** Transmit data is input on these pins synchronously to GTX_CLK_n in GMII mode.
AF12 AF13 AE13 AE14	TX[7:4]_2		TXD[7:4]_2				
AD24 AD23 AF24 AE24	TX[7:4]_1		TXD[7:4]_1				
T26 R26 R25 P25	TX[7:4]_0		TXD[7:4]_0				
AF1 AE12 AD22 T25	TX[8]_3 TX[8]_2 TX[8]_1 TX[8]_0	*Not used*	TX_EN_3 TX_EN_2 TX_EN_1 TX_EN_0	TX_EN_3 TX_EN_2 TX_EN_1 TX_EN_0	*Tie pins to GND*	I_{PD}	**Transmit Data Code Group, bit 8 (TBI mode).** **Transmit Enable Input (GMII, MII modes).** Synchronized to the rising edge of GTX_CLK_n (1000Mb mode) or TX_CLK_n (100Mb mode), this input indicates valid data is present on the TXD bus.

Table 13-2. MAC TX Signal Descriptions (Sheet 2 of 2)

BGA Ball	Signal Name MAC Interface Mode					Type	Description
	TBI	RTBI	GMII	MII	RGMII		
AE1 AE11 AE23 U25	TX[9]_3 TX[9]_2 TX[9]_1 TX[9]_0	TD[9]_3 and TD[4]_3 TD[9]_2 and TD[4]_2 TD[9]_1 and TD[4]_1 TD[9]_0 and TD[4]_0	TX_ER_3 TX_ER_2 TX_ER_1 TX_ER_0	TX_ER_3 TX_ER_2 TX_ER_1 TX_ER_0	TX_CTL_4 TX_CTL_3 TX_CTL_2 TX_CTL_1	I_{PD}	**Transmit Data Code Group, bit [9] (TBI mode).** **Multiplexed Transmit Data (RTBI mode).** Bit [4] is synchronously input on the rising edge of TXC_n, and bit [9] on the falling edge of TXC_n. **Transmit Error Input (GMII, MII modes).** When asserted, this synchronous input causes error symbols to be transmitted from the PHY when operating in 1000Mb or 100Mb modes. **Transmit Enable, Transmit Error Multiplexed Input (RGMII mode).** In RGMII mode, this input is sampled by the PHY on opposite edges of TXC_n to indicate two transmit conditions of the MAC: 1) On the rising edge of TXC_n, this input serves as TXEN, indicating valid data is available on the TD input data bus. 2) On the falling edge of TXC_n, this input signals a transmit error from the MAC based on a logical derivative of TXEN and TXERR, per RGMII Specification v1.2a (section 3.4).
AD2 AF11 AF23 U26	PMA_TX_ CLK_3 PMA_TX_ CLK_2 PMA_TX_ CLK_1 PMA_TX_ CLK_0	TXC_3 TXC_2 TXC_1 TXC_0	GTX_CLK_3 GTX_CLK_2 GTX_CLK_1 GTX_CLK_0	*Not used*[1]	TXC_3 TXC_2 TXC_1 TXC_0	I_{PD}	**PMA Transmit Code-Group Clock Input (TBI mode).** 125MHz transmit code-group clock. This code-group clock is used to latch data into the PMA (in this case, the PHY) for transmission. PMA_TX_CLK_n is also used by the transmitter clock multiplier unit to generate the 1250MHz bit rate clock. PMA_TX_CLK_n has a ±100ppm tolerance and is derived from GMII GTX_CLK_n. **Transmit Clock Input (RTBI mode).** The transmit clock is 125MHz with a ±50ppm tolerance. **Transmit Clock Input (GMII mode).** The transmit clock GTX_CLK_n is a 125MHz ±100ppm reference clock used to synchronize the TXD data code group, TXD[7:0], into the PCS. **Transmit Clock Input (RGMII mode).** The transmit clock shall be either a 125MHz (1000Mb) or 25MHz (100Mb/10Mb) with a ±50ppm tolerance.

[1] See TX_CLK pin description in following section.

13.7 MAC Receive Interface Pins (MAC RX)

All output pins for the MAC interface include impedance-calibrated, tristate-able output drive capability.

Table 13-3. MAC RX Signal Descriptions (Sheet 1 of 3)

<table>
<tr><th rowspan="2">BGA Ball</th><th colspan="5">Signal Name
MAC Interface Mode</th><th rowspan="2">Type</th><th rowspan="2">Description</th></tr>
<tr><th>TBI</th><th>RTBI</th><th>GMII</th><th>MII</th><th>RGMII</th></tr>
<tr><td>AB2
AC1
AC2
AD1</td><td>RX[3:0]_3</td><td>RD[8:5]_3
and
RD[3:0]_3</td><td>RXD[3:0]_3</td><td>RXD[3:0]_3</td><td>RD[7:4]_3
and
RD[3:0]_3</td><td rowspan="4">O_{ZC}</td><td rowspan="4">Receive Data Code Group (TBI mode). Part of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by PMA_RX_CLK1_n.

Multiplexed Receive Data Nibbles (RTBI mode). Bits [3:0] are synchronously input on the rising edge of RXC_n, and bits [8:5] on the falling edge of RXC_n.

Receive Data Code Group (GMII, MII modes). Receive data is driven out of the device synchronously to the rising edge of RX_CLK_n. RXD[3]_n is the MSB; RXD[0]_n is the LSB.

Multiplexed Receive Data Nibbles (RGMII mode). Bits [3:0] are synchronously output on the rising edge of RXC_n, and bits [7:4] on the falling edge of RXC_n.</td></tr>
<tr><td>AE9
AF9
AE10
AF10</td><td>RX[3:0]_2</td><td>RD[8:5]_2
and
RD[3:0]_2</td><td>RXD[3:0]_2</td><td>RXD[3:0]_2</td><td>RD[7:4]_2
and
RD[3:0]_2</td></tr>
<tr><td>AE21
AF22
AE22
AD21</td><td>RX[3:0]_1</td><td>RD[8:5]_1
and
RD[3:0]_1</td><td>RXD[3:0]_1</td><td>RXD[3:0]_1</td><td>RD[7:4]_1
and
RD[3:0]_1</td></tr>
<tr><td>W25
W26
V25
V26</td><td>RX[3:0]_0</td><td>RD[8:5]_0
and
RD[3:0]_0</td><td>RXD[3:0]_0</td><td>RXD[3:0]_0</td><td>RD[7:4]_0
and
RD[3:0]_0</td></tr>
<tr><td>Y1
AA1
AA2
AB1</td><td>RX[7:4]_3</td><td rowspan="4">Leave pins unconnected</td><td>RXD[7:4]_3</td><td rowspan="4">Not used</td><td rowspan="4">Leave pins unconnected</td><td rowspan="4">O_{ZC}</td><td rowspan="4">Receive Data Code Group (TBI mode). Part of 10-bit parallel receive code-group data. When code groups are properly aligned, any received code group containing a comma is clocked by PMA_RX_CLK1_n.

Receive Data Code Group (GMII mode). Receive data is driven out of the device synchronously to the rising edge of RX_CLK_n. RXD[7]_n is the MSB.

In MII, RGMII, and RTBI modes, these pins are not used.</td></tr>
<tr><td>AE7
AF7
AE8
AF8</td><td>RX[7:4]_2</td><td>RXD[7:4]_2</td></tr>
<tr><td>AF19
AF20
AE20
AF21</td><td>RX[7:4]_1</td><td>RXD[7:4]_1</td></tr>
<tr><td>AA26
AA25
Y25
Y26</td><td>RX[7:4]_0</td><td>RXD[7:4]_0</td></tr>
<tr><td>W2
AD6
AF18
AC25</td><td>PMA_RX_CLK0_3
PMA_RX_CLK0_2
PMA_RX_CLK0_1
PMA_RX_CLK0_0</td><td>RXC_3
RXC_2
RXC_1
RXC_0</td><td>RX_CLK_3
RX_CLK_2
RX_CLK_1
RX_CLK_0</td><td>RX_CLK_3
RX_CLK_2
RX_CLK_1
RX_CLK_0</td><td>RXC_3
RXC_2
RXC_1
RXC_0</td><td>O_{ZC}</td><td>PMA Receiver Clock 0 Output (TBI mode). The 62.5MHz receive clock that the protocol device (MAC) uses to latch odd-numbered code groups in the received PHY bit stream. This clock may be stretched during code-group alignment and is not shortened.

Receive Clock Output (GMII, MII, and RGMII/RTBI modes). Receive data is sourced from the PHY synchronously on the rising edge of RX_CLK_n in GMII/MII modes, or RXC_n in RGMII/RTBI modes, and is the recovered clock from the media.</td></tr>
</table>

Table 13-3. MAC RX Signal Descriptions (Sheet 2 of 3)

BGA Ball	Signal Name MAC Interface Mode					Type	Description
	TBI	RTBI	GMII	MII	RGMII		
V2 AE5 AE17 AC26	PMA_RX_CLK1_3 PMA_RX_CLK1_2 PMA_RX_CLK1_1 PMA_RX_CLK1_0	*Leave pins unconnected*	*Leave pins unconnected*	TX_CLK_3 TX_CLK_2 TX_CLK_1 TX_CLK_0	*Leave pins unconnected*	O_{ZC}	**PMA Receiver Clock 1 Output (TBI mode).** The 62.5MHz receive clock that the protocol device (MAC) uses to latch even-numbered code groups in the received PHY bit stream. PMA_RX_CLK1_n is 180° out of phase with PMA_RX_CLK0_n. This clock may be stretched during code-group alignment and is not shortened. **Transmit Clock (MII mode).** 25MHz MII clock output used to synchronize TXD data in 100Mb mode, or 2.5MHz MII output clock to synchronize TXD data in 10Mb mode. *In GMII, RGMII, and RTBI modes, these pins should be left unconnected since they are not used.*
Y2 AF6 AE19 AB26	RX[8]_3 RX[8]_2 RX[8]_1 RX[8]_0	*Leave pins unconnected*	RX_DV_3 RX_DV_2 RX_DV_1 RX_DV_0	RX_DV_3 RX_DV_2 RX_DV_1 RX_DV_0	*Leave pins unconnected*	O_{ZC}	**Receive Data Code Group, bit [8] (TBI mode).** **Receive Data Valid Output (GMII, MII modes).** RX_DV_n is asserted by the PHY to indicate that the PHY is presenting recovered and decoded data on the RXD[7:0]_n pins. RX_DV_n is synchronous with respect to RX_CLK_n. *In RGMII and RTBI modes, these output pins should be left unconnected since they are not used.*
W1 AE6 AE18 AB25	RX[9]_3 RX[9]_2 RX[9]_1 RX[9]_0	RD[9]_3 and RD[4]_3 RD[9]_2 and RD[4]_2 RD[9]_1 and RD[4]_1 RD[9]_0 and RD[4]_0	RX_ER_3 RX_ER_2 RX_ER_1 RX_ER_0	RX_ER_3 RX_ER_2 RX_ER_1 RX_ER_0	RX_CTL_3 RX_CTL_2 RX_CTL_1 RX_CTL_0	O_{ZC}	**Receive Data Code Group, bit [9] (TBI mode).** **Multiplexed Receive Data (RTBI mode).** Bit [4] is synchronously input on the rising edge of RXC_n, and bit [9] on the falling edge of RXC_n. **Receiver Error Output (GMII, MII modes).** This active high output is synchronous to the received data clock (RX_CLK_n). For 1000Mb mode, this signal is asserted when error symbols or carrier extension symbols are received; in 100Mb mode, it is asserted when error symbols are received. **Multiplexed Receive Data Valid / Receive Error Output (RGMII mode).** In RGMII mode, this output is sampled by the MAC on opposite edges of RXC_n to indicate two receive conditions from the PHY: 1) on the rising edge of RXC_n, this output serves as RXDV, signaling valid data is available on the RD input data bus. 2) on the falling edge of RXC_n, this output signals a receive error from the PHY based on a logical derivative of RXDV and RXERR, per RGMII Specification v1.2a (section 3.4).
U1 AF4 AF16 AD25	COM_DET_3 COM_DET_2 COM_DET_1 COM_DET_0	*Leave pins unconnected*	CRS_3 CRS_2 CRS_1 CRS_0	CRS_3 CRS_2 CRS_1 CRS_0	*Leave pins unconnected*	O_{ZC}	**Comma Detect Output (TBI mode).** An indication that the code group associated with the current PMA_RX_CLK1_n contains a valid comma. The TBI in the CIS8204 detects and code-group-aligns to the comma+ bit sequence. **Carrier Sense Output (GMII, MII modes).** CRS_n is asserted high when a valid carrier is detected on the media.

Table 13-3. MAC RX Signal Descriptions (Sheet 3 of 3)

BGA Ball	Signal Name MAC Interface Mode					Type	Description
	TBI	RTBI	GMII	MII	RGMII		
V1 AF5 AF17 AD26	RX_CLK125_3 RX_CLK125_2 RX_CLK125_1 RX_CLK125_0	*Leave pins unconnected*	COL_3 COL_2 COL_1 COL_0	COL_3 COL_2 COL_1 COL_0	*Leave pins unconnected*	O_{ZC}	**Receiver Clock 125MHz Output (TBI mode).** This signal behaves differently, depending on whether TBI loopback mode is enabled: 1) When TBI loopback mode is enabled (see MII Register bit 23.7), RX_CLK125_n becomes one-half the frequency of the GTX_CLK_n input clock from the protocol device (or MAC). 2) When no carrier is present on the media, this signal is the same as the device's free running output clock signal, CLK125. 3) When a valid carrier is detected on the media, this output signal is the recovered clock from the TBI's data stream. When switching from one of these three operating modes to another, RX_CLK125_n's low time will be extended, if necessary, to avoid clock glitching. **Collision Detect Output (GMII, MII modes).** This output is asserted high when a collision is detected on the media. For full-duplex modes, this output is driven low.

13.8 Twisted Pair Interface Pins (TPI)

Table 13-4. TPI Signal Descriptions

BGA Ball	Signal Name	Type	Description
B6 B14 B22 F26	TXIP_A_3 TXIP_A_2 TXIP_A_1 TXIP_A_0	A_{DIFF}	**TX/RX Channel "A" Positive Hybrid Pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "A" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1. See Figure 13-4.
A6 A14 A22 E26	TXVP_A_3 TXVP_A_2 TXVP_A_1 TXVP_A_0		
A5 A13 A21 E25	TXVN_A_3 TXVN_A_2 TXVN_A_1 TXVN_A_0	A_{DIFF}	**TX/RX Channel "A" Negative Hybrid Pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "A" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2. See Figure 13-4.
B5 B13 B21 F25	TXIN_A_3 TXIN_A_2 TXIN_A_1 TXIN_A_0		
B4 B12 B20 D26	TXIP_B_3 TXIP_B_2 TXIP_B_1 TXIP_B_0	A_{DIFF}	**TX/RX Channel "B" Positive Hybrid Pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "B" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3. See Figure 13-4.
A4 A12 A20 C26	TXVP_B_3 TXVP_B_2 TXVP_B_1 TXVP_B_0		
A3 A11 A19 C25	TXVN_B_3 TXVN_B_2 TXVN_B_1 TXVN_B_0	A_{DIFF}	**TX/RX Channel "B" Negative Hybrid Pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "B" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6. See Figure 13-4.
B3 B11 B19 D25	TXIN_B_3 TXIN_B_2 TXIN_B_1 TXIN_B_0		
B2 B10 B18 B26	TXIP_C_3 TXIP_C_2 TXIP_C_1 TXIP_C_0	A_{DIFF}	**TX/RX Channel "C" Positive Hybrid Pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "C" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10M/100M modes). See Figure 13-4.
A2 A10 A18 A26	TXVP_C_3 TXVP_C_2 TXVP_C_1 TXVP_C_0		
A1 A9 A17 A25	TXVN_C_3 TXVN_C_2 TXVN_C_1 TXVN_C_0	A_{DIFF}	**TX/RX Channel "C" Negative Hybrid Pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "C" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10M/100M modes). See Figure 13-4.
B1 B9 B17 B25	TXIN_C_3 TXIN_C_2 TXIN_C_1 TXIN_C_0		
D2 B8 B16 B24	TXIP_D_3 TXIP_D_2 TXIP_D_1 TXIP_D_0	A_{DIFF}	**TX/RX Channel "D" Positive Hybrid Pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "D" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10M/100M modes). See Figure 13-4.
C2 A8 A16 A24	TXVP_D_3 TXVP_D_2 TXVP_D_1 TXVP_D_0		
C1 A7 A15 A23	TXVN_D_3 TXVN_D_2 TXVN_D_1 TXVN_D_0	A_{DIFF}	**TX/RX Channel "D" Negative Hybrid Pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "D" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10M/100M modes). See Figure 13-4.
D1 B7 B15 B23	TXIN_D_3 TXIN_D_2 TXIN_D_1 TXIN_D_0		

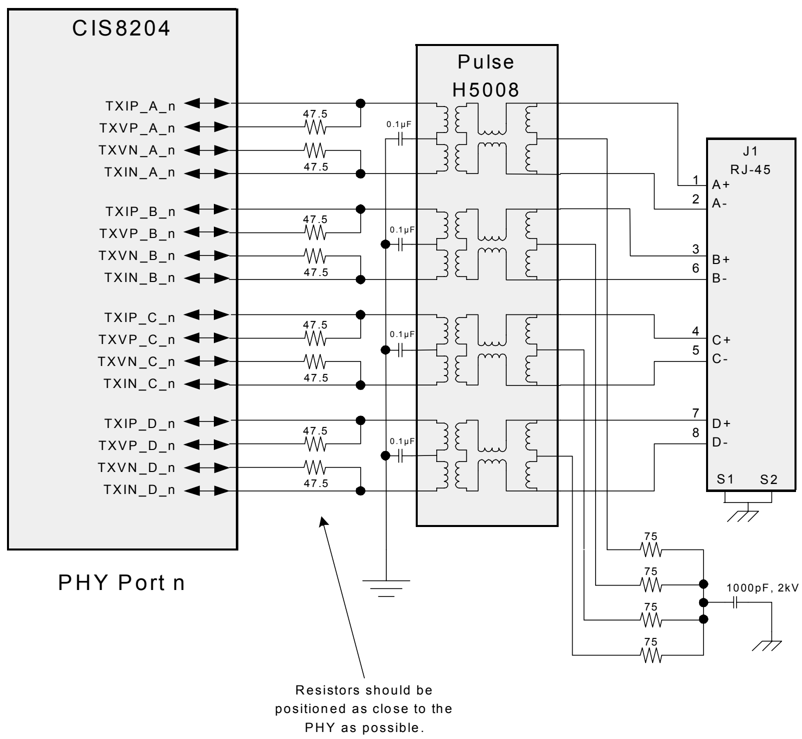

Figure 13-4. CIS8204 Twisted Pair Interface (per PHY port)

13.9 Serial Management Interface Pins (SMI)

Table 13-5. SMI Signal Descriptions

BGA Ball	Signal Name	Type	Description
R1	MDC	I	**Management Data Clock.** A 0 to 25MHz reference input used to clock serial MDIO data into and out of the CIS8204. The expected nominal frequency is 2.5MHz, as specified by the IEEE standard. This clock is typically asynchronous with respect to the PHY's transmit or receive clock.
P2	MDIO	I/O	**Management Data I/O.** MDIO configuration and status data is exchanged on this pin bidirectionally between the PHY and the Station Manager, synchronously to the rising edge of MDC. This pin normally requires a 1.5kΩ to 2kΩ external pull-up resistor at the Station Manager. The value of the pull-up resistor depends on the MDC clock frequency and the maximum capacitive load on the MDIO pin.
R2	MDINT#	OD	**Management Interrupt Output.** This open drain, active low output signal indicates a change in any of the four PHY's link operating conditions for which a station manager must interrogate to determine further information. See MII Registers 25 (bit 15) and 26 (bit 15) for more information. This pin should be pulled up to VDDIO at the Station Manager or controller through an external 2.2kΩ pull-up resistor.
N1 N2 P1	PHYADD[4] PHYADD[3] PHYADD[2]	$I_{PD}/(O_{ZC})$[1]	**PHY Address Bus Input.** These inputs are the three uppermost bits of the 5-bit IEEE-specified PHY address. The states of these three pins are latched during power-up, or a hardware or software reset. The lower two bits, [1:0], of the 5-bit PHY address are hard-wired to each of the four PHY ports within the device.

[1] In normal operating mode, these three pins are used as inputs only. However, for manufacturing test purposes, these pins are used as digital output pins.

13.10 Configuration and Control Pins (Config)

Table 13-6. Config Signal Descriptions (Sheet 1 of 2)

BGA Ball	Signal Name	Type	Description
T1	RESET#	I	**Hardware Chip Reset.** Active low input which resets each of the PHY's MII Management Register Set bits to their default reset states. See MII Register bit 0.15 for more information.
T2	PWDN	I_{PD}	**Chip Power-Down.** Active high input forces entire device into lowest power operating mode. All four PHYs are deactivated.

Table 13-6. Config Signal Descriptions (Sheet 2 of 2)

BGA Ball	Signal Name	Type	Description
M2, L2 K1, K2 J1, H1 G1, G2 M1 L1 J2 H2	MODE[1:0]_3 MODE[1:0]_2 MODE[1:0]_1 MODE[1:0]_0 DUPLEX_3 DUPLEX_2 DUPLEX_1 DUPLEX_0	I_{PU}/(O_{ZC})[1]	**Force Advertised Operating Mode.** Used in conjunction with the DUPLEX_n pin, the MODE[1:0]_n inputs force or preset each PHY's advertised link capabilities (speed, duplex, and MASTER/SLAVE). The states of these pins are not latched; any change in the states of these pins will cause the PHY to restart the auto-negotiation sequence. MODE[1]_n / MODE[0]_n / DUPLEX_n / Advertised operating mode: 0 / 0 / 0 / 10BASE-T, HALF duplex 0 / 0 / 1 / 10BASE-T, FULL duplex 0 / 1 / 0 / 100BASE-TX, HALF duplex 0 / 1 / 1 / 100BASE-TX, FULL duplex 1 / 0 / 0 / 1000BASE-T, force SLAVE timing mode 1 / 0 / 1 / 1000BASE-T, force MASTER timing mode 1 / 1 / X / Normal operating mode. Allow all PHY characteristics to be determined by the MII register settings and the Auto-Negotiation or Parallel-Detect processes. Notes: 1) These pins are not intended to be used during normal operating modes. They are primarily intended for use in designs that may not include a station manager, or for PHY characterization testing. 2) Regardless of the states of the MODE and DUPLEX pins, the Auto-Negotiation and Parallel-Detect processes will always be performed, unless the user disables Auto-Negotiation by writing a "0" to MII Register bit 0.12 3) The priority of the MODE and DUPLEX pins versus the MII register settings may be changed by writing the MODE/DUPLEX Pin Priority Select bit (MII Register bit 28.2). 4) If the Auto-Negotiation or Parallel-Detect processes do not result in a link operating mode that matches that specified by the MODE and DUPLEX pins, the link will NOT be established. The PHY will enter the "link_fail" state. 3) Since these pins include on-chip pull-ups, these pins may be left unconnected for designs which do not require this functionality.

[1] In normal operating mode, these twelve pins are used as inputs only. However, for manufacturing test purposes, these pins are used as digital output pins.

13.11 System Clock Interface Pins (SCI)

Table 13-7. SCI Signal Descriptions

BGA Ball	Signal Name	Type	Description
F2	REFCLK	I	**PHY Reference Clock Input / Crystal Input.** The reference input clock can either be a 25MHz or 125MHz reference clock, with a ±50ppm frequency tolerance.
F1	PLLMODE	I_{PD}/(O_{ZC})[1]	**PLL Mode Select.** Pin is sampled during the device power-up sequence. When PLLMODE is high, indicates to PLL that a 125MHz clock input is used as PHY reference clock. When pulled low, indicates to the PLL that the reference clock is a 25MHz reference. In output mode, this pin is also used for manufacturing test purposes only.
U2	CLK125	O_{ZC}	**125MHz Reference Clock Output.** A general purpose, free-running, low jitter, reference clock output, regenerated either from the 25MHz or 125MHz clock reference supplied on REFCLK input pin. This output pin is enabled (toggling) by default. See MII Register bit 18.0 and 18.8 for more information.

[1] In normal operating mode, this pin is used as an input only. However, for manufacturing test purposes, this pin is used as a digital output pin.

13.12 Serial LED Interface Pins (SLI)

Table 13-8. SLI Signal Descriptions

BGA Ball	Signal Name	Type	Description
L26	LED_CLK	O_{ZC}	**Serial LED Clock Output.** Reference output clock for Serial LED Interface.
M26	LED_DATA	O_{ZC}	**Serial LED Data Output.** Serial bit stream containing a maximum of 9 bits (per PHY) of link status information (duplex, Link10/100/1000, link quality, activity, transmit, receive, collision). Data is clocked out continuously at a rate of approximately 1MHz. Data is valid on the rising edge of LED_CLK clock output. See Section 17: "Serial LED Interface" for more information.

13.13 JTAG Test Access Port (TAP)

Table 13-9. JTAG TAP Signal Descriptions

BGA Ball	Signal Name	Type	Description
J26	TDI	$I_{PU(5V)}$	**JTAG Test Data Serial Input Data.** Serial test pattern data is scanned into the device on this input pin, which is sampled with respect to the rising edge of TCK. This pin should be tied high during normal chip operation.
K26	TDO	O_{ZC}	**JTAG Test Data Serial Output Data.** Serial test data from the CIS8204 is driven out of the device on the falling edge of TCK. This pin should be left floating during normal chip operation.
K25	TMS	$I_{PU(5V)}$	**JTAG Test Mode Select.** This input pin, sampled on the rising edge of TCK, controls the TAP (Test Access Port) controller's 16-state, instruction state machine. This pin should be tied high during normal chip operation.
L25	TCK	$I_{PU(5V)}$	**JTAG Test Clock.** This input pin is the master clock source used to control all JTAG test logic in the device. This pin should be tied low during normal chip operation.
J25	TRST#	$I_{PU(5V)}$	**JTAG Reset.** This active low input pin serves as an asynchronous reset to the JTAG TAP controller's state machine. As required by the JTAG standard, this pin includes an integrated on-chip pull-up resistor. Alternatively, if the JTAG port of the CIS8204 is *not* used on the printed circuit board, then this pin should be tied to ground (VSSIO) with a pull-down resistor.

13.14 Analog Bias Pins (AP)

Table 13-10. AP Signal Descriptions

BGA Ball	Signal Name	Type	Description
G26	REF_REXT	A_{BIAS}	**Bias** pin to external 2.26kΩ (1%) resistor tied to analog ground.
G25	REF_FILT	A_{BIAS}	**Reference Generator Filter** pin to external 1µF (±10%) capacitor tied to analog ground.
H23	VREFP[1]	A_{BIAS}	**Positive Voltage Bias.** Analog reference generator positive supply input. VREFP should be tied to analog V+A33 supply with a short signal trace. A 1µF capacitor should be placed between VREFP and VREFN, as close to the device package as possible.
H26	VREFN	A_{BIAS}	**Negative Voltage Bias.** Reference filter ground. Must be tied with a short trace to the bottom of the REF_FILT capacitor, and then to GND.

[1] VREFP supplies the analog voltage reference circuitry. Careful attention to the PCB layout for this supply pin must be observed in order to avoid any bus drops, which would cause voltage inaccuracy in the voltage reference generator. Separate traces for VREFP and VREFN to the 3.3V supply regulator and ground, respectively, are recommended. See Applications Note "CIS8204 Design and Layout Guidelines" for more information.

13.15 No Connects (NC)

Table 13-11. NC Signal Descriptions

BGA Ball	Signal Name	Type	Description
E1	TANA_3	NC	Do not connect these pins. They are used only in IC manufacturing test. Leave all ‘no connect’ pins floating during normal operation.
E2	TANA_2		
D24	TANA_1		
E24	TANA_0		
C23	NC		
C24	NC		
D23	NC		
E23	NC		
H25	NC		

13.16 Digital Power Supply Pins

Table 13-12. Digital Power Supply Signal Descriptions (Sheet 1 of 2)

HS-BGA Ball	HS-BGA Supply Name	Recommended PCB Power Plane Assignment	Type	Nominal Supply Voltage (V)	Description
Digital I/O Power Pins					
J4, L4 N4, U4 W4, AA4 AB4 AC4, AC5 AC6, AC8 AC10, AC12 L23 N23, U23 W23, AA23 AC14, AC16 AC18, AC20 AC22, AC23 AB23	VDDIO	V+IO	P	3.3 or 2.5	I/O power supply (3.3V for GMII or TBI modes, or 2.5V for RGMII or RTBI modes).
J3, L3 N3, U3 W3, AA3 AB3, AC3 AD8 AD10, AD12 AB24, AC24 G24, L24 N24, U24 W24, AA24 AD14, AD16 AD18, AD20	VSSIO	GND	G	0	I/O ground (0V).
Digital Core Power Pins					
H4, K4 M4, P4 R4, T4 V4, Y4 AC7, AC9 AC11, AC13 F23 M23, P23 R23, T23 V23, Y23 AC15, AC17 AC19, AC21	VDDDIG	V+DIG	P	1.5	Core power supply
H3, K3 M3, P3 R3, T3 V3, Y3 AD7, AD9 AD11, AD13 F24 M24, P24 R24, T24 V24, Y24 AD15, AD17 AD19	VSSDIG	GND	G	0	Core ground (0V). Also see thermal balls (below).

Table 13-12. Digital Power Supply Signal Descriptions (Sheet 2 of 2)

HS-BGA Ball	HS-BGA Supply Name	Recommended PCB Power Plane Assignment	Type	Nominal Supply Voltage (V)	Description
L11, L12 L13, L14 L15, L16 M11, M12 M13, M14 M15, M16 N11, N12 N13, N14 N15, N16 P11, P12 P13, P14 P15, P16 R11, R12 R13, R14 R15, R16 T11, T12 T13, T14 T15, T16	VSSDIG	GND	G	0	Core ground (0V). *These 36 balls also serve as thermal vias to enhance thermal performance of the HS-BGA package. To achieve optimal thermal performance, certain PCB layout guidelines should be followed. Please refer to the "CIS8204 Design and Layout Applications Note" for more information.*

13.17 Analog Power Supply Pins

Table 13-13. Analog Power Supply Signal Descriptions

HS-BGA Ball	HS-BGA Supply Name	Recommended PCB Power Plane Assignment	Type	Nominal Supply Voltage (V)	Description
Analog I/O Power Pins					
C4, D5 D6, D7 D8, D9 D10, D11 D15, D16 D17, D18 D19, D20 D21, D22	VDDLD	V+A33	P	3.3	Line driver 3.3V power supply.
C3, C5 C6, C7 C8, C9 C10, C11 C15, C16 C17, C18 C19, C20 C21, C22	VSSLD	GND	G	0	Line driver ground (0V).
Analog Core Power Pins					
D4, D12 D14, G23	VDDREC	V+A33	P	3.3	Analog receive 3.3V power supply.
D3, C12 C14	VSSREC	GND	G	0	Analog receive ground (0V).[1]
H24	VSSREF	GND	G	0	Reference generator ground.
F4, G4 K23, J23	VDD15	V+A15	P	1.5	PHY port-specific analog power supply for ADCs.
F3, G3 K24, J24	VSS15	GND	G	0	PHY port-specific ground for ADCs (0V).
E4	VDDPLL33	V+A33	P	3.3	PLL 3.3V supply.
E3	VSSPLL33	GND	G	0	PLL ground.
D13	VDDPLL15	V+A15	P	1.5	PLL 1.5V supply.
C13	VSSPLL15	GND	G	0	PLL ground.

[1] VSSREC_0 does not exist as a device pin.

14 System Schematics

14.1 General System Schematic

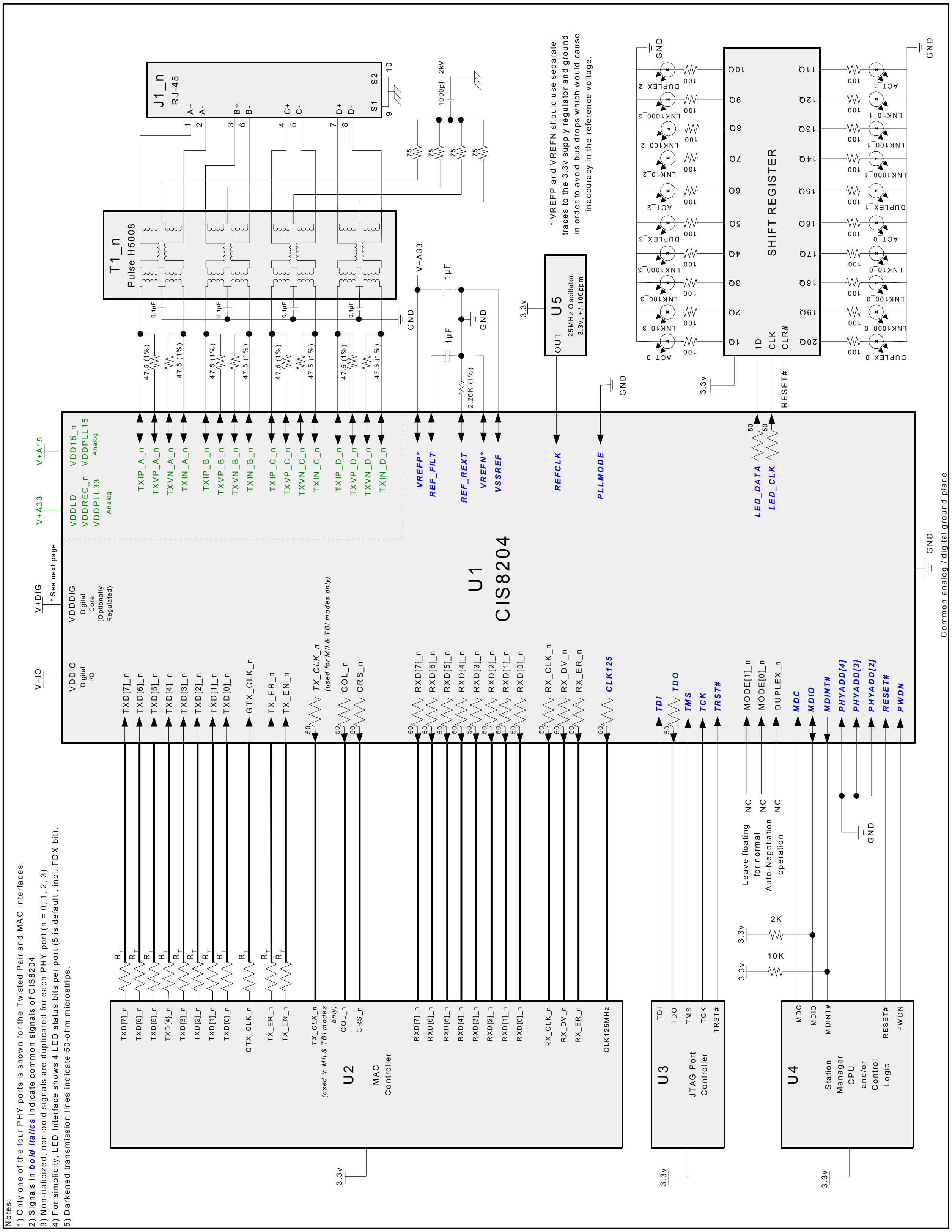

Figure 14-1. General System Schematic (shown with GMII and 3.3V I/O)

14.2 System Schematic – Power Supplies

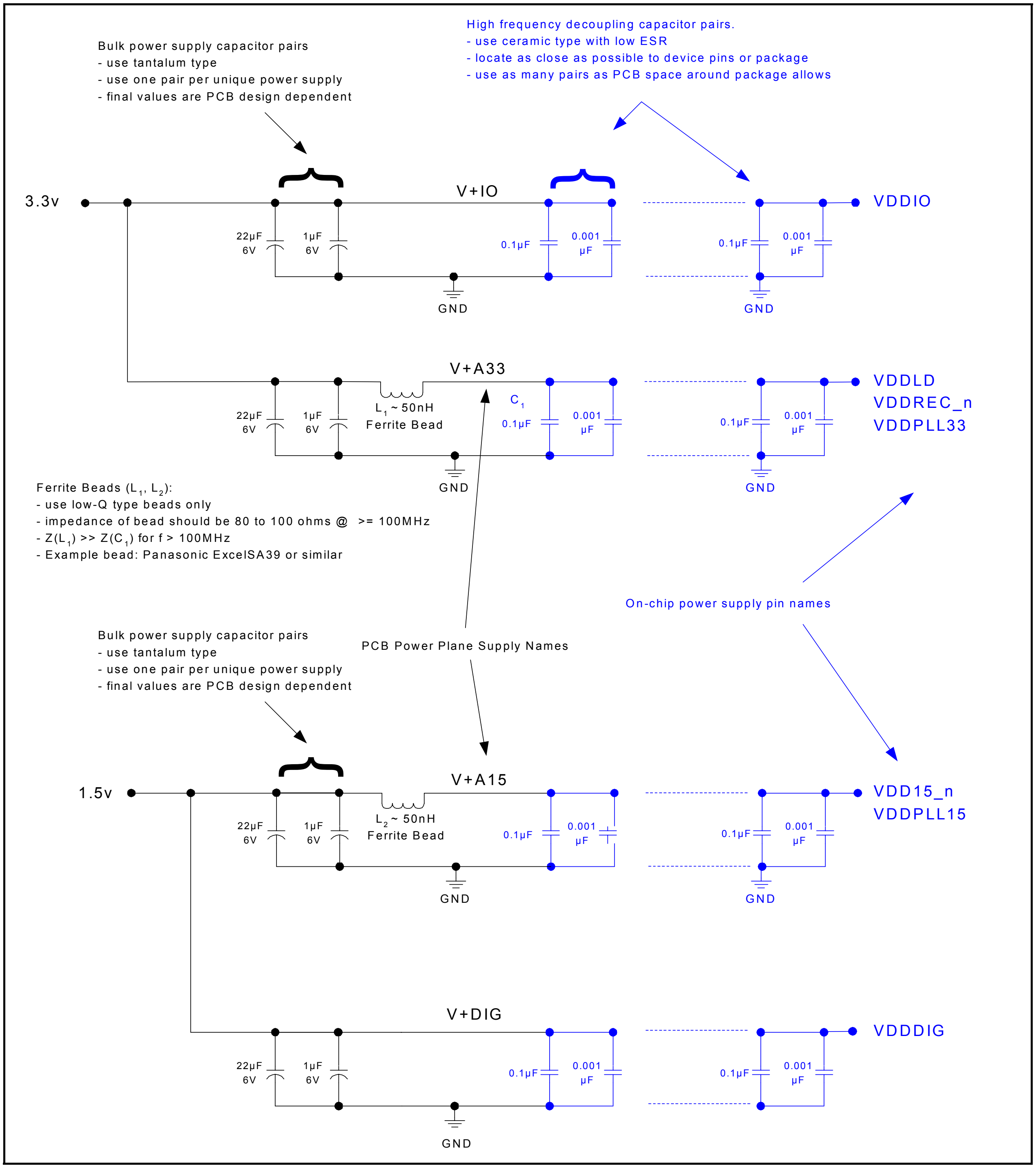

Figure 14-2. Power Supply Connections for a 3.3V I/O Application

15 MAC Interfaces

15.1 GMII MAC I/F

GMII MAC I/F mode, selected by setting the MAC I/F selection bits to GMII/MII mode (Register 23.15:12 = “0000”), clocks data at 125MHz in 1000Mb mode, 25MHz in 100Mb, or 2.5MHz in 10Mb mode. The I/O power supply should be set at 3.3V. See Section 19.6: “MAC I/F Configuration” for more information.

Figure 15-1. GMII MAC Interface

Note:
- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8204 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.

15.2 MII MAC I/F

GMII MAC I/F mode, selected by setting the MAC I/F selection bits to GMII/MII mode (Register 23.15:12 = “0000”), clocks data at 25MHz in 100Mb mode, or 2.5MHz in 10Mb mode. The I/O power supply should be set at 3.3V. See Section 19.6: “MAC I/F Configuration” for more information.

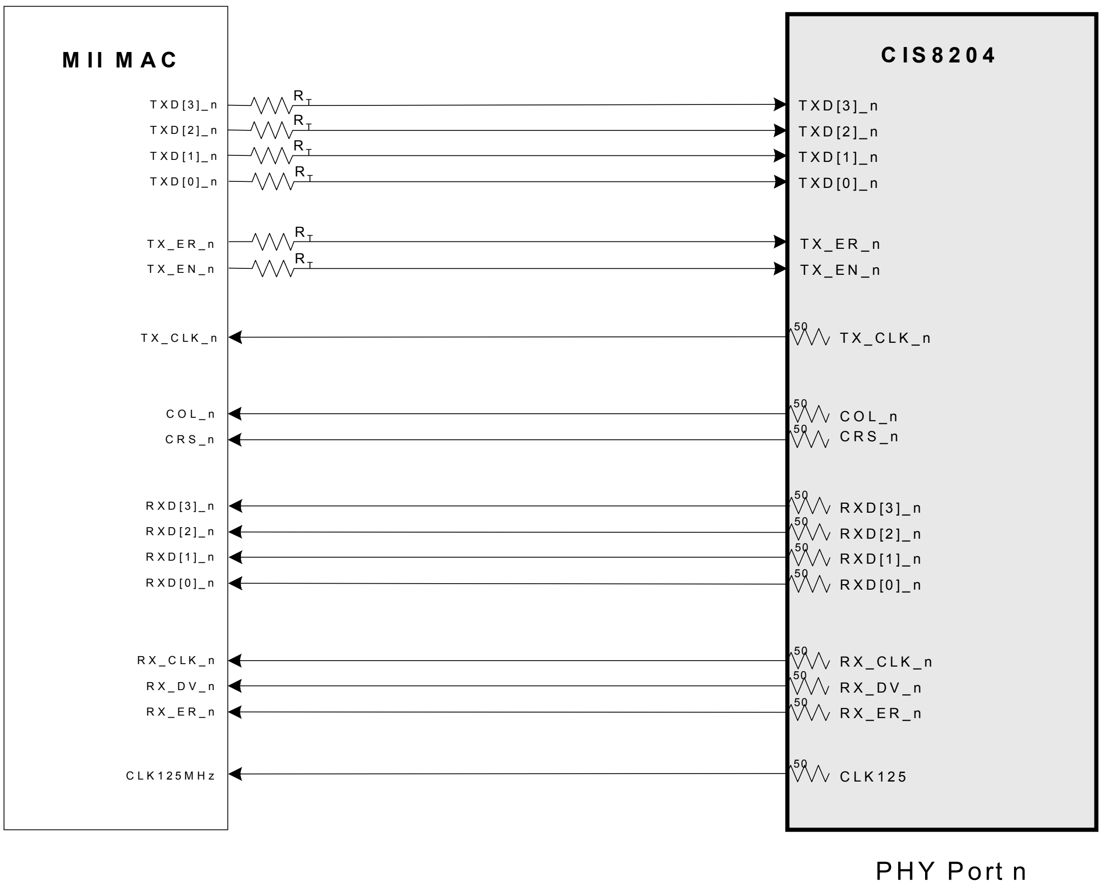

Figure 15-2. MII MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8204 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.

15.3 RGMII MAC I/F

RGMII MAC I/F mode, selected by setting the MAC I/F selection bits to RGMII mode (Register 23.15:12 = “0001”), clocks data at 125MHz in 1000Mb mode, 25MHz in 100Mb mode, or 2.5MHz in 10Mb mode. The I/O power supply should be set at 2.5V. See Section 19.6: “MAC I/F Configuration” for more information.

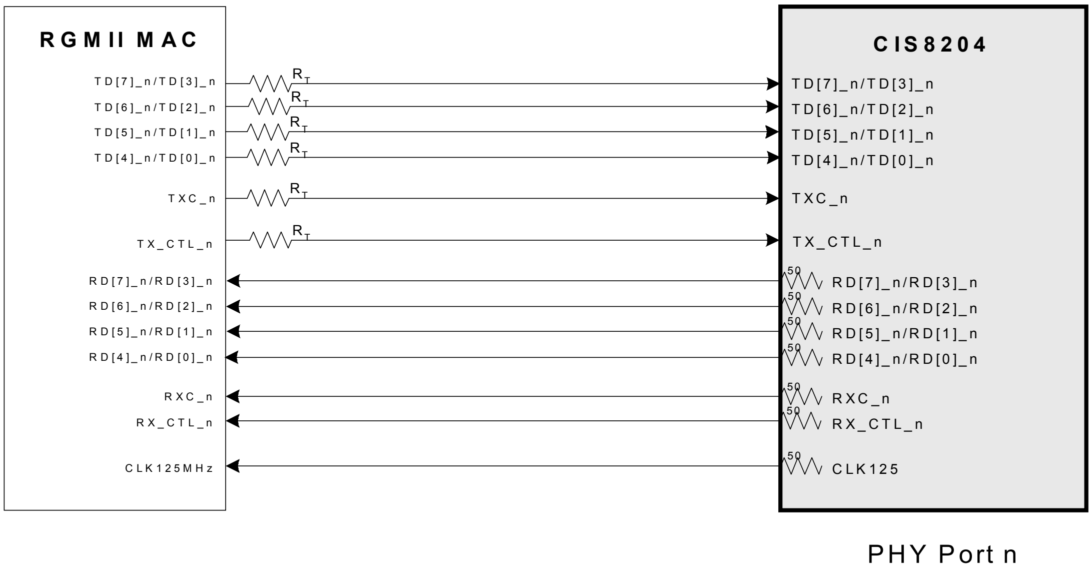

Figure 15-3. RGMII MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8204 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.
- The CIS8204 includes innovative on-chip timing compensation circuitry to simplify PCB design and layout. Please refer to Section 24.9: “RGMII/RTBI Mode Timing” for more information.

15.4 TBI MAC I/F

TBI MAC I/F mode, selected by setting the MAC I/F selection bits to TBI mode (Register 23.15:12 = “0010”), clocks data at 125MHz. The I/O power supply should be set at 3.3V. See Section 19.6: “MAC I/F Configuration” for more information.

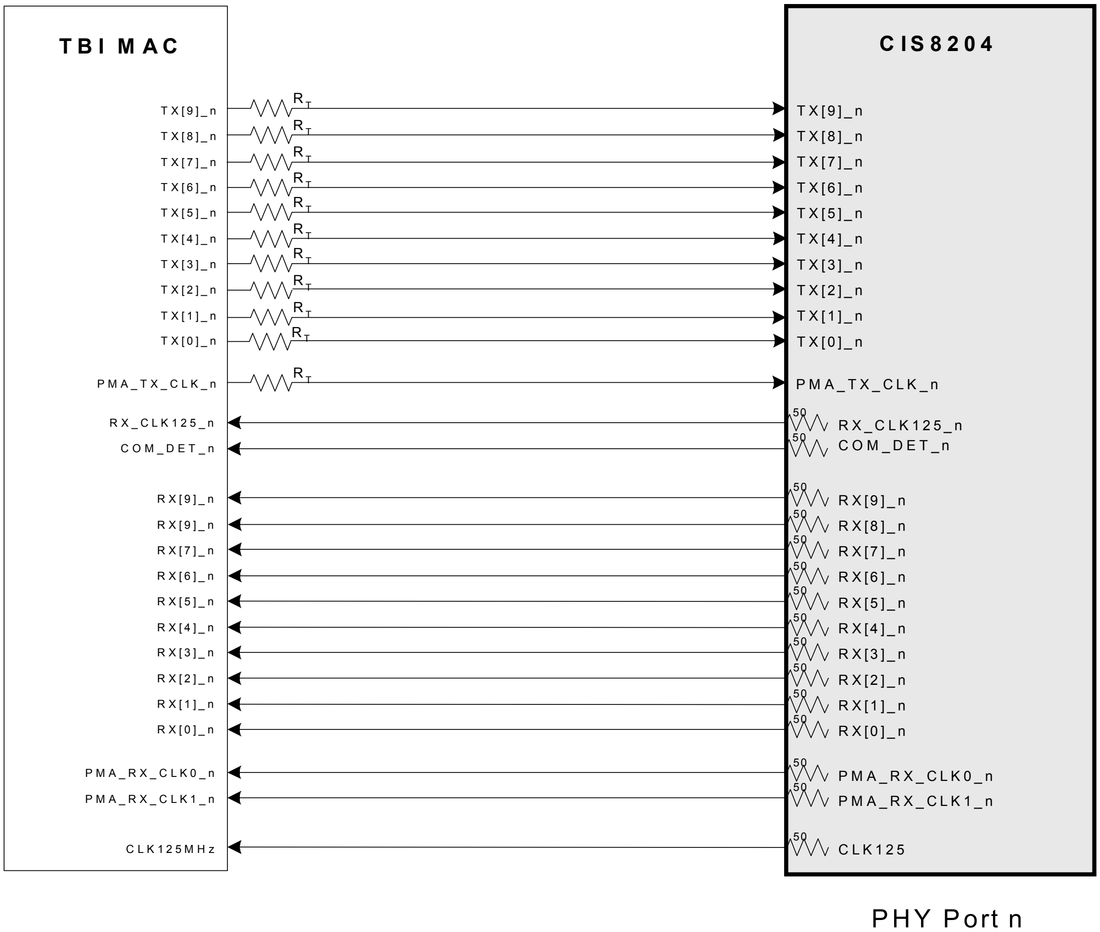

Figure 15-4. TBI MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8204 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.

15.5 RTBI MAC I/F

RTBI MAC I/F mode, selected by setting the MAC I/F selection bits to RTBI mode (Register 23.15:12 = “0011”), clocks data at 125MHz. The I/O power supply should be set at 2.5V. See Section 19.6: “MAC I/F Configuration” for more information.

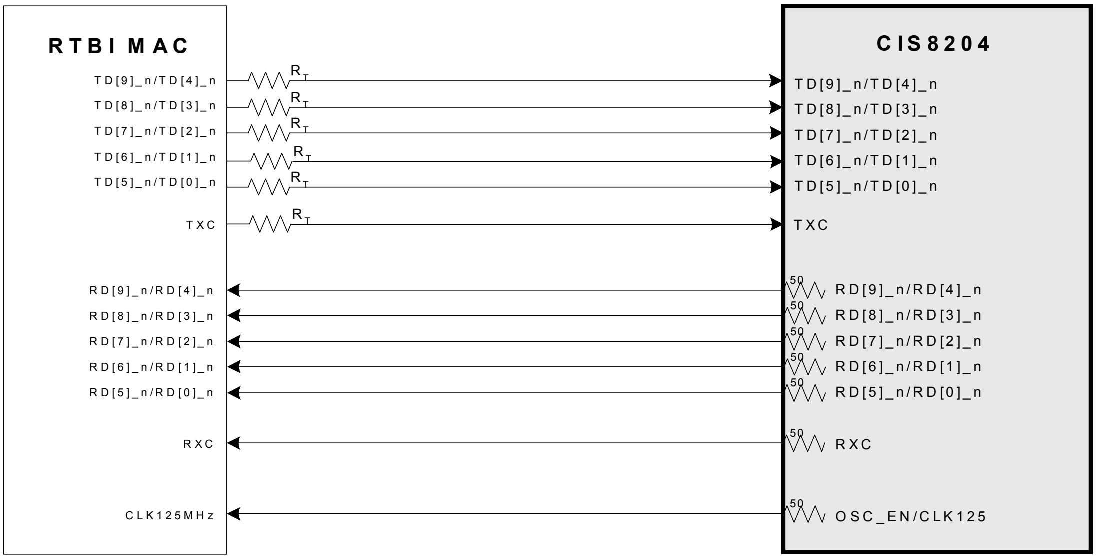

Figure 15-5. RTBI MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the CIS8204 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- Darkened transmission lines indicate 50Ω controlled impedance traces.
- The CIS8204 includes innovative on-chip timing compensation circuitry to simplify PCB design and layout. Please refer to Section 24.9: “RGMII/RTBI Mode Timing” for more information.

16 Serial Management Interface (SMI)

The CIS8204 includes a Serial Management Interface, or “SMI”, that is fully compliant with the IEEE 802.3-2002 specifications. The SMI interface provides access to various status and control registers within the CIS8204. This MII Register set is comprised of a block of thirty-two 16-bit registers. Registers 0 through 10, in addition to Register 15, are required for IEEE compliance. The CIS8204 implements all IEEE-required registers, in addition to several others, providing additional performance-monitoring capabilities. See MII Register Descriptions section section for more information.

The SMI is a two pin, synchronous serial interface, with bidirectional data on MDIO being clocked on the rising edge of MDC. One physical interface (MDIO and MDC) provides access to all four PHYs of the CIS8204. The SMI can be clocked at a rate from 0 to 25MHz, depending on the total load on MDIO.

As many as eight CIS8204s (or thirty-two distinct PHY ports) can share a common SMI signal pair (MDC, MDIO). Thirty-two distinct PHYs can be addressed via the PHYADD[4:2] pins, with address pins PHYADD[1:0] selecting one of the four PHYs in the CIS8204. An external pull-up is required on MDIO; it is typically 2kΩ, but depends on the total load on MDIO.

Data is transferred over the SMI using 32-bit frames with an optional and arbitrary length preamble. The SMI frame format is described in the following table.

Table 16-1. SMI Frame Format

	Direction from CIS8204	Preamble	Start of Frame	Op Code	PHY Address	Register Address	Turn-Around	Data	Idle
# of bits		0+	2	2	5	5	2	16	1+
Read	Output	Z’s	ZZ	ZZ	Z’s	Z’s	Z0	data	Z’s
	Input	1’s	01	10	addr	addr	ZZ	Z’s	Z’s
Write	Output	Z’s	ZZ	ZZ	Z’s	Z’s	ZZ	Z’s	Z’s
	Input	1’s	01	01	addr	addr	10	data	Z’s

- Idle: During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical “1” state. Since idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.
- Preamble: For the CIS8204, the preamble is optional. By default, preambles are not expected or required. The preamble is a string of “1”s. See MII Register 1.6 for more information.
- Start of frame: A “01” pattern indicates the start of frame. If these bits are anything other than “01”, all following bits are ignored until the next “preamble:0” pattern is detected.
- Operation code: A “10” pattern indicates a read. A “01” pattern indicates a write. If these bits are anything other than “01” or “10”, all following bits are ignored until the next “preamble:0” pattern is detected.
- PHY address: The next five bits are the PHY address. The CIS8204 responds to a message frame only when the received PHY address matches its physical address. The three most significant bits of a PHY’s address are indicated by the PHYADD[4:2] pins. The two least significant bits are decoded internally to address one of the four PHYs.
- Register address: The next five bits are the register address.
- Turn-around: The next two bits are “turn-around” (TA) bits. They are used to avoid contention when a read operation is performed on the MDIO. During read operations, the CIS8204 will drive the second TA bit, which is a logical “0”.
- Data: The next sixteen bits are data bits. When data is being read from the PHY, data is valid at the output of the PHY from one rising edge of MDC to the next rising edge of MDC. When data is being written to the PHY, data must be valid around the rising edge of MDC.
- Idle: At least one idle bit is required between consecutive SMI frames.

The following two figures diagram SMI read and SMI write operations.

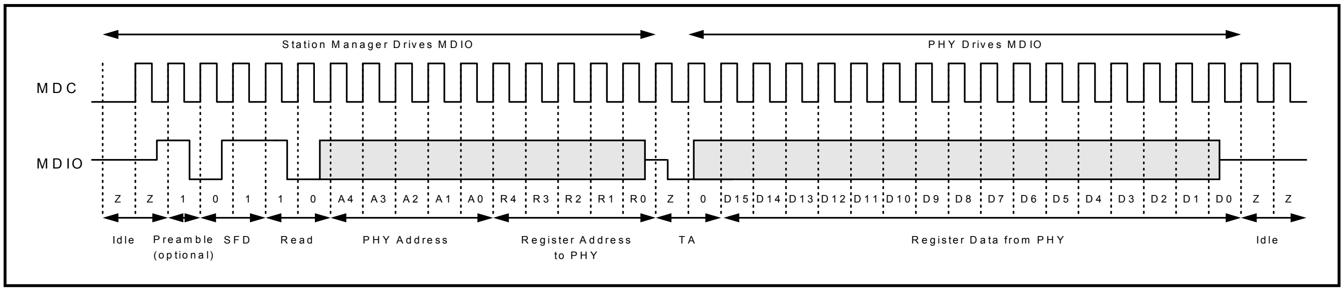

Figure 16-1. MDIO Read Frame

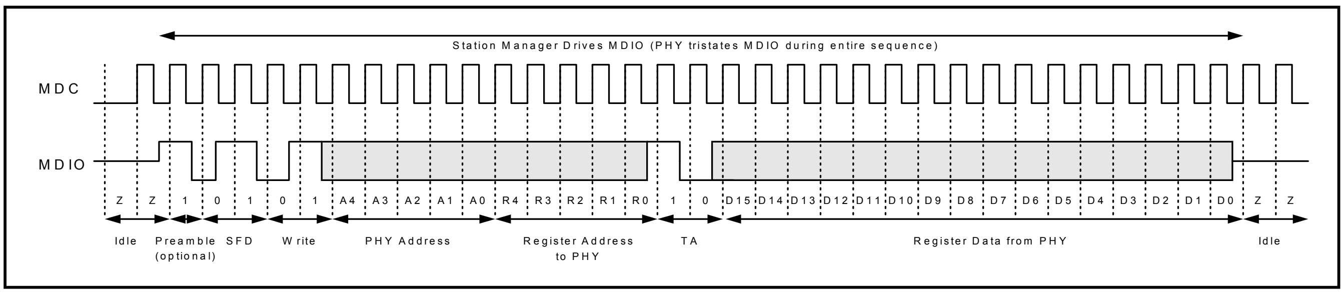

Figure 16-2. MDIO Write Frame

16.1 SMI Interrupt

The SMI includes an active low, open-drain output signal (MDINT#) for signalling the Station Manager when certain events occur in each PHY. When any of the four CIS8204 PHYs generates an interrupt, the open-drain MDINT# pin is pulled low, as long as the interrupt pin enable bit (MII Register bit 25.15) is enabled. MDINT# must be tied to VDDIO with a pull-up resistor at the Station Manager. See Figure 16-3.

Interrupts are disabled (masked off) in each of the CIS8204 PHYs by default. All interrupt mask bits are located in MII Register 25. Interrupt status bits are in MII Register 26. An interrupt is automatically acknowledged (cleared) when status bits in Register 26 are read.

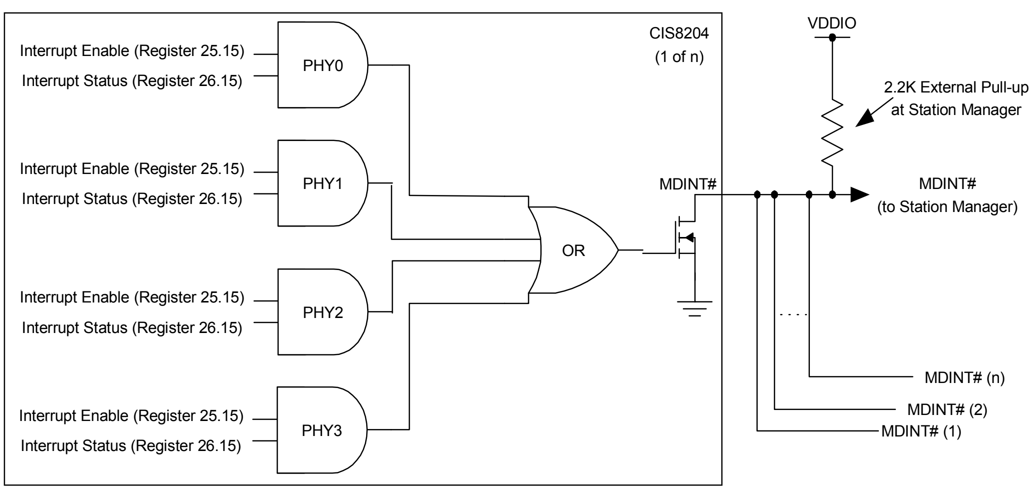

Figure 16-3. Logical Representation of MDINT# Pin

17 Serial LED Interface

The CIS8204 includes an LED output signal, which provides LED status information on a per PHY basis via a serial bit stream. The Serial LED Control Register (MII Register 27) controls all operating characteristics of the Serial LED Interface.

The Serial LED output uses two pins: data and clock. Data is clocked out continuously at a clock rate of approximately 1MHz. Data is valid on the rising edge of the clock. Data is clocked out in the order shown below, with bit 0 being clocked out first. Data bits for PHY0 are clocked out first, and data for the other PHYs are clocked out sequentially, in order.

A maximum frame in preambled mode is 73 bits long (37-bit preamble + 9 status bits/PHY x 4 PHYs), assuming all nine status bits per PHY are enabled. Note, however, that the serial frame can be shorter when any individual LED status bit is disabled, or if the preamble is suppressed (which is disabled by default). See MII Register 27 for more information.

Table 17-1. LED Status Bit Order

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
FDX	Link1000	Link100	Link10	Link	Link/Activity	Transmit	Receive	Collision

There are two operating modes: preambled and un-preambled (or preamble suppression).

- For the un-preambled mode (default mode):
  Up to 36 data bits are clocked out sequentially. At the end of a frame, the clock is stopped for 10ms. This pattern is repeated indefinitely. In this mode, the serial data can be clocked into an external shift register, whose outputs drive LEDs directly. As the data is clocked into a shift register, the shift register outputs will flicker. However, since the clock is stopped for 10ms after it is loaded, the flicker during bit shifting would not be perceptible to the human observer.
- For the preambled mode:
  The clock runs continuously. To delineate frames, a 37-bit preamble is added to the start of each frame. The preamble consists of thirty-six “1”s, followed by an additional “1”. This preamble can be used by the external LED logic and driver circuit to detect a new frame and change the state of the LEDs only after a new frame is completely received.

The Serial LED Interface’s bit definitions are defined in the following table.

Table 17-2. SLI Bit Definitions

LED Status Bit	Active State (asserted high)	Inactive State (asserted low)
FDX	Link is operating in full-duplex mode	Link is operating in half-duplex mode
Link1000	Link established at 1Gbps	Link NOT established at 1Gbps
Link100	Link established at 100Mbps	Link NOT established at 100Mbps
Link10	Link established at 10Mbps	Link NOT established at 10Mbps
Link	Link established at 1Gbps, 100Mbps, or 10Mbps	Link NOT established
Link/Activity	Transmit or Receive activity detected	Transmit or Receive activity NOT detected
Transmit	Transmit activity detected	Transmit activity NOT detected
Receive	Receive activity detected	Receive activity NOT detected
Collision	Collision detected (valid in half-duplex mode only)	No collision detected (valid in half-duplex mode only)

For system design simplicity, the default states of the LED enable bits in MII Register 27 have been chosen to enable the five most commonly implemented LEDs in a triple speed Ethernet application: FDX/HDX, Link10, Link100, Link1000, and Link/Activity.

This results in the normal length of a serial LED data frame of twenty bits (5 bits/PHY x 4 PHYs), since preamble suppression is the default operating mode.

18 Test Mode Interface (JTAG)

The CIS8204 supports the Test Access Port and Boundary Scan Architecture IEEE 1149.1 standards. The device includes an IEEE 1149.1 conformant test interface, often referred to as a “JTAG TAP Interface”. IEEE 1149.1 defines test logic to provide standardized test methodologies for:

- testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate,
- testing the integrated circuit itself during IC and systems manufacture, and
- observing or modifying circuit activity during the component’s normal operation.

The JTAG Test interface logic on the CIS8204, accessed through a Test Access Port (TAP) interface, consists of a boundary-scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal TRST#. Refer to the JTAG TAP Signal Descriptions and System Schematic sections for additional information about these pins.

The following figure diagrams the TAP and Boundary Scan Architecture.

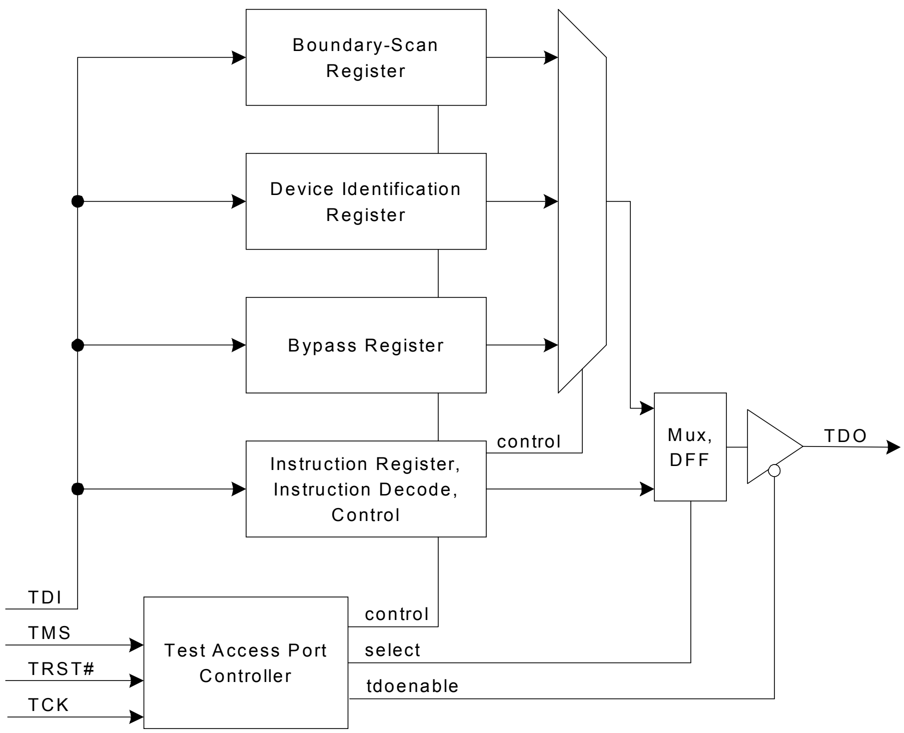

Figure 18-1. Test Access Port and Boundary Scan Architecture

The CIS8204 also includes the optional Device Identification Register, shown in the following table, which allows the manufacturer, part number, and version number of the device to be determined through the TAP Controller. See Chapter 11 of the IEEE 1149.1-1990 specifications for more details. Also, note that some of the information in the identification register is duplicated in the IEEE-specified bit fields in MII Register 3 (PHY Identifier Register #2).

Table 18-1. JTAG Device Identification Register Description

Description	Device Version Number (or Revision Code)	Part Number (or Model Number)	Cicada’s Manufacturer Identity	LSB
Bit Field	31 - 28	27 - 12	11 - 1	0
Binary Value	0111	0000000000000100	00110011000	1

The JTAG TAP port's AC timing requirements can be found in Section 24: "AC Timing Specifications".

18.1 Supported Instructions and Instruction Codes

After a TAP reset, the Device Identification Register is serially connected between TDI and TDO by default. The TAP Instruction Register is loaded either from a shift register (when a new instruction is shifted in), or, if there is no new instruction in the shift register, a hard-wired default value of 0110 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

The CIS8204 supports the instruction codes listed in the following table and described below.

Table 18-2. JTAG Interface Instruction Codes

Instruction	Code	Selected Register	Register Width	Specification
EXTEST	000	Boundary-Scan Register	217	Mandatory IEEE 1149.1
SAMPLE/PRELOAD	001	Boundary-Scan Register	217	Mandatory IEEE 1149.1
IDCODE	110	Device Identification Register	32	Optional IEEE 1149.1
CLAMP	010	Bypass Register	1	Optional IEEE 1149.1
HIGHZ	011	Bypass Register	1	Optional IEEE 1149.1
BYPASS	111	Bypass Register	1	Mandatory IEEE 1149.1
NANDTEST	101	Bypass Register	1	Optional IEEE 1149.1
Reserved	100			

EXTEST
The mandatory EXTEST instruction allows testing of off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values (with the PRELOAD instruction) prior to the EXTEST instruction.[1]

SAMPLE/PRELOAD
The mandatory SAMPLE/PRELOAD instruction allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

IDCODE
The optional IDCODE instruction provides the version number (bits 31:28), part number (bits 27:12), and Cicada's manufacturer identity (bits 11:1) to be serially read from the CIS8204. See Table 18-1: "JTAG Device Identification Register Description" for the CIS8204-specific values for this instruction.

CLAMP
The optional CLAMP instruction allows the state of the signals driven from the component pins to be determined from the Boundary-Scan Register while the Bypass Register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins will not change.[2]

HIGHZ
The optional HIGHZ instruction places the component in a state in which *all* of its system logic outputs are placed in a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.[2]

[1]Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., non-test) operation.

[2]Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., non-test) operation.

BYPASS
The Bypass Register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

NANDTEST
NANDTEST is an internal command used to activate the NAND Tree test mode. See Section 18.3: “NAND Tree Test Mode” for more information.

18.2 Boundary-Scan Register Cell Order

All inputs and outputs are observed in the Boundary-Scan Register cells. All outputs are additionally driven by the contents of Boundary-Scan Register cells. Bidirectional pins have all three related Boundary-Scan Register cells: the input, the output, and the control.

Port ordering from TDI to TDO is listed in the following table.

Table 18-3. JTAG Boundary-Scan Port Order (Sheet 1 of 3)

No.	Port	Type	No.	Port	Type
1	LED_CLK (CTRL)	Control/Observe	39	TX_CLK_0 (OUT)	Control/Observe
2	LED_CLK (OUT)	Control/Observe	40	COL_0 (CTRL)	Control/Observe
3	LED_DATA (CTRL)	Control/Observe	41	COL_0 (OUT)	Control/Observe
4	LED_DATA (OUT)	Control/Observe	42	CRS_0 (CTRL)	Control/Observe
5	TXD[0]_0 (IN)	Observe	43	CRS_0 (OUT)	Control/Observe
6	TXD[1]_0 (IN)	Observe	44	TXD[0]_1 (IN)	Observe
7	TXD[2]_0 (IN)	Observe	45	TXD[1]_1 (IN)	Observe
8	TXD[3]_0 (IN)	Observe	46	TXD[2]_1 (IN)	Observe
9	TXD[4]_0 (IN)	Observe	47	TXD[3]_1 (IN)	Observe
10	TXD[5]_0 (IN)	Observe	48	TXD[4]_1 (IN)	Observe
11	TXD[6]_0 (IN)	Observe	49	TXD[5]_1 (IN)	Observe
12	TXD[7]_0 (IN)	Observe	50	TXD[6]_1 (IN)	Observe
13	TX_EN_0 (IN)	Observe	51	TXD[7]_1 (IN)	Observe
14	TX_ER_0 (IN)	Observe	52	TX_EN_1 (IN)	Observe
15	GTX_CLK_0 (IN)	Observe	53	TX_ER_1 (IN)	Observe
16	RXD[0]_0 (CTRL)	Control/Observe	54	GTX_CLK_1 (IN)	Observe
17	RXD[0]_0 (OUT)	Control/Observe	55	RXD[0]_1 (CTRL)	Control/Observe
18	RXD[1]_0 (CTRL)	Control/Observe	56	RXD[0]_1 (OUT)	Control/Observe
19	RXD[1]_0 (OUT)	Control/Observe	57	RXD[1]_1 (CTRL)	Control/Observe
20	RXD[2]_0 (CTRL)	Control/Observe	58	RXD[1]_1 (OUT)	Control/Observe
21	RXD[2]_0 (OUT)	Control/Observe	59	RXD[2]_1 (CTRL)	Control/Observe
22	RXD[3]_0 (CTRL)	Control/Observe	60	RXD[2]_1 (OUT)	Control/Observe
23	RXD[3]_0 (OUT)	Control/Observe	61	RXD[3]_1 (CTRL)	Control/Observe
24	RXD[4]_0 (CTRL)	Control/Observe	62	RXD[3]_1 (OUT)	Control/Observe
25	RXD[4]_0 (OUT)	Control/Observe	63	RXD[4]_1 (CTRL)	Control/Observe
26	RXD[5]_0 (CTRL)	Control/Observe	64	RXD[4]_1 (OUT)	Control/Observe
27	RXD[5]_0 (OUT)	Control/Observe	65	RXD[5]_1 (CTRL)	Control/Observe
28	RXD[6]_0 (CTRL)	Control/Observe	66	RXD[5]_1 (OUT)	Control/Observe
29	RXD[6]_0 (OUT)	Control/Observe	67	RXD[6]_1 (CTRL)	Control/Observe
30	RXD[7]_0 (CTRL)	Control/Observe	68	RXD[6]_1 (OUT)	Control/Observe
31	RXD[7]_0 (OUT)	Control/Observe	69	RXD[7]_1 (CTRL)	Control/Observe
32	RX_DV_0 (CTRL)	Control/Observe	70	RXD[7]_1 (OUT)	Control/Observe
33	RX_DV_0 (OUT)	Control/Observe	71	RX_DV_1 (CTRL)	Control/Observe
34	RX_ER_0 (CTRL)	Control/Observe	72	RX_DV_1 (OUT)	Control/Observe
35	RX_ER_0 (OUT)	Control/Observe	73	RX_ER_1 (CTRL)	Control/Observe
36	RX_CLK_0 (CTRL)	Control/Observe	74	RX_ER_1 (OUT)	Control/Observe
37	RX_CLK_0 (OUT)	Control/Observe	75	RX_CLK_1 (CTRL)	Control/Observe
38	TX_CLK_0 (CTRL)	Control/Observe	76	RX_CLK_1 (OUT)	Control/Observe

Table 18-3. JTAG Boundary-Scan Port Order (Sheet 2 of 3)

No.	Port	Type
77	TX_CLK_1 (CTRL)	Control/Observe
78	TX_CLK_1 (OUT)	Control/Observe
79	COL_1 (CTRL)	Control/Observe
80	COL_1 (OUT)	Control/Observe
81	CRS_1 (CTRL)	Control/Observe
82	CRS_1 (OUT)	Control/Observe
83	TXD[0]_2 (IN)	Observe
84	TXD[1]_2 (IN)	Observe
85	TXD[2]_2 (IN)	Observe
86	TXD[3]_2 (IN)	Observe
87	TXD[4]_2 (IN)	Observe
88	TXD[5]_2 (IN)	Observe
89	TXD[6]_2 (IN)	Observe
90	TXD[7]_2 (IN)	Observe
91	TX_EN_2 (IN)	Observe
92	TX_ER_2 (IN)	Observe
93	GTX_CLK_2 (IN)	Observe
94	RXD[0]_2 (CTRL)	Control/Observe
95	RXD[0]_2 (OUT)	Control/Observe
96	RXD[1]_2 (CTRL)	Control/Observe
97	RXD[1]_2 (OUT)	Control/Observe
98	RXD[2]_2 (CTRL)	Control/Observe
99	RXD[2]_2 (OUT)	Control/Observe
100	RXD[3]_2 (CTRL)	Control/Observe
101	RXD[3]_2 (OUT)	Control/Observe
102	RXD[4]_2 (CTRL)	Control/Observe
103	RXD[4]_2 (OUT)	Control/Observe
104	RXD[5]_2 (CTRL)	Control/Observe
105	RXD[5]_2 (OUT)	Control/Observe
106	RXD[6]_2 (CTRL)	Control/Observe
107	RXD[6]_2 (OUT)	Control/Observe
108	RXD[7]_2 (CTRL)	Control/Observe
109	RXD[7]_2 (OUT)	Control/Observe
110	RX_DV_2 (CTRL)	Control/Observe
111	RX_DV_2 (OUT)	Control/Observe
112	RX_ER_2 (CTRL)	Control/Observe
113	RX_ER_2 (OUT)	Control/Observe
114	RX_CLK_2 (CTRL)	Control/Observe

No.	Port	Type
115	RX_CLK_2 (OUT)	Control/Observe
116	TX_CLK_2 (CTRL)	Control/Observe
117	TX_CLK_2 (OUT)	Control/Observe
118	COL_2 (CTRL)	Control/Observe
119	COL_2 (OUT)	Control/Observe
120	CRS_2 (CTRL)	Control/Observe
121	CRS_2 (OUT)	Control/Observe
122	TXD[0]_3 (IN)	Observe
123	TXD[1]_3 (IN)	Observe
124	TXD[2]_3 (IN)	Observe
125	TXD[3]_3 (IN)	Observe
126	TXD[4]_3 (IN)	Observe
127	TXD[5]_3 (IN)	Observe
128	TXD[6]_3 (IN)	Observe
129	TXD[7]_3 (IN)	Observe
130	TX_EN_3 (IN)	Observe
131	TX_ER_3 (IN)	Observe
132	GTX_CLK_3 (IN)	Observe
133	RXD[0]_3 (CTRL)	Control/Observe
134	RXD[0]_3 (OUT)	Control/Observe
135	RXD[1]_3 (CTRL)	Control/Observe
136	RXD[1]_3 (OUT)	Control/Observe
137	RXD[2]_3 (CTRL)	Control/Observe
138	RXD[2]_3 (OUT)	Control/Observe
139	RXD[3]_3 (CTRL)	Control/Observe
140	RXD[3]_3 (OUT)	Control/Observe
141	RXD[4]_3 (CTRL)	Control/Observe
142	RXD[4]_3 (OUT)	Control/Observe
143	RXD[5]_3 (CTRL)	Control/Observe
144	RXD[5]_3 (OUT)	Control/Observe
145	RXD[6]_3 (CTRL)	Control/Observe
146	RXD[6]_3 (OUT)	Control/Observe
147	RXD[7]_3 (CTRL)	Control/Observe
148	RXD[7]_3 (OUT)	Control/Observe
149	RX_DV_3 (CTRL)	Control/Observe
150	RX_DV_3 (OUT)	Control/Observe
151	RX_ER_3 (CTRL)	Control/Observe
152	RX_ER_3 (OUT)	Control/Observe

Table 18-3. JTAG Boundary-Scan Port Order (Sheet 3 of 3)

No.	Port	Type
153	RX_CLK_3 (CTRL)	Control/Observe
154	RX_CLK_3 (OUT)	Control/Observe
155	TX_CLK_3 (CTRL)	Control/Observe
156	TX_CLK_3 (OUT)	Control/Observe
157	COL_3 (CTRL)	Control/Observe
158	COL_3 (OUT)	Control/Observe
159	CRS_3 (CTRL)	Control/Observe
160	CRS_3 (OUT)	Control/Observe
161	CLK125 (CTRL)	Control/Observe
162	CLK125 (OUT)	Control/Observe
163	PWDN (IN)	Observe
164	RESET# (IN)	Observe
165	MDINT# (OUT)	Observe
166	MDC (IN)	Observe
167	MDIO (CTRL)	Control/Observe
168	MDIO (OUT)	Control/Observe
169	MDIO (IN)	Observe
170	PHYADD[2] (CTRL)	Control/Observe
171	PHYADD[2] (OUT)	Control/Observe
172	PHYADD[2] (IN)	Observe
173	PHYADD[3] (CTRL)	Control/Observe
174	PHYADD[3] (OUT)	Control/Observe
175	PHYADD[3] (IN)	Observe
176	PHYADD[4] (CTRL)	Control/Observe
177	PHYADD[4] (OUT)	Control/Observe
178	PHYADD[4] (IN)	Observe
179	DUPLEX_3 (CTRL)	Control/Observe
180	DUPLEX_3 (OUT)	Control/Observe
181	DUPLEX_3 (IN)	Observe
182	MODE[1]_3 (CTRL)	Control/Observe
183	MODE[1]_3 (OUT)	Control/Observe
184	MODE[1]_3 (IN)	Observe
185	MODE[0]_3 (CTRL)	Control/Observe
186	MODE[0]_3 (OUT)	Control/Observe
187	MODE[0]_3 (IN)	Observe
188	DUPLEX_2 (CTRL)	Control/Observe
189	DUPLEX_2 (OUT)	Control/Observe
190	DUPLEX_2 (IN)	Observe

No.	Port	Type
191	MODE[1]_2 (CTRL)	Control/Observe
192	MODE[1]_2 (OUT)	Control/Observe
193	MODE[1]_2 (IN)	Observe
194	MODE[0]_2 (CTRL)	Control/Observe
195	MODE[0]_2 (OUT)	Control/Observe
196	MODE[0]_2 (IN)	Observe
197	DUPLEX_1 (CTRL)	Control/Observe
198	DUPLEX_1 (OUT)	Control/Observe
199	DUPLEX_1 (IN)	Observe
200	MODE[1]_1 (CTRL)	Control/Observe
201	MODE[1]_1 (OUT)	Control/Observe
202	MODE[1]_1 (IN)	Observe
203	MODE[0]_1 (CTRL)	Control/Observe
204	MODE[0]_1 (OUT)	Control/Observe
205	MODE[0]_1 (IN)	Observe
206	DUPLEX_0 (CTRL)	Control/Observe
207	DUPLEX_0 (OUT)	Control/Observe
208	DUPLEX_0 (IN)	Observe
209	MODE[1]_0 (CTRL)	Control/Observe
210	MODE[1]_0 (OUT)	Control/Observe
211	MODE[1]_0 (IN)	Observe
212	MODE[0]_0 (CTRL)	Control/Observe
213	MODE[0]_0 (OUT)	Control/Observe
214	MODE[0]_0 (IN)	Observe
215	PLLMODE [CTRL]	Control/Observe
216	PLLMODE [OUT]	Control/Observe
217	PLLMODE [IN]	Observe

18.3 NAND Tree Test Mode

The NAND Tree test mode is an asynchronous test mode that is especially useful due to its speed advantages. This command connects groups of input pins together into a NAND Tree scheme. A group's inputs are initially held to logic high while its corresponding group of output pins are driven low. If any one of the input pins within a group is toggled from logic high to logic low, all the outputs in that group will toggle to the logic high state. This mode is entered by using the NANDTEST instruction code "101" within the JTAG Interface.

There are five NAND Tree pin groups, each with its separate assigned group of outputs, as listed in the following table and in Figure 18-2.

Table 18-4. NAND Tree Chains

Inputs	Outputs
GTX_CLK_0, TX_ER_0, TX_EN_0, TXD[7:0]_0	RX_CLK_0, TX_CLK_0, RX_ER_0, RX_DV_0, RXD[7:0]_0, COL_0, CRS_0
GTX_CLK_1, TX_ER_1, TX_EN_1, TXD[7:0]_1	RX_CLK_1, TX_CLK_1, RX_ER_1, RX_DV_1, RXD[7:0]_1, COL_1, CRS_1
GTX_CLK_2, TX_ER_2, TX_EN_2, TXD[7:0]_2	RX_CLK_2, TX_CLK_2, RX_ER_2, RX_DV_2, RXD[7:0]_2, COL_2, CRS_2
GTX_CLK_3, TX_ER_3, TX_EN_3, TXD[7:0]_3	RX_CLK_3, TX_CLK_3, RX_ER_3, RX_DV_3, RXD[7:0]_3, COL_3, CRS_3
PLLMODE, MODE[1:0]_0, MODE[1:0]_1, MODE[1:0]_2, MODE[1:0]_3, DUPLEX_0, DUPLEX_1, DUPLEX_2, DUPLEX_3, PHYADDR[4:2], MDIO, MDC, RESET#, PWDN	CLK125, LED_CLK, LED_DATA, MDINT#

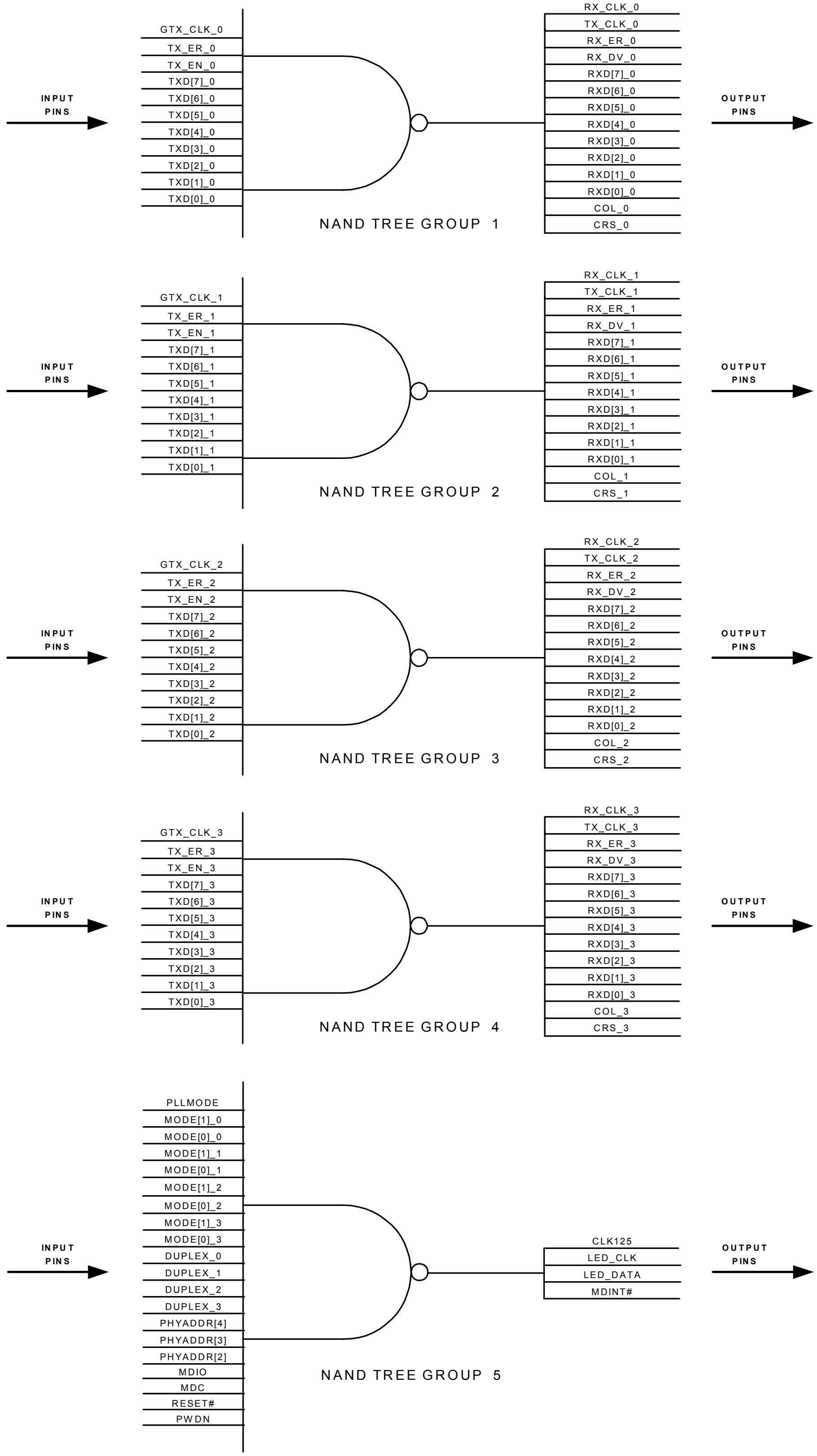

Figure 18-2. NAND Tree Logic Diagrams

19 Initialization & Configuration

19.1 Resets

A hardware reset is asynchronous (not related to MDC or any other input clock), applies to the entire chip (all four PHY ports), and is activated by asserting the RESET# signal (pulling to logical "0").

A software reset is synchronous with MDC and is specific to the PHY being addressed through MDIO. The table below summarizes the differences between the various initialization types.

Table 19-1. Initialization Types

Reset Control				MII Register States	Global or PHY Port Specific	Effect on PHY functions	TX_CLK and RX_CLK Active?
RESET# Pin	PWRDN Pin	Software Reset MII Register 0.15	Power Down MII Register 0.11				
0	X	X	X	Undefined	Global	All PHY Functions Disabled	Off
↑	0	0	0	Registers Reset to Default	Global	All PHY Functions Reset and Enabled	Enabled
1	1	X	X	Register Values Retained	Global	All PHY Functions Disabled Except MII Register Access. This is the lowest power operating mode.	Off
1	↓	X	X	Register Values Retained	Global	All PHY Functions Enabled, Auto-negotiation Restarted if Necessary	Enabled
1	0	↑[1]	X	Registers Reset to Default	PHY Port Specific	All PHY Functions Reset and Registers Reset, Auto-negotiation Restarted	No Effect
1	0	0	1	Register Values Retained	PHY Port Specific	All PHY Functions Disabled Except MII Register Access	Off
1	0	0	↓	Register Values Retained	PHY Port Specific	All PHY Functions Enabled, Auto-negotiation Restarted if Necessary	Enabled

[1] This bit is self clearing.

19.2 Power-Up Sequence

The following events occur in order when the CIS8204 is brought out of reset. This is triggered by a low-to-high transition of the RESET# pin. For more information, see Section 24.16: "Power-Down and Reset Timing".

1. Values for MODE, DUPLEX, PLLMODE and PHYADD pins are latched asynchronously immediately out of reset.
2. On the first rising edge of REFCLK after reset, the SMI (Serial Management Interface) becomes active.
3. Approximately 11 milliseconds after reset, the reference voltages and currents stabilize.
4. Once a stable reference is available, the PLL requires 50 microseconds to lock.
5. With a locked PLL, the analog-to-digital converter is calibrated, which requires 2.05 milliseconds.
6. Once the ADC is calibrated, the CLK125 output is activated

Once the PLL has locked, the internal chip clocks begin to run. At this point, the operation of the CIS8204 is dependent on the value of PWDN:

- If PWDN is high, the individual PHY blocks will not be enabled. The SMI is still operational.
- If PWDN is low, all sections of the device are enabled.

19.3 Manual Configuration

The MODE[1:0]_n and DUPLEX_n pins are intended for use in designs where a station manager is not available, or when manual PHY characterization testing or system diagnostics must be performed. This situation implies that the MII registers will not generally be extensively manipulated to control a PHY's operation (when the MODE and DUPLEX pins are used to set the operating mode). The states of these pins are not latched; any change in the states of these pins will cause the PHY to restart the auto-negotiation sequence.

In order to force the PHY's speed and duplex operating modes, the recommended sequence of events is as follows:

1) During a power-up or hardware reset sequence, force the MODE[1:0]_n and DUPLEX_n pins on a particular PHY to their desired states (e.g., VDDIO or GND). See Register bit 28.2 for more information.

2) Subsequent Auto-Negotiation and Parallel-Detect processes will now use the values specified by the MODE[1:0]_n and DUPLEX_n pins.

The effect of values forced on the MODE/DUPLEX pins when Auto-Negotiation or Parallel-Detect processes are completed will now only be visible in the Auxiliary Control and Status Register (28, bits 5:3).

19.4 Manual MASTER/SLAVE Mode

To set MASTER or SLAVE timing mode for 1000BASE-T:

1) Force the MODE[1:0]_n and DUPLEX_n pins to 10Xb, where X = 0 (SLAVE) and X =1 (MASTER). See Register 28.2 for more information.

2) Reset the device (hardware or software).

3) Subsequent Auto-Negotiation and Parallel-Detect processes will now use the values specified by the MODE[1:0]_n and DUPLEX_n pins.

19.5 Auto-Negotiation

The CIS8204 supports Auto-Negotiation, a standards-defined (IEEE 802.3-2002, Clause 28) process for determining the operating attributes of the local PHY and its link partner. Auto-Negotiation evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode.

In particular, Auto-Negotiation can determine speed, duplex, and MASTER/SLAVE modes for 1000BASE-T. Auto-Negotiation also allows the local MAC to communicate with the Link Partner MAC (via optional "Next-Pages") to set attributes that may not be defined in the standard.

The operating mode of the local PHY of the CIS8204 can be set by any one of three methods:

- Configuration control pins (MODE[1:0]_n and DUPLEX_n), as described in the previous section,
- SMI configuration control bits, or
- Auto-Negotiation.

Auto-Negotiation is used by default. Indeed, a station manager (connected via the SMI to the CIS8204) is optional; in the absence of a station manager, the CIS8204 will auto-negotiate upon exiting reset.

By default, the configuration control pins take precedence over the SMI configuration control bits unless MODE[1:0]_n = 11b and DUPLEX_n = X, which is the default operating mode for enabling Auto-Negotiation. See Section 13.10: "Configuration and Control Pins (Config)" for more information.

If Auto-Negotiation is enabled, Auto-Negotiation will start upon any of the following conditions:

- Release of hardware reset,
- Release of software reset,
- Restart Auto-Negotiation (Register bit 0.9),
- Release of Power-Down (Register bit 0.11), or
- Entering the “link_fail” state.

Once Auto-Negotiation starts, the CIS8204 will first determine if the Link Partner is Auto-Negotiation capable. If the Link Partner is Auto-Negotiation capable, the CIS8204 will, by default, determine the highest-performance operating mode that is common between the local PHY and the Link Partner’s PHY. If the Link Partner is not Auto-Negotiation capable, the CIS8204 will use Parallel-Detect to set the operating mode.

Note: When connecting the CIS8204 to a TBI-based MAC, the MAC should always disable IEEE 802.3z (Clause 37) Auto-Negotiation (if supported). 802.3z Auto-Negotiation was conceived to support two PHYs on opposite sides of a fiber optic cable, not to support MAC to PHY Auto-Negotiation.

19.6 MAC I/F Configuration

The MAC interface supports five different modes of operation: GMII, MII, RGMII, TBI, and RTBI. By default, the device operates in GMII MAC I/F mode with 3.3V I/O. Alternate MAC I/F operating modes, as well as I/O voltage supply levels, are selected by writing the appropriate MII Register 23 (Extended PHY Control Register #1) as shown in the following table.

Table 19-2. MAC I/F Mode Descriptions

MAC I/F Mode	Standard (Clause)	Supported Speed (Mbps)	Data Path Width x Freq.	I/O Voltage (Spec.)	Mode Selected by	Notes
GMII	802.3 (Clause 35)	1000	8b x 125MHz	3.3V	Hardware Reset or Software Reset or MII Register Write: 23.15:12 = 0000 23.11:9 = 000	Default operating mode
MII	802.3 (Clause 22)	100	4b x 25MHz			MII is default operating mode when link Auto-Negotiates (or is forced) to operate at 10Mb or 100Mb speeds
		10	4b x 2.5MHz			
RGMII[1]	RGMII v1.3	1000	4b x 125MHz DDR	2.5V (JEDEC EIA/JESD8-5)	MII Register Write: 23.15:12 = 0001 23.11:9 = 001	RGMII vs. 802.3 differences: 1) TXC is always generated by the MAC 2) RXC is always generated by the PHY
	RGMII v1.3 + MII (802.3 Clause 22)	100	4b x 25MHz			
		10	4b x 2.5MHz			
TBI	802.3 (Clause 36)	1000	10b x 125MHz	3.3V	MII Register Write: 23.15:12 = 0010 23.11:9 = 000	-
RTBI	RGMII v1.3	1000	5b x 125MHz DDR	2.5V (JEDEC EIA/JESD8-5)	MII Register Write: 23.15:12 = 0011 23.11:9 = 001	-

[1] The RGMII interface is timing compatible with the RGMII v1.3 and v2.0 specifications. The CIS8204 RGMII is not electrically compatible with the v2.0 specification as this requires HSTL voltage levels.

Switching between the various MAC interface modes is not recommended during normal operation, unless as supported by the GMII and RGMII standards to allow switching between 1000Mb, 100Mb, and 10Mb speeds. In addition, although any of the MAC interfaces will function electrically with I/O power supplies set at 3.3V or 2.5V, correct logical operation of the MAC interfaces at I/O voltages other than those specified above is not implied or guaranteed.

19.7 System Clock Interface (SCI)

The SCI is a three-pin interface comprised of the following pins: PLLMODE, REFCLK, and CLK125. See Section 13.11: “System Clock Interface Pins (SCI)” for more information.

PLLMODE is an input pin, sampled during power-up or reset sequences, which sets the reference clock frequency used by the PLL. When PLLMODE is low, the reference clock frequency of REFCLK is required to be 25MHz, with a ±50ppm frequency offset tolerance. When PLLMODE is high, REFCLK’s input frequency must be 125MHz (±50ppm).

The SCI also provides a free-running, general purpose, 125MHz output clock signal, CLK125, for use within the system. See Register 18.0 for more information. The CLK125 output pin is normally enabled (toggling) by default (but driven low when not enabled).

19.8 Auto MDI / MDI-X Function

For trouble-free configuration and management of Ethernet links, the CIS8204 includes robust Automatic Crossover Detection functionality for all three speeds (10BASE-T, 100BASE-TX, and 1000BASE-T) – fully compliant with the IEEE standard. In addition, the CIS8204 detects and corrects polarity errors on *all* MDI pairs, which is not required by the standard. Both the Automatic MDI/MDI-X and Polarity Correction functions are enabled by default.[1] However, complete user control of these two features is contained in MII Registers 18.5 (Automatic MDI/MDI-X Correction) and 18.4 (Automatic Polarity Correction). Status bits for each of these functions are indicated in MII Registers 26.6 and 26.5. For all three speeds of operation, any of the following MDI pair (A, B, C, D) connection combinations may be supplied to the device, with complete automatic detection and correction by the CIS8204.

The CIS8204's Automatic MDI/MDI-X algorithm will successfully detect, correct, and operate with any of the MDI wiring pair combinations listed in the following table.

Table 19-3. Accepted MDI Pair Connection Combinations

	RJ-45 Connections				Comments
	1,2	3,6	4,5	7,8	
MDI Pair Connection Combinations Accepted by CIS8204	A	B	C	D	Normal MDI mode Normal DTE/NIC mode No crossovers
	B	A	C	D	MDI-X mode Normal for switches & repeaters Crossover on A and B pairs only
	A	B	D	C	Normal MDI mode Normal for DTEs (NICs) No crossovers Pair swap on C and D pairs
	B	A	D	C	Normal MDI-X mode Normal switch/repeater mode Crossovers assumed Crossover on A and B pairs Pair swap on C and D pairs

[1]Consistent with 10/100/1000BASE-T PHYs on the market today, Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

The diagram below depicts the last combination in the table above, showing the CIS8204 operating with a link partner with crossovers on all four MDI pairs.

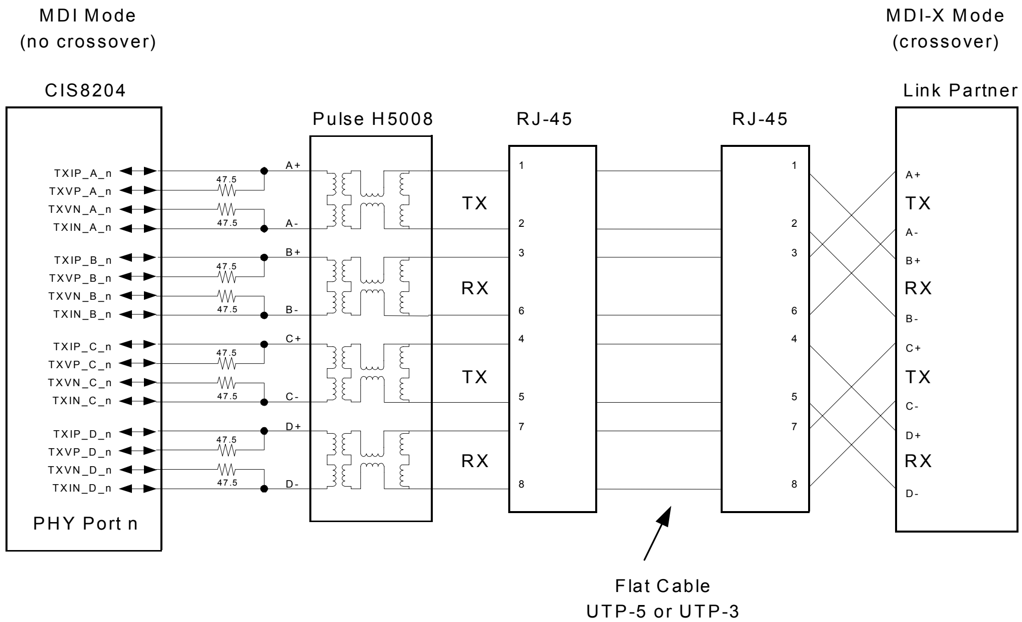

Figure 19-1. MDI / MDI-X Crossover Example

19.9 Serial LED I/F

See Section 17: “Serial LED Interface” for more information.

19.10 Power Supply Decoupling and Board Layout Guidelines

Please refer to the System Schematics in this document and the Applications Note: “Design and Layout Guidelines for the CIS8204”.

20 MII Register Set Conventions

The MII registers' bit modes are defined in the following table.

Table 20-1. MII Register Bit Modes

Register Bit Type	Description
R/W	Read and Write
RO	Read Only
LH	Latched High
LL	Latched Low
SC	Self-Cleared

Register conventions are as follows:

- Shaded registers indicate standard MII registers.
- All unshaded registers are optional registers, per the IEEE 802.3 standard.
- "Reset value" refers to the state of register bit(s) after *either* a hardware *or* a software reset. The only difference between a hardware and software reset is that all internal analog reference voltages and currents, including the PLL, are powered down while a hardware reset is asserted, but are not powered down while a software reset is asserted.

20.1 MII Register Names & Addresses

Table 20-2. MII Register Names & Addresses

Register Name	Register Number	Register Address (Hex)
Mode Control	0	00
Mode Status	1	01
PHY Identifier Register #1	2	02
PHY Identifier Register #2	3	03
Auto-Negotiation Advertisement	4	04
Auto-Negotiation Link Partner Ability	5	05
Auto-Negotiation Expansion	6	06
Auto-Negotiation Next-Page Transmit	7	07
Auto Negotiation Link Partner Next Page	8	08
1000BASE-T Control	9	09
1000BASE-T Status	10	0A
Reserved	11	0B
Reserved	12	0C
Reserved	13	0D
Reserved	14	0E
1000BASE-T Status Extension #1	15	0F
100BASE-TX Status Extension	16	10
1000BASE-T Status Extension #2	17	11
Bypass Control	18	12
Receive Error Counter	19	13
False Carrier Sense Counter	20	14
Disconnect Counter	21	15
10BASE-T Control & Status	22	16
Extended PHY Control #1	23	17
Extended PHY Control #2	24	18
Interrupt Mask	25	19
Interrupt Status	26	1A
Serial LED Control	27	1B
Auxiliary Control & Status	28	1C
Delay Skew Status	29	1D
Reserved	30	1E
Reserved	31	1F

20.2 MII Register Map Quick Reference (Sheet 1 of 2)

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register 0 (00h) Mode Control Register	Software Reset 0	Loopback 0	Forced Speed Select[0] 0	Auto-Neg Enable 1	Power-Down 0	Isolate 0	Restart Auto-Neg 0	Duplex Mode 0	Collision Test 0	Forced Speed Select[1] 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 1 (01h) Mode Status Register	100B-T4 0	100B-X FDX 1	100B-X HDX 1	10B-T FDX 1	10B-T HDX 1	100B-T2 FDX 0	100B-T2 HDX 0	Extended Status 1	Reserved 0	Preamble Suppression 1	Auto-Neg Complete 0	Remote Fault 0	Auto-Neg Capability 1	Link Status 0	Jabber Detect 0	Extended Capability 1
Register 2 (02h) PHY Identifier #1	OUI_MSB[3] 0	OUI_MSB[4] 0	OUI_MSB[5] 0	OUI_MSB[6] 0	OUI_MSB[7] 0	OUI_MSB[8] 0	OUI_MSB[9] 0	OUI_MSB[10] 0	OUI_MSB[11] 0	OUI_MSB[12] 0	OUI_MSB[13] 0	OUI_MSB[14] 0	OUI_MSB[15] 1	OUI_MSB[16] 1	OUI_MSB[17] 1	OUI_MSB[18] 1
Register 3 (03h) PHY Identifier #2	OUI_LSB[19] 1	OUI_LSB[20] 1	OUI_LSB[21] 0	OUI_LSB[22] 0	OUI_LSB[23 0	OUI_LSB[24] 1	Vendor Model Number[5] 0	Vendor Model Number[4] 0	Vendor Model Number[3] 0	Vendor Model Number[2] 1	Vendor Model Number[1] 0	Vendor Model Number[0] 0	Vendor Rev Number[3] 0	Vendor Rev Number[2] 1	Vendor Rev Number[1] 1	Vendor Rev Number[0] 1
Register 4 (04h) Auto-Neg Advertisement Register	Next Page 0	Reserved 0	Remote Fault 0	Reserved 0	Asymmetric Pause 0	Symmetric Pause 0	100B-T4 0	100B-X FDX 1	100B-X HDX 1	10B-T FDX 1	10B-T HDX 1	Selector Field[4] 0	Selector Field[3] 0	Selector Field[2] 0	Selector Field[1] 0	Selector Field[0] 1
Register 5 (05h) Auto-Neg Link Partner Ability Register	Next Page 0	ACK 0	Remote Fault 0	Reserved 0	Asymmetric Pause 0	Symmetric Pause 0	100B-T4 0	100B-X FDX 0	100B-X HDX 0	10B-T FDX 0	10B-T HDX 0	Selector Field[4] 0	Selector Field[3] 0	Selector Field[2] 0	Selector Field[1] 0	Selector Field[0] 0
Register 6 (06h) Auto-Neg Expansion Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Parallel Detect Fault 0	LP NP Able 0	NP Able 1	Page Received 0	LP Auto-Neg Able 0
Register 7 (07h) Auto-Neg NP Transmit Register	Next Page 0	Reserved 0	Message Page 1	ACK2 0	Toggle 0	Message/ Unformatted[10] 0	Message/ Unformatted[9] 0	Message/ Unformatted[8] 0	Message/ Unformatted[7] 0	Message/ Unformatted[6] 0	Message/ Unformatted[5] 0	Message/ Unformatted[4] 0	Message/ Unformatted[3] 0	Message/ Unformatted[2] 0	Messag/ Unformatted[1] 0	Message/ Unformatted[0] 1
Register 8 (08h) Auto-Neg Link Partner NP Receive Register	LP Next Page 0	LP ACK 0	LP Message Page 0	LP ACK2 0	LP Toggle 0	LP Message/ Unformatted[10] 0	LP Message/ Unformatted[9] 0	LP Message/ Unformatted[8] 0	LP Message/ Unformatted[7] 0	LP Message/ Unformatted[6] 0	LP Message/ Unformatted[5] 0	LP Message/ Unformatted[4] 0	LP Message/ Unformatted[3] 0	LP Message/ Unformatted[2] 0	LP Message/ Unformatted[1] 0	LP Message/ Unformatted[0] 0
Register 9 (09h) 1000BASE-T Control Register	Transmit Test[1] 0	Transmit Test[2] 0	Transmit Test[3] 0	M/S Config Enable 0	M/S Config Value 0	Port Type 0	1000B-T FDX 1	1000B-T HDX 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 10 (0Ah) 1000BASE-T Status Register	M/S Config Fault 0	M/S Config Resolution 1	Local Receiver Status 0	Remote Receiver Status 0	LP 1000B-T FDX 0	LP 1000B-T HDX 0	Reserved 0	Reserved 0	Idle Error Count[7] 0	Idle Error Count[6] 0	Idle Error Count[5] 0	Idle Error Count[4] 0	Idle Error Count[3] 0	Idle Error Count[2] 0	Idle Error Count[1] 0	Idle Error Count[0] 0
Register 11 (0Bh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 12 (0Ch) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 13 (0Dh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 14 (0Eh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 15 (0Fh) 1000BASE-T Status Extension Register	1000B-X FDX 0	1000B-X HDX 0	1000B-T FDX 1	1000B-T HDX 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0

Key:

Bit Name (Read/Writable) Reset Value	Bit Name (Read Only) Reset Value

MII Register Map Quick Reference (Sheet 2 of 2)

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register 16 (10h) 100BASE-TX Status Extension Register	100B-TX Descrambler Locked 0	100B-TX Lock Error Detected 0	100B-TX Disconnect State 0	100B-TX Current Link Status 0	100B-TX Receive Error Detected 0	100B-TX Transmit Error Detected 0	100B-TX SSD Error Detected 0	100B-TX ESD Error Detected 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 17 (11h) 1000BASE-T Status Extension Register #2	1000B-T Descrambler Locked 0	1000B-T Lock Error Detected 0	1000B-T Disconnect State 0	1000B-T Current Link Status 0	1000B-T Receive Error Detected 0	1000B-T Transmit Error Detected 0	1000B-T SSD Error Detected 0	1000B-T ESD Error Detected 0	1000B-T Carrier Extension Error Detected 0	Non-compliant BCM5400 Detected 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 18 (12h) Bypass Control Register	Transmit Disable 0	Bypass 4B5B Encoder/ Decoder 0	Bypass Scrambler 0	Bypass Descrambler 0	Bypass PCS Receive 0	Bypass PCS Transmit 0	Bypass LFI Timer 0	Transmitter Test Clock Enable 0	Non-compliant BCM5400 Detect 0	Bypass Non-compliant BCM5400 0	Disable Automatic Pair Swap Correction 0	Disable Polarity Correction 0	Parallel-Detect Control 0	Disable Pulse Shaping Filter 0	Disable Auto 1000B-T NP Exchange 0	125MHz Clock Output Enable 1
Register 19 (13h) Receive Error Counter Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Receive Error Counter[7] 0	Receive Error Counter[6] 0	Receive Error Counter[5] 0	Receive Error Counter[4] 0	Receive Error Counter[3] 0	Receive Error Counter[2] 0	Receive Error Counter[1] 0	Receive Error Counter[0] 0
Register 20 (14h) False Carrier Sense Counter Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	False Carrier Counter[7] 0	False Carrier Counter[6] 0	False Carrier Counter[5] 0	False Carrier Counter[4] 0	False Carrier Counter[3] 0	False Carrier Counter[2] 0	False Carrier Counter[1] 0	False Carrier Counter[0] 0
Register 21 (15h) Disconnect Counter Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Disconnect Counter[7] 0	Disconnect Counter[6] 0	Disconnect Counter[5] 0	Disconnect Counter[4] 0	Disconnect Counter[3] 0	Disconnect Counter[2] 0	Disconnect Counter[1] 0	Disconnect Counter[0] 0
Register 22 (16h) 10BASE-T Control & Status Register	Link Disable 0	Jabber Detect Disable 0	10B-T/100B-TX Echo Disable 0	SQE Disable 0	Squelch[1] 0	Squelch[0] 0	Reserved 0	EOF Error Detected 0	10B-T Disconnect 0	10B-T Link Status 0	Current Ref Trim[2] 0	Current Ref Trim[1] 0	Current Ref Trim[0] 0	Reserved 0	Reserved 0	Reserved 0
Register 23 (17h) Extended PHY Control Register #1	MAC I/F Mode[3] 0	MAC I/F Mode[2] 0	MAC I/F Mode[1] 0	MAC I/F Mode[0] 0	MAC I/F Voltage[2] 0	MAC I/F Voltage[1] 0	MAC I/F Voltage[0] 0	RGMII Skew Compensation 0	EWRAP 0	TBI Bit Order Reversal 0	Reserved 0	Link/Activity LED Blink Rate Control[1] 0	Link/Activity LED Blink Rate Control[0] 0	Link/Activity LED Blink Enable 1	Link/Activity LED Combine 0	Reserved 0
Register 24 (18h) Extended PHY Control Register #2	100/1000B-TX Edge Rate[2] 0	100/1000B-TX Edge Rate[1] 0	100/1000B-TX Edge Rate[0] 0	100/1000B-T TX VRef Trim[2] 0	100/1000B-T TX VRef Trim[1] 0	100/1000B-T TX VRef Trim[0] 0	TX FIFO Depth[2] (all modes) 1	TX FIFO Depth[1] (all modes) 0	TX FIFO Depth[0] (all modes) 0	RX FIFO Depth[2] (TBI) 1	RX FIFO Depth[1] (TBI) 0	RX FIFO Depth[0] (TBI) 0	Cable Quality Status 0	Cable Quality Status 0	Cable Quality Status 0	1000B-T Analog Loopback 0
Register 25 (19h) Interrupt Mask Register	Interrupt Pin Enable 0	Speed State-Change Interrupt Mask 0	Link State-Change Interrupt Mask 0	Duplex State-Change Interrupt Mask 0	Auto-Neg Error Interrupt Mask 0	Auto-Neg-Done Interrupt Mask 0	Page-Received Interrupt Mask 0	Symbol Error Interrupt Mask 0	Descrambler Lock-Lost Interrupt Mask 0	MDI Crossover Interrupt Mask 0	Polarity-Change Interrupt Mask 0	Jabber-Detect Interrupt Mask 0	False Carrier Interrupt Mask 0	Parallel-Detect Interrupt Mask 0	MASTER/ SLAVE Interrupt Mask 0	10B-T RX_ER Interrupt Mask 0
Register 26 (1Ah) Interrupt Status Register	Interrupt Status 0	Speed State-Change Interrupt Status 0	Link State-Change Interrupt Status 0	Duplex State-Change Interrupt Status 0	Auto-Neg Error Interrupt Status 0	Auto-Neg-Done Interrupt Status 0	Page-Received Intterupt Status 0	Symbol Error Interrupt Status 0	Descrambler Lock-Lost Interrupt Status 0	MDI Crossover Interrupt Status 0	Polarity-Change Interrupt Status 0	Jabber-Detect Interrupt Status 0	False Carrier Interrupt Status 0	Parallel-Detect Interrupt Mask 0	MASTER/ SLAVE Interrupt Status 0	RX_ER Interrupt Status 0
Register 27 (1Bh) Serial LED Control Register	Reserved 0	LED Preamble Enable 0	FDX/HDX LED Force On 0	FDX/HDX LED Disable 0	Link 10/100/1000 LEDs Force On 0	Link 10/100/1000 LEDs Disable 0	Link Status LED Force On 0	Link Status LED Disable 1	Link/Activity LED Force On 0	Link/Activity LED Disable 0	Transmit LED Force On 0	Transmit LED Disable 1	Receive LED Force On 0	Receive LED Disable 1	Collision-Detect LED Force On 0	Collision-Detect LED Disable 1
Register 28 (1Ch) Auxiliary Control & Status Register	Auto-Neg Complete 0	Auto-Neg Disabled 0	MDI/MDI-X XOver Indication 0	CD Pair Swap 0	A Polarity Inversion 0	B Polarity Inversion 0	C Polarity Inversion 0	D Polarity Inversion 0	Reserved 0	Link Quality 0	Duplex Status 0	Speed Status[1] 0	Speed Status[0] 0	MODE/DUPLEX Pin Priority 0	Reserved 0	Reserved 0
Register 29 (1Dh) Delay Skew Status Register	Reserved 0	Pair A Delay Skew[2] 0	Pair A Delay Skew[1] 0	Pair A Delay Skew[0] 0	Reserved 0	Pair B Delay Skew[2] 0	Pair B Delay Skew[1] 0	Pair B Delay Skew[0] 0	Reserved 0	Pair C Delay Skew[2] 0	Pair C Delay Skew[1] 0	Pair C Delay Skew[0] 0	Reserved 0	Pair D Delay Skew[2] 0	Pair D Delay Skew[1] 0	Pair D Delay Skew[0] 0
Register 30 (1Eh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 31 (1Fh) Reserved Register	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0

Key:

Bit Name (Read/Writable) Reset Value	Bit Name (Read Only) Reset Value

21 MII Register Descriptions

21.1 Register 0 (00h) – Mode Control Register

Bit	Name	Access	States	Reset Value
	Register 0 (00h) – Mode Control Register			
15	Software Reset	R/W SC	1 = Reset asserted 0 = Reset de-asserted	0
14	Loopback	R/W	1 = Loopback on 0 = Loopback off	0
6, 13	Forced Speed Selection	R/W	00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved	10
12	Auto-Negotiation Enable	R/W	1 = Auto-Negotiation enabled 0 = Auto-Negotiation disabled	1
11	Power-Down	R/W	1 = Power-down 0 = Power-up	0
10	Isolate	R/W	1 = Isolate PHY from MII or GMII 0 = Normal Operation	0
9	Restart Auto-Negotiation	R/W SC	1 = Restart MII 0 = Normal operation	0
8	Duplex Mode	R/W	1 = Full duplex 0 = Half duplex	0
7	Collision Test Enable	R/W	1 = Collision test enabled 0 = Collision test disabled	0
6	MSB for Speed Selection (see bit 13 above)	-	-	1
5:0	Reserved	-	-	000000

0.15 – Software Reset

Software Reset (i.e., setting Software Reset to "1") is self-clearing (i.e., automatically set to "0"). The only difference between a hardware and software reset is that a hardware reset also powers down all internal analog reference voltages and currents, including the PLL.

Once Software Reset is asserted, the PHY is returned to normal operating mode and is ready for the next SMI transaction, so Software Reset always reads back "0". Software Reset restores all SMI registers to their default states.

0.14 – Loopback

When Loopback is asserted, the Transmit Data (TXD) on the MAC interface is looped back as Receive Data (RXD). In loopback mode, no signal is transmitted over the network media. The loopback mechanism works in all (10/100/1000) modes of operation. The operating mode is determined by bits 0.13 and 0.6 (forced speed selection).

0.13, 0.6 – Forced Speed Selection

These bits determine the 10/100/1000 speed when Auto-Negotiation is disabled by clearing control bit 0.12. These bits are ignored if control bit 0.12 is set. Note that Auto-Negotiation is always required in 1000BASE-T mode and in normal operating modes unless the MODE and DUPLEX pins are used (see MII Register 28 for more information). These bits also determine the operating mode when Loopback (0.14) is set to "1".

0.12 – Auto-Negotiation Enable

After a power-up, or reset, the PHY automatically activates the Auto-Negotiation state machine, setting bit 0.12 to a "1". If bit 0.12 is written to a "0", the Auto-Negotiation process is disabled, and the present contents of the PHY's SMI register bits determine the operating characteristics. However, the values of the MODE[1:0]_n and DUPLEX_n pins take precedence in setting the advertised operating capabilities determined by a PHY's SMI register bits, unless Register bit 28.2 (MODE/DUPLEX Pin Priority Select bit) is set to "1". Note that Auto-Negotiation is always required in 1000BASE-T mode.

0.11 – Power-Down

Power-Down functions the same as Software Reset, except that it is not self-clearing, and that R/W SMI bits are *not* restored to their default states by Power-Down. The MII pins (except for SMI pins MDC, MDIO, and MDINT#) are electrically isolated during power-down. After Power-Down is released (i.e., set to "0"), the PHY will be ready for normal operation before the next SMI transaction. If Auto-Negotiation is enabled, the PHY will begin Auto-Negotiation immediately upon exiting Power-Down.

0.10 – Isolate

When Isolate is asserted (i.e., set to "1"), all MII and GMII outputs (except for MDIO) will be high impedance. Operation of the PHY is otherwise unaffected. For example, if Isolate is asserted while Auto-Negotiation is under way, Auto-Negotiation will continue unaffected.

0.9 – Restart Auto-Negotiation

When Restart Auto-Negotiation is asserted (i.e., set to "1"), the Auto-Negotiation state machine will restart the Auto-Negotiation process, even if it is in the middle of an Auto-Negotiation process. This control bit is self-clearing, meaning that it will always return a "0" when read.

0.8 – Duplex Mode

The CIS8204 operates in half-duplex by default. The CIS8204 can be reconfigured to operate in full-duplex by setting the Duplex Mode bit to a "1" while Auto-Negotiation is disabled by clearing bit 0.12. Changes to the state of Duplex Mode while Auto-Negotiation is enabled are ignored.

0.7 – Collision Test Enable

The collision test mode allows the COL pins to be tested during loopback mode. While the collision test mode is enabled (by setting Collision Test Enable to a "1"), asserting TX_EN will cause the COL output to go high within 512 bit times. De-asserting TX_EN will cause the COL output to go low within 4 bit times. The collision test mode should be enabled only when loopback is enabled.

05:0 – Reserved

21.2 Register 1 (01h) – Mode Status Register

Register 1 (01h) – Mode Status Register

Bit	Name	Access	States	Reset Value
15	100BASE-T4 Capability	RO	1 = 100BASE-T4 capable	0
14	100BASE-X FDX Capability	RO	1 = 100BASE-X FDX capable	1
13	100BASE-X HDX Capability	RO	1 = 100BASE-X HDX capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T FDX capable	1
11	10BASE-T HDX Capability	RO	1 = 10BASE-T HDX capable	1
10	100BASE-T2 FDX Capability	RO	1 = 100BASE-T2 FDX capable	0
9	100BASE-T2 HDX Capability	RO	1 = 100BASE-T2 HDX capable	0
8	Extended Status Enable	RO	1 = Extended status information present in R15	1
7	Reserved	RO		0
6	Preamble Suppression Capability	RO	1 = MF preamble may be suppressed 0 = MF preamble always required	1
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete	0
4	Remote Fault	RO LH	1 = Far-end fault detected 0 = No fault detected	0
3	Auto-Negotiation Capability	RO	1 = Auto-Negotiation capable	1
2	Link Status	RO LL	1 = Link is up 0 = Link is down	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1

1.15 – 100BASE-T4 Capability

The CIS8204 is not 100BASE-T4 capable, so this bit is hard-wired to “0”.

1.14 – 100BASE-X FDX Capability

The CIS8204 is 100BASE-X FDX capable, so this bit is hard-wired to “1”.

1.13 – 100BASE-X HDX Capability

The CIS8204 is 100BASE-X HDX capable, so this bit is hard-wired to “1”.

1.12 – 10BASE-T FDX Capability

The CIS8204 is 10BASE-T FDX capable, so this bit is hard-wired to “1”.

1.11 – 10BASE-T HDX Capability

The CIS8204 is 10BASE-T HDX capable, so this bit is hard-wired to “1”.

1.10 – 100BASE-T2 FDX Capability

The CIS8204 is not 100BASE-T2 FDX capable, so this bit is hard-wired to “0”.

1.9 – 100BASE-T2 HDX Capability

The CIS8204 is not 100BASE-T2 HDX capable, so this bit is hard-wired to “0”.

1.8 – Extended Status Enable

The CIS8204 is extended status capable, so this bit is hard-wired to “1”.

1.7 – Reserved

1.6 – Preamble Suppression Capability

The CIS8204 accepts management frames on the SMI without preambles, so preamble suppression capability is hard-wired to "1". The management frame preamble may be as short as 1 bit.

1.5 – Auto-Negotiation Complete

When this bit is a "1", the contents of Registers 4, 5, 6, 10 and 28 are valid.

1.4 – Remote Fault

Bit 1.4 will be set to "1" if the Link Partner signals a far-end fault. The bit is cleared automatically upon a read if the far-end fault condition has been removed.

1.3 – Auto-Negotiation Capability

The CIS8204 is Auto-Negotiation capable, so this bit is hard-wired to "1". Note that this bit will read a "1" even if Auto-Negotiation is disabled via bit 0.12.

1.2 – Link Status

This bit will return a "1" when the CIS8204 link state machine has reached the "link pass" state, meaning that a valid link has been established. If the link is subsequently lost, the Link Status will revert to a "0" state. It will remain a "0" until Link Status is read while the link state machine is in the "link pass" state.

1.1 – Jabber Detect

Note that Jabber Detect is required for 10BASE-T mode only. Jabber Detect will be set to "1" when the jabber condition is detected. Jabber Detect will be cleared automatically when this register is read.

1.0 – Extended Capability

The CIS8204 has extended register capability, so this bit is hard-wired to "1".

21.3 Register 2 (02h) – PHY Identifier Register #1

	Register 2 (02h) – Mode Control Register			
15:0	Organizationally Unique Identifier	RO	OUI most significant bits (Cicada OUI bits 3:18)	0000000000001111 or (000Fh)

2.15:0 – PHY Identifier Register #1

Cicada has been assigned an OUI from the IEEE of 0003F1h. Per IEEE requirements, only OUI bits 3 to 18 are used in this register.

21.4 Register 3 (03h) – PHY Identifier Register #2

Register 3 (03h) – PHY Identifier Register #2

Bit	Name	Access	States	Reset Value
15:10	Organizationally Unique Identifier	RO	OUI least significant bits (Cicada OUI bits 19:24)	110001
9:4	Vendor Model Number	RO	Vendor’s model number (IC)	000100 = CIS8204 0001XX = CIS820XX (future products)
3:0	Vendor Revision Number	RO	Vendor’s revision number (IC)	0111 = Silicon Revision B4 1000 = Silicon Revision B5

3.15:10 – OUI

Cicada has been assigned an OUI from the IEEE of 0003F1h. Per IEEE requirements, only OUI bits 19 to 24 are used in this register.

21.5 Register 4 (04h) – Auto-Negotiation Advertisement Register

Register 4 (04h) – Auto-Negotiation Advertisement Register

Bit	Name	Access	States	Reset Value
15	Next-Page Transmission Request	R/W	1 = Next-Page transmission request	0
14	Reserved	RO		0
13	Transmit Remote Fault	R/W	1 = Transmit remote fault	0
12	Reserved technologies	R/W		0
11	Advertise Asymmetric Pause	R/W	1 = Advertise Asymmetric Pause capable	0
10	Advertise Symmetric Pause	R/W	1 = Advertise Symmetric Pause capable	0
9	Advertise 100BASE-T4 Capability	R/W	1 = 100BASE-T4 capable	0
8	Advertise 100BASE-X FDX	R/W	1 = 100BASE-X FDX capable	1
7	Advertise 100BASE-X HDX	R/W	1 = 100BASE-X HDX capable	1
6	Advertise 10BASE-T FDX	R/W	1 = 10BASE-T FDX capable	1
5	Advertise 10BASE-T HDX	R/W	1 = 10BASE-T HDX capable	1
4:0	Advertise Selector Field	R/W		00001

This register controls the advertised abilities of the local (not remote) PHY. The state of this register is latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Thus, any writes to this register prior to completion of Auto-Negotiation as indicated by bit 1.5 should be followed by a re-negotiation for the new values to be properly used for Auto-Negotiation. Once Auto-Negotiation has completed, this register value may be read via the SMI to determine the highest common denominator technology.

4.15 – Auto-Negotiation Additional Next-Page Transmission Request

In 1000BASE-T, required Next-Pages are transmitted per the standard. A user may optionally transmit additional Next-Pages. The CIS8204 supports additional Next-Page transmission. Bit 4.15 is set by the user to request additional Next-Page transmission. See description of Register bit 18.1 for more details on Next-Page exchanges.

4.14, 4.12 – Reserved

4.13 – Transmit Remote Fault

The state of this bit is transmitted to the Link Partner during Auto-Negotiation. This bit does not have any effect on the local PHY operation. This bit is automatically cleared following a successful negotiation with the Link Partner.

4.11:10 – Advance Pause Capability

These bits are used by the local MAC to communicate pause capability to the Link Partner; this has no effect on PHY operation.

4.9:5 – Advertise Capability

Bits 4.9:5 allow the user to customize the ability information transmitted to the Link Partner during auto-negotiation. By writing a “1” to any of the bits, the corresponding ability will be advertised to the Link Partner. Writing a “0” to any bit causes the corresponding ability to be suppressed from transmission. The state of these bits has no other effect on the operation of the local PHY. Resetting the chip restores the default bit values. Note that the default values of these bits indicate the true ability of the CIS8204.

4.4:0 – Advertise Selector Field

Since the CIS8204 is a member of the 802.3 class of PHYs, the Advertise Selector Field defaults to “00001”. These bits are R/W only because the Ethernet standard requires them to be R/W. Changing the value of these bits has no effect on PHY operation.

21.6 Register 5 (05h) – Auto-Negotiation Link Partner Ability Register

Register 5 (05h) – Auto-Negotiation Link Partner Ability Register

Bit	Name	Access	States	Reset Value
15	LP Next-Page Transmit Request	RO	1 = LP NP transmit request	0
14	LP Acknowledge	RO	1 = LP acknowledge	0
13	LP Remote Fault	RO	1 = LP remote fault	0
12	Reserved technologies	RO		0
11	LP Asymmetric Pause Capability	RO	1 = Advertise Asymmetric Pause capable	0
10	LP Symmetric Pause Capability	RO	1 = Advertise Symmetric Pause capable	0
9	LP Advertise 100BASE-T4 Capability	RO	1 = LP Advertise 100BASE-T4 capable	0
8	LP Advertise 100BASE-X FDX	RO	1 = LP 100BASE-X FDX capable	0
7	LP Advertise 100BASE-X HDX	RO	1 = LP 100BASE-X HDX capable	0
6	LP Advertise 10BASE-T FDX	RO	1 = LP 10BASE-T FDX capable	0
5	LP Advertise 10BASE-T HDX	RO	1 = LP 10BASE-T HDX capable	0
4:0	LP Advertise Selector Field	RO	LP Advertise Selector Field	00000

5.15 – LP Next-Page Transmit Request

Bit 5.15 returns a “1” when the Link Partner implements the Next-Page function and has Next-Page information it wants to transmit. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

5.14 – LP Acknowledge

Bit 5.14 returns a “1” when the Link Partner signals that it has successfully received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3.

5.13 – LP Remote Fault

Bit 5.13 returns a “1” when the Link Partner signals that a remote fault (from its perspective) has occurred. The local PHY does not otherwise use this bit.

5.12 – Reserved

5.11 – LP Asymmetric Pause Capability

The LP Asymmetric Pause Capability bit indicates whether the Link Partner has asymmetric pause capability. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) is set.

5.10 – LP Symmetric Pause Capability

The LP Symmetric Pause Capability bit indicates whether the Link Partner supports symmetric pause frame capability. This bit is used by the Link Partner’s MAC to communicate symmetric pause capability to the local MAC; it has no effect on PHY operation.

5.9:5 – Advertise Capability

Bits 9:5 reflect the abilities of the Link Partner. A “1” on any of these bits indicates that the Link Partner advertises capability of performing the corresponding mode of operation.

5.4:0 – LP Selector Field Status

Bits 5.4:0 indicate the state of the Link Partner’s Selector Field. The local PHY does not otherwise use these bits.

21.7 Register 6 (06h) – Auto-Negotiation Expansion Register

Bit	Name	Access	States	Reset Value
	Register 6 (06h) – Auto-Negotiation Expansion Register			
15:5	Reserved	RO		00000000000
4	Parallel Detection Fault	RO LH	1 = Parallel detection fault	0
3	LP Next-Page Able	RO	1 = LP Next-Page capable	0
2	Local PHY Next-Page Able	RO	1 = Next-Page capable	1
1	Page Received	RO LH	1 = New page has been received	0
0	LP Auto-Negotiation Able	RO	1 = LP Auto-Negotiation capable	0

6.15:5 – Reserved

6.4 – Parallel Detection Fault

Parallel Detection Fault returns a “1” when a parallel detection fault occurs in the local Auto-Negotiation state machine. Once set, this bit is automatically cleared when (and only when) Register 6 is read.

6.3 – LP Next-Page Able

LP Next-Page Able returns a “1” when the Link Partner has Next-Page capabilities. This bit is used in the Auto-Negotiation state machines, as defined in Clause 28 of IEEE 802.3. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

6.2 – Local PHY Next-Page Able

Since the CIS8204 is Next-Page able, this bit is hard-wired to “1”.

6.1 – Page Received

Page Received is set to “1” when a new Link Code Word is received from the Link Partner, validated, and acknowledged. Page Received is automatically cleared when (and only when) Register 6 is read via the SMI.

6.0 – LP Auto-Negotiation Able

LP Auto-Negotiation Capable is set to “1” if the Link Partner advertises Auto-Negotiation capability. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set.

21.8 Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register

	Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register			
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Next Page	R/W	1 = More pages follow 0 = Last page	0
14	Reserved	RO		0
13	Message Page	R/W	1 = Message page 0 = Unformatted page	1
12	Acknowledge2	R/W	1 = Will comply with request 0 = Cannot comply with request	0
11	Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0
10:0	Message/Unformatted Code	R/W		00000000001

7.15 – Next Page

The Next Page bit indicates whether this is the last Next-Page to be transmitted. By default, this bit is set to “0”, indicating that this is the last page.

7.14 – Reserved

7.13 – Message Page

The Message Page bit indicates whether this page is a message page or an unformatted page. This bit does not otherwise affect the operation of the local PHY. By default, this bit is set to “1”, indicating that this is a message page.

7.12 – Acknowledge2

The Acknowledge2 bit indicates if the local MAC reports that it is able to act on the information (or perform the task) indicated in the previous message. The local PHY does not interpret or act on changes in the state of this bit.

7.11 – Toggle

The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. The Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word.

7.10:0 – Message/Unformatted Code

The Message/Unformatted Code bits indicate the message code being transmitted to the Link Partner. The local PHY passes the message code to the Link Partner without interpreting or reacting to it. By default, this code is set to “000 0000 0001”, indicating a null message.

21.9 Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register

Bit	Name	Access	States	Reset Value
	Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register			
15	LP Next Page	RO	1 = More pages follow 0 = Last page	0
14	LP Acknowledge	RO	1 = LP acknowledge	0
13	LP Message Page	RO	1 = Message page 0 = Unformatted page	0
12	LP Acknowledge2	RO	1 = LP will comply with request	0
11	LP Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0
10:0	LP Message/Unformatted Code	RO		00000000000

SMI Register 8 contains the Link Partner's Next-Page register contents. The contents of this register are only valid when the Page Received bit (6.1) is set.

8.15 – LP Next Page

This bit indicates if more pages follow from the Link Partner.

8.14 – LP Acknowledge

This bit returns a "1" when the Link Partner signals that it has received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3.

8.13 – LP Message Page

The Message Page bit indicates if the page received from the Link Partner is a message page or an unformatted page.

8.12 – LP Acknowledge2

The Acknowledge2 bit indicates whether the Link Partner MAC reports that it is able to act on the information (or perform the task) indicated in the message. The local PHY does not interpret or act on changes in the state of this bit.

8.11 – LP Toggle

The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. In the Link Partner, the Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word from the Link Partner.

8.10:0 – LP Message/Unformatted Code

The Message/Unformatted Code bits indicate the message code being transmitted by the Link Partner.

21.10 Register 9 (09h) – 1000BASE-T Control Register[1]

Register 9 (09h) – 1000BASE-T Control Register

Bit	Name	Access	States	Reset Value
15:13	Transmitter Test Mode	R/W	Described below, per IEEE 802.3, 40.6.1.1.2	000
12	MASTER/SLAVE Manual Configuration Enable	R/W	1 = Enable MASTER/SLAVE Manual Configuration value 0 = Disable MASTER/SLAVE Manual Configuration value	0
11	MASTER/SLAVE Manual Configuration Value	R/W	1 = Configure PHY as MASTER during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one. 0 = Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one.	0
10	Port Type	R/W	1 = Multi-port device 0 = Single-port device	1
9	1000BASE-T FDX Capability	R/W	1 = PHY is 1000BASE-T FDX capable	1
8	1000BASE-T HDX Capability	R/W	1 = PHY is 1000BASE-T HDX capable	1
7:0	Reserved	R/W		00000000

9.15:13 Transmitter/Receiver Test Mode[1]

This test is valid only in 1000BASE-T mode. Refer to IEEE 802.3-2002, section 40.6.1.1.2 for more information.

Table 21-1. 1000BASE-T Transmitter/Receiver Test Modes

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Test Mode
0	0	0	Normal operation
0	0	1	Test Mode 1 – Transmit waveform test
0	1	0	Test Mode 2 – Transmit jitter test in MASTER mode
0	1	1	Test Mode 3 – Transmit jitter test in SLAVE mode
1	0	0	Test Mode 4 – Transmitter distortion test
1	0	1	Reserved; operation not defined
1	1	0	Reserved; operation not defined
1	1	1	Reserved; operation not defined

- **Test Mode 1:** The PHY repeatedly transmits the following sequence of data symbols from all four transmitters: {{"+2" followed by 127 "0" symbols}, {"-2" followed by 127 "0" symbols}, {"+1" followed by 127 "0" symbols}, {"-1" followed by 127 "0" symbols}, {128 "+2" symbols, 128 "-2" symbols, 128 "+2" symbols, 128 "-2" symbols}, {1024 "0" symbols}}. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.
- **Test Mode 2:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
- **Test Mode 3:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in SLAVE timing mode.
- **Test Mode 4:** The PHY transmits the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:
  The maximum-length shift register used to generate the sequences defined by this polynomial is updated once per symbol

[1]The state of this register is internally latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

interval (8ns). The bits stored in the shift register delay line at a particular time *n* are denoted by Scrn[10:0]. At each symbol period, the shift register is advanced by one bit, and one new bit represented by Scrn[0] is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive-OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the quinary symbols, s_n, as shown in Table 21-2. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.

Table 21-2. 1000BASE-T Transmitter/Receiver Test Mode 4 – Quinary Symbols

$x2_n$	$x1_n$	$x0_n$	Quinary Symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	-1
1	0	0	0
1	0	1	1
1	1	0	-2
1	1	1	-1

9.12 – MASTER/SLAVE Manual Configuration Enable[1]

When this bit is set to “0” (default), the MASTER/SLAVE designation of the local PHY is determined using the arbitration protocol established in the IEEE Ethernet standard. When this bit is set to “1”, the MASTER/SLAVE designation of the local PHY is set by bit 9.11. Note that MASTER/SLAVE configuration is valid only in 1000BASE-T mode.

9.11 – MASTER/SLAVE Configuration Value[1]

This bit is ignored when bit 9.12 is set to “0”. However, if bit 9.12 is set to “1”, bit 9.11 determines the MASTER/SLAVE designation of the local PHY. If bit 9.12 is set to “1” and bit 9.11 set to “0” (default), the local PHY is forced to be a SLAVE. If bit 9.12 is set to “1” and bit 9.11 set to “1”, the local PHY is forced to be a MASTER. Note that MASTER/SLAVE configuration is valid only in 1000BASE-T mode.

9.10 – Port Type[1]

Since the CIS8204 is a quad port physical layer transceiver, bit 9.10 is set to “1” by default. When set to “1”, this bit indicates a preference for operation as a MASTER. If the Link Partner does not indicate the same preference, the local PHY will operate as a MASTER, and the Link Partner will be a SLAVE. Otherwise, the normal MASTER/SLAVE assignment protocol is used.

9.9 – 1000BASE-T FDX[1]

Since the CIS8204 is 1000BASE-T FDX capable, this bit is “1” by default. If bit 9.9 is written to be “0”, the Auto-Negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T FDX. Note that the Link Partner will be notified of the state of 9.9 during Auto-Negotiation. After Auto-Negotiation is complete, changing the state of this bit has no effect unless Auto-Negotiation is manually restarted.

9.8 – 1000BASE-T HDX[1]

Since the CIS8204 is 1000BASE-T HDX capable, this bit is “1” by default. If bit 9.8 is written to be “0”, the Auto-Negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T HDX. Note that the Link Partner will be notified of the state of 9.8 during Auto-Negotiation. After Auto-Negotiation is complete, changing the state of this bit has no effect unless Auto-Negotiation is manually restarted.

9.7:0 – Reserved

[1]The state of this register is internally latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

21.11 Register 10 (0Ah) – 1000BASE-T Status Register[1]

Bit	Name	Access	States	Reset Value
	Register 10 (0Ah) – 1000BASE-T Status Register			
15	MASTER/SLAVE Configuration Fault	RO LH SC	1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected	0
14	MASTER/SLAVE Configuration Resolution	RO	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	1
13	Local Receiver Status	RO	1 = Local receiver OK (loc_rcvr_status == OK) 0 = Local receiver not OK (loc_rcvr_status == NOT_OK)	0
12	Remote Receiver Status	RO	1 = Remote receiver OK (rem_rcvr_status == OK) 0 = Remote receiver not OK (rem_rcvr_status == NOT_OK)	0
11	LP 1000BASE-T FDX Capability	RO	1 = LP 1000BASE-T FDX capable 0 = LP not 1000BASE-T FDX capable	0
10	LP 1000BASE-T HDX Capability	RO	1 = LP is 1000BASE-T HDX capable 0 = LP is not 1000BASE-T HDX capable	0
9:8	Reserved	RO		00
7:0	Idle Error Count	RO SC		00000000

10.15 – MASTER/SLAVE Configuration Fault[1]

This bit indicates whether a MASTER/SLAVE configuration fault has been detected by the local PHY. A configuration fault occurs if both the local and remote PHYs are forced to the same MASTER/SLAVE state, or if no resolution is reached after seven retries. When such a fault has been detected, this bit is set to “1”, but the PHY continues to renegotiate until the MASTER/SLAVE configuration is resolved. Once set, this bit is automatically cleared when (and only when) Register 10 is read via the SMI.

10.14 – MASTER/SLAVE Configuration Resolution[1]

By default, the MASTER/SLAVE configuration is determined as part of the Auto-Negotiation process. However, the MASTER/SLAVE status can optionally be manually forced via bits in Register 9. Bit 10.14 indicates the final MASTER/SLAVE configuration status for the local PHY. This bit can change state only as a result of the reset or subsequent restart of the Auto-Negotiation process. This bit is only valid when the Auto-Negotiation Complete bit (1.5) is set.

10.13 – Local Receiver Status[1]

Bit 10.13 indicates the state of the loc_rcvr_status flag within the PMA receive function within the local PHY.

10.12 – Remote Receiver Status[1]

Bit 10.12 indicates the state of the rem_rcvr_status flag within the PMA receive function within the local PHY.

10.11 – LP 1000BASE-T FDX Capability[2]

Bit 10.11 is set to “1” if the Link Partner PHY advertises 1000BASE-T FDX capability; otherwise, this bit is set to “0”.

10.10 – LP 1000BASE-T HDX Capability[2]

[1]The bits in this register apply only in 1000BASE-T mode.

[2]This bit is valid only when the Page Recieved bit (6.1) is set to a “1”.

Bit 10.10 is set to “1” if the Link Partner PHY advertises 1000BASE-T HDX capability; otherwise, this bit is set to “0”.

10.9:8 – Reserved

10.7:0 – Idle Error Count[1]

Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND_N (indicating that both the local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rx_error_status in the PMA receive function is equal to ERROR. Bits 10.7:0 are reset to all “0”s when the error count is read by the management function, or upon execution of the PCS reset function, and they are saturated to all “1”s in case of overflow.

[1]This bit applies only in 1000BASE-T mode.

21.12 Register 11 (0Bh) – Reserved Register

	Register 11 (0Bh) – Reserved Register			
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

11.15:0 – Reserved

21.13 Register 12 (0Ch) – Reserved Register

	Register 12 (0Ch) – Reserved Register			
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

12.15:0 – Reserved

21.14 Register 13 (0Dh) – Reserved Register

	Register 13 (0Dh) – Reserved Register			
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

13.15:0 – Reserved

21.15 Register 14 (0Eh) – Reserved Register

	Register 14 (0Eh) – Reserved Register			
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

14.15:0 – Reserved

21.16 Register 15 (0Fh) – 1000BASE-T Status Extension Register #1

Register 15 (0Fh) – 1000BASE-T Status Extension Register

Bit	Name	Access	States	Reset Value
15	1000BASE-X FDX Capability	RO	1 = PHY is 1000BASE-X FDX capable 0 = PHY is not 1000BASE-X FDX capable	0
14	1000BASE-X HDX Capability	RO	1 = PHY is 1000BASE-X HDX capable 0 = PHY is not 1000BASE-X HDX capable	0
13	1000BASE-T FDX Capability	RO	1 = PHY is 1000BASE-T FDX capable 0 = PHY is not 1000BASE-T FDX capable	1
12	1000BASE-T HDX Capability	RO	1 = PHY is 1000BASE-T HDX capable 0 = PHY is not 1000BASE-T HDX capable	1
11:0	Reserved	RO		000000000000

15.15 – 1000BASE-X FDX Capability

The CIS8204 is not 1000BASE-X capable, so this bit is hard-wired to “0”.

15.14 – 1000BASE-X HDX Capability

The CIS8204 is not 1000BASE-X capable, so this bit is hard-wired to “0”.

15.13 – 1000BASE-T FDX Capability

The CIS8204 is 1000BASE-T FDX capable, so this bit is hard-wired to “1”.

15.12 – 1000BASE-T HDX Capability

The CIS8204 is 1000BASE-T HDX capable, so this bit is hard-wired to “1”.

15.11:0 – Reserved

21.17 Register 16 (10h) – 100BASE-TX Status Extension Register[1]

Bit	Name	Access	States	Reset Value
	Register 16 (10h) – 100BASE-TX Status Extension Register			
15	100BASE-TX Descrambler Locked	RO	1 = Descrambler locked 0 = Descrambler not locked	0
14	100BASE-TX Lock Error Detected	RO SC	1 = Lock error detected since last read 0 = Lock error not detected since last read	0
13	100BASE-TX Disconnect State	RO SC	1 = PHY 100BASE-TX link disconnected 0 = PHY 100BASE-TX link not disconnected	0
12	100BASE-TX Current Link Status	RO	1 = PHY 100BASE-TX link active 0 = PHY 100BASE-TX link inactive	0
11	100BASE-TX Receive Error Detected	RO SC	1 = Receive error detected since last read 0 = Receive error not detected since last read	0
10	100BASE-TX Transmit Error Detected	RO SC	1 = Transmit error detected since last read 0 = Transmit error not detected since last read	0
9	100BASE-TX SSD Error Detected	RO SC	1 = SSD error detected since last read 0 = SSD error not detected since last read	0
8	100BASE-TX ESD Error Detected	RO SC	1 = ESD error detected since last read 0 = ESD error not detected since last read	0
7:0	Reserved	RO		00000000

16.15 – 100BASE-TX Descrambler Locked[1]

Bit 16.15 is set to “1” when the 100BASE-TX descrambler is locked; otherwise, this bit is set to “0”.

16.14 – 100BASE-TX Lock Error Detected[1]

Bit 16.14 is set to “1” if the 100BASE-TX descrambler has lost lock since the last read of this bit; otherwise, this bit is set to “0”.

16.13 – 100BASE-TX Disconnect State[1]

Bit 16.13 is set to “1” if the 100BASE-TX connection has been broken since the last read of this bit; otherwise, this bit is set to “0”.

16.12 – 100BASE-TX Current Link Status[1]

Bit 16.12 is set to “1” if the 100BASE-TX link is active; otherwise, this bit is set to “0”.

16.11 – 100BASE-TX Receive Error Detected[1]

Bit 16.11 is set to “1” if a 100BASE-TX packet with an invalid code has been received since the last read of this bit; otherwise, this bit is set to “0”.

16.10 – 100BASE-TX Transmit Error Detected[1]

Bit 16.10 is set to “1” if a 100BASE-TX packet has been received with a transmit error code since the last read of this bit; otherwise, this bit is set to “0”.

16.9 – 100BASE-TX False Carrier (SSD Error) Detected[1]

Bit 16.9 is set to “1” if a 100BASE-TX false carrier (Start-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to “0”.

[1]The bits in this register apply only in 100BASE-TX mode.

16.8 – 100BASE-TX Premature End (ESD Error) Detected[1]

Bit 16.8 is set to "1" if a 100BASE-TX premature end (End-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to "0".

16.7:0 – Reserved

[1]The bits in this register apply only in 100BASE-TX mode.

21.18 Register 17 (11h) – 1000BASE-T Status Extension Register #2[1]

Bit	Name	Access	States	Reset Value
	Register 17 (11h) – 1000BASE-T Status Extension Register #2			
15	1000BASE-T Descrambler Locked	RO	1 = Descrambler locked 0 = Descrambler not locked	0
14	1000BASE-T Lock Error Detected	RO SC	1 = Lock error detected since last read 0 = Lock error not detected since last read	0
13	1000BASE-T Disconnect State	RO SC	1 = PHY 1000BASE-T link disconnected 0 = PHY 1000BASE-T link not disconnected	0
12	1000BASE-T Current Link Status	RO	1 = PHY 1000BASE-T link active 0 = PHY 1000BASE-T link inactive	0
11	1000BASE-T Receive Error Detected	RO SC	1 = Receive error detected since last read 0 = Receive error not detected since last read	0
10	1000BASE-T Transmit Error Detected	RO SC	1 = Transmit error detected since last read 0 = Transmit error not detected since last read	0
9	1000BASE-T SSD Error Detected	RO SC	1 = SSD error detected since last read 0 = SSD error not detected since last read	0
8	1000BASE-T ESD Error Detected	RO SC	1 = ESD error detected since last read 0 = ESD error not detected since last read	0
7	1000BASE-T Carrier Extension Error Detected	RO SC	1 = Carrier extension error detected since last read 0 = Carrier extension error not detected since last read	0
6	Non-compliant BCM5400 Detected	RO	1 = Non-compliant BCM5400 detected 0 = Non-compliant BCM5400 not detected	0
5:0	Reserved	RO		000000

17.15 – 1000BASE-T Descrambler Locked [1]

Bit 17.15 is set to “1” when the 1000BASE-T descrambler is locked; otherwise, this bit is set to “0”.

17.14 – 1000BASE-T Lock Error Detected[1]

Bit 17.14 is set to “1” if the 1000BASE-T descrambler has lost lock since the last read of this bit; otherwise, this bit is set to “0”.

17.13 – 1000BASE-T Disconnect State[1]

Bit 17.13 is set to “1” if the 1000BASE-T connection has been broken since the last read of this bit; otherwise, this bit is set to “0”.

17.12 – 1000BASE-T Current Link Status[1]

Bit 17.12 is set to “1” if the 1000BASE-T link is active; otherwise, this bit is set to “0”.

17.11 – 1000BASE-T Receive Error Detected[1]

Bit 17.11 is set to “1” if a 1000BASE-T packet with an invalid code has been received since the last read of this bit; otherwise, this bit is set to “0”.

17.10 – 1000BASE-T Transmit Error Detected[1]

Bit 17.10 is set to “1” if a 1000BASE-T packet has been received with a transmit error code since the last read of this bit; otherwise, this bit is set to “0”.

[1]The bits in this register apply only in 1000BASE-T mode.

17.9 – 1000BASE-T False Carrier (SSD Error) Detected[1]

Bit 17.9 is set to "1" if a 1000BASE-T false carrier (Start-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to "0".

17.8 – 1000BASE-T Premature End (ESD Error) Detected[1]

Bit 17.8 is set to "1" if a 1000BASE-T premature end (End-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to "0".

17.7 – 1000BASE-T Carrier Extension Error Detected[1]

Bit 17.7 is set to "1" if a carrier extension error has been detected since the last read of this bit; otherwise, this bit is set to "0".

17.6 – Non-compliant BCM5400 Detected[1]

Bit 17.6 is a read-only bit set to "1" if the CIS8204 detects a non-compliant BCM5400 as its link partner; otherwise, this bit is set to "0". This bit is valid only when the 1000BASE-T descrambler has achieved a locked state.

17.5:0 – Reserved

[1]The bits in this register apply only in 1000BASE-T mode.

21.19 Register 18 (12h) – Bypass Control Register

Bit	Name	Access	States	Reset Value
	Register 18 (12h) – Bypass Control Register			
15	Transmit Disable	R/W	1 = Transmitter disabled in PHY 0 = Transmitter enabled	0
14	Bypass 4B5B Encoder/Decoder	R/W	1 = Bypass 4B5B encoder/decoder 0 = Enable 4B5B encoder/decoder	0
13	Bypass Scrambler	R/W	1 = Bypass scrambler 0 = Enable scrambler	0
12	Bypass Descrambler	R/W	1 = Bypass descrambler 0 = Enable descrambler	0
11	Bypass PCS Receive	R/W	1 = Bypass PCS receive 0 = Enable PCS receive	0
10	Bypass PCS Transmit	R/W	1 = Bypass PCS transmit 0 = Enable PCS transmit	0
9	Bypass Link Fail Inhibit (LFI) Timer	R/W	1 = Bypass link_fail_inhibit timer (to enable faster Auto-Negotiation) 0 = Do not bypass link_fail_inhibit timer	0
8	Transmitter Test Clock Enable	R/W	1 = Enable TX_TCLK test output on CLK125 pin 0 = Disable TX_TCLK test output on CLK125 pin	0
7	Force Non-compliant BCM5400 Detection	R/W	1 = Force non-compliant BCM5400 detection 0 = Do not force non-compliant BCM5400 detection	0
6	Bypass Non-compliant BCM5400 Detection	R/W	1 = Disable automatic non-compliant BCM5400 detection 0 = Enable automatic non-compliant BCM5400 detection	0
5	Disable Automatic Pair Swap Correction	R/W	1 = Disable pair swap correction 0 = Enable pair swap correction	0
4	Disable Polarity Correction	R/W	1 = Disable polarity inversion correction 0 = Enable polarity inversion correction	0
3	Parallel-Detect Control	R/W	1 = Do not ignore advertised ability 0 = Ignore advertised ability	1
2	Disable Pulse Shaping Filter	R/W	1 = Disable pre-emphasis filter 0 = Enable pre-emphasis filter	0
1	Disable Automatic 1000BASE-T Next-Page Exchange	R/W	1 = Disable automatic 1000BASE-T Next-Page exchanges 0 = Enable automatic 1000BASE-T Next-Page exchanges	0
0	125MHz Clock Output Enable	R/W	1 = Enable 125MHz output clock pin (CLK125) 0 = Disable 125MHz output clock pin (CLK125)	1

18.15 – Transmit Disable

When bit 18.15 is set to “1”, the analog blocks are powered down and zeros are sent to the DAC.

18.14 – Bypass 4B5B Encoder/Decoder[1]

When bit 18.14 is set to “1”, the 5B codes (TX_ER and TXD[3:0]) will be passed from the MII interface directly to the scrambler, bypassing the 4B5B encoder. Note that in this mode, J/K and T/R code insertion will not be performed. The receiver will pass descrambled/aligned 5B codes directly to the MII interface (RX_ER and RXD[3:0]), bypassing the 4B5B decoder. Carrier sense (CRS) is still asserted when a valid frame is detected.

18.13 – Bypass Scrambler[2]

When bit 18.13 is set to “1”, the scrambler is disabled.

[1]This bit applies only in 100BASE-TX mode.

[2]This bit applies only in 100BASE-TX and 1000BASE-T modes.

18.12 – Bypass Descrambler[1]

When bit 18.12 is set to "1", the descrambler is disabled.

18.11 – Bypass PCS Receive[1]

When bit 18.11 is set to "1", PCS receive for the four subchannels is bypassed. In 1000BASE-T mode, a 4-D symbol is encoded into a 10-bit data word and sent to the GMII interface. The RX_DV and RX_ER pins are used for the upper two bits of the encoded data, and RXD pins are used for the remaining eight bits of the encoded data. When receiving idle codes, the Viterbi decoder can by bypassed, receiving symbols through the 4-D slicer instead. In 100BASE-TX mode, to pass the unaligned symbols directly to the MII interface, this control bit should be set only when the 4B5B decoder is also bypassed.

18.10 – Bypass PCS Transmit[1]

When bit 18.10 is set to "1", the PCS transmit for the four subchannels is bypassed.

18.9 – Bypass LFI Timer

If this bit is set, the link_fail_inhibit timer defined in Clause 28 of the IEEE 802.3 standard is bypassed under certain conditions to allow faster re-Auto-Negotiation. This timer will be bypassed if either the MASTER/SLAVE negotiation resulted in a tie, or no common capabilities were discovered during the previous negotiation. If this bit is not set, the Auto-Negotiation state machines behave as defined in the IEEE standard.

18.8 – Enable Transmit Clock TX_TCLK Output on CLK125 Pin

When bit 18.8 is written to a "1", the CLK125 output pin becomes a test pin for the transmit clock "TX_TCLK" of a particular PHY port. This capability is intended to enable measurement of transmitter timing jitter, as specified in IEEE Standard 802.3-2002, section 40.6.1.2.5. When in IEEE-specified transmitter test modes 2 or 3 (see IEEE 802.3-2002, section 40.6.1.1.2 and MII Register bits 9.15:13), the peak-to-peak jitter of the zero-crossings of the differential signal output at the MDI, relative to the corresponding edge of TX_TCLK, is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

While transmitter test mode clocks TX_TCLK_n are intended only for characterization test purposes, CLK125 is intended, for example, to serve as a general purpose system or MAC reference clock.

Five distinct clock signals can be multiplexed onto the CIS8204's CLK125 pin, depending on a combination of the settings of MII Register bits 9.15:13, MII Register bit 18.8, and MII Register bit 18.0 (CLK125 Output Enable), as specified in the following table.

Table 21-3. CLK125 Pin Multiplexed Clock Signals

Signal Multiplexed onto CLK125 Pin	Enabled by MII Register States
TX_TCLK_0	PHY0, ((9.15:13 == 010) || (9.15:13 == 011) || (18.8 ==1))
TX_TCLK_1	PHY1, ((9.15:13 == 010) || (9.15:13 == 011) || (18.8 ==1))
TX_TCLK_2	PHY2. ((9.15:13 == 010) || (9.15:13 == 011) || (18.8 ==1))
TX_TCLK_3	PHY3, ((9.15:13 == 010) || (9.15:13 == 011) || (18.8 ==1))
CLK125[1]	PHY0, 18.0 == 1

[1] Only PHY Port 0's bit 18.0 controls the operation of CLK125 (see MII Register bit 18.0).

[1]This bit applies only in 100BASE-TX and 1000BASE-T modes.

18.7 – Force Non-compliant BCM5400 Detection[1]

The state of this bit does not affect the operation of the PHY when MII Register bit 18.6 is set to “0”. If Register bit 18.6 is set to “1” and this bit is set to “1”, then the local PHY operates as a non-compliant BCM5400 PHY. If Register bit 18.6 is set to “1” and this bit is set to “0”, the local PHY operates as a fully IEEE compliant PHY. (Note that this control bit applies only in 1000BASE-T mode.)

18.6 – Bypass Non-compliant BCM5400 Detection[1]

When bit 18.6 is set to “0”, the PHY automatically detects and corrects for non-compliant BCM5400 link partner PHYs. When this bit is set to “1”, automatic non-compliant BCM5400 detection is disabled, and the local PHY’s operating mode is determined by the status of MII Register bit 18.7. If bit 18.7 is a “1”, then the local PHY operates as a non-compliant BCM5400 PHY. When bit 18.7 is a “0”, the local PHY operates as a fully IEEE-compliant PHY. (Note that this control bit applies only in 1000BASE-T mode.)

18.5 – Disable Automatic Pair Swap Correction

When bit 18.5 is set to “0”, the PHY automatically corrects pair swaps between subchannels A and B, and between subchannels C and D, due to “MDI/MDI-X crossover”. It will also correct pair swaps between subchannels C and D due to cabling errors. When bit 18.5 is set to “1”, the PHY does not correct pair swaps. Note that this control bit applies in all modes: 10BASE-T, 100BASE-TX, and 1000BASE-T.[2]

18.4 – Disable Polarity Correction

When bit 18.4 is set to “0”, the PHY automatically corrects polarity inversion on all the subchannels. When bit 18.4 is set to “1”, the PHY does not compensate for polarity inversions.

18.3 – Parallel-Detect Control

When bit 18.3 is “1”, a MII Register 4, bits [8:5], are taken into account when attempting to parallel-detect. This is the default behavior expected by the standard. Setting 18.3 to a “0” will result in Auto-Negotiation ignoring the advertised abilities, as specified in MII Register 4, during parallel detection of a non-auto-negotiating 10BASE-T or 100BASE-TX PHY.

18.2 – Disable Pulse Shaping Filter

When bit 18.2 is set to “1”, the 1000BASE-T two-tap digital transmit filter is disabled. This bit applies only in 1000BASE-T mode.

18.1 – Disable Automatic 1000BASE-T Next-Page Exchanges

Bit 18.1 is used to control the automatic exchange of 1000BASE-T Next-Pages defined in IEEE 802.3-2002 (Annex 40C). When this bit is set, the automatic exchange of these pages is disabled, and the control is returned to the user through the SMI after the base page has been exchanged. The user then has complete responsibility to:

- send the correct sequence of Next-Pages to the Link Partner, *and*
- determine common capabilities and force the device into the correct configuration following successful exchange of pages.

When bit 18.1 is reset to “0”, the 1000BASE-T related Next-Pages are automatically exchanged without user intervention. If the Next Page bit 4.15 was set by the user in the Auto-Negotiation Advertisement register at the time the Auto-Negotiation was restarted, control is returned to the user for additional Next-Pages following the 1000BASE-T Next-Page exchange.

If both 18.1 and 4.15 are reset when an Auto-Negotiation sequence is initiated, all Next-Page exchange is automatic, including sourcing of null pages. No user notification is provided until either Auto-Negotiation completes or fails. See the description of Register bit 4.15 for more details on standard Next-Page exchanges.

[1]This bit applies only in 1000BASE-T mode.

[2]Consistent with 10/100/1000BASE-T PHYs on the market today, this bit applies only when Auto-Negotiation is enabled; Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

18.0 – Enable 125MHz Free-Running Clock Output

When bit 18.0 is set to “1”, the CIS8204 provides a free-running, general-purpose 125MHz clock on the CLK125 output pin for use, for example, by the MAC, system manager CPU, or control logic. By default, this pin is enabled, and is always toggling (active), independent of the status of any link, unless a hardware reset is active (which also powers down the PLL). When disabled, this pin is normally driven low. Note that only PHY Port 0’s bit 18.0 controls the operation of CLK125.

21.20 Register 19 (13h) – Receive Error Counter Register

Bit	Name	Access	States	Reset Value
	Register 19 (13h) – Receive Error Counter Register			
15:8	Reserved	RO		00000000
7:0	Receive Error Counter	RO SC	Number of non-collision packets with receive errors since last read	00000000

19.15:8 – Reserved

19.7:0 – Receive Error Counter

Each time the PHY receives a non-collision packet containing at least one error, 19.7:0 is incremented. The counter will saturate at 0FFh. This register is cleared only when read, or upon either a hardware or software reset. These bits are valid only in 100BASE-TX and 1000BASE-T modes.

21.21 Register 20 (14h) – False Carrier Sense Counter Register

Bit	Name	Access	States	Reset Value
	Register 20 (14h) – False Carrier Sense Counter Register			
15:8	Reserved	RO		00000000
7:0	False Carrier Sense Counter	RO SC	Number of false carrier events since last read	00000000

20.15:8 – Reserved

20.7:0 – False Carrier Sense Counter

The PHY will increment 20.7:0 each time it detects a false carrier on the receive input. The counter will saturate at 0FFh. This register is cleared only when read, or upon either a hardware or software reset. These bits are valid only in 100BASE-TX and 1000BASE-T modes.

21.22 Register 21 (15h) – Disconnect Counter Register

Bit	Name	Access	States	Reset Value
	Register 21 (15h) – Disconnect Counter Register			
15:8	Reserved	RO		00000000
7:0	Disconnect Counter	RO SC	Number of disconnects since last read	00000000

21.15:8 – Reserved

21.7:0 – Disconnect Counter

The PHY will increment 21.7:0 each time the carrier integrity monitor (CIM) enters the “link unstable” state. The counter will saturate at 0FFh. This register is cleared only when read, or upon a hardware or software reset.

21.23 Register 22 (16h) – 10BASE-T Control & Status Register[1]

Bit	Name	Access	States	Reset Value
	Register 22 (16h) – 10BASE-T Control & Status Register			
15	Link Disable	R/W	1 = Disable link integrity test 0 = Enable link integrity test	0
14	Jabber Detect Disable	R/W	1 = Disable jabber detect 0 = Enable jabber detect	0
13	Disable 10BASE-T/100BASE-TX Echo Mode	R/W	1 = Disable 10BASE-T/100BASE-TX echo mode 0 = Enable 10BASE-T/100BASE-TX echo mode	0
12	SQE Disable Mode	R/W	1 = Disable SQE transmit 0 = Enable SQE transmit	0
11:10	10BASE-T Squelch Control	R/W	00 = Normal squelch 01 = Low squelch 10 = High squelch 11 = Reserved	00
9	Reserved	R/W		0
8	EOF Error Detected	RO SC	1 = EOF error detected since last read 0 = EOF error not detected since last read	0
7	10BASE-T Disconnect State	RO SC	1 = 10BASE-T link disconnected 0 = 10BASE-T link connected	0
6	10BASE-T Link Status	RO	1 = 10BASE-T link active 0 = 10BASE-T link inactive	0
5:3	Reserved	R/W	Must write to 000	000
2:0	Reserved	RO		000

22.15 – Disable Link-Integrity State Machine[1]

When bit 22.15 is set to “0”, the CIS8204 link integrity state machine runs automatically; it also controls link pass status. When bit 22.15 is set to “1”, the link integrity state machine is bypassed, and the PHY is forced into link pass status.

22.14 – Disable Jabber Detect[1]

When bit 22.14 is set to “0”, the CIS8204 automatically shuts off the transmitter when a transmission request exceeds the IEEE-specified time limit. When bit 22.14 is set to “1”, transmission requests are allowed to be arbitrarily long without shutting down the transmitter.

22.13 – Disable 10BASE-T/100BASE-TX Echo Mode[1]

When bit 22.13 is set to “1”, the logical state of the TX_EN pin will *not* echo onto the CRS pin, effectively disabling CRS from being asserted in half-duplex operation. When bit 22.13 is set to “0”, the TX_EN pin will be echoed onto the CRS pin. Data on TXD is echo’d to RXD in 10BASE-T mode only.

22.12 – SQE Disable

When bit 22.12 is set to “1”, SQE (Signal Quality Error) pulses are not sent. Note that this control bit applies in 10BASE-T HDX mode only.

22.11:10 – Squelch Control[1]

When bits 22.11:10 are set to “00”, the CIS8204 uses the squelch threshold levels prescribed by the IEEE’s 10BASE-T specification. When bits 22.11:10 are set to “01”, the squelch level is decreased, which may improve the bit error rate performance on long loops. When bits 22.11:10 are set to “10”, the squelch level is increased, which may improve the bit error rate in high-noise environments.

[1]The bits in this register apply only in 10BASE-T mode, except for bit 22.13, which applies to both 10BASE-T and 100BASE-TX modes.

22.9, 22.2:0 – Reserved

22.8 – EOF Error[1]

When bit 22.8 returns a "1", a defective EOF (End-of-Frame) sequence has been received since the last time this bit was read. This bit is automatically set to "0" when it is read.

22.7 – 10BASE-T Disconnect State

Bit 22.7 is set to "1" if the 10BASE-T connection has been broken by the carrier integrity monitor since the last read of this bit; otherwise, this bit is set to "0".

22.6 – 10BASE-T Link Status

Bit 22.6 is set to "1" if the 10BASE-T link is active; otherwise, this bit is set to "0".

22.5:3 – Reserved - Must write to 000

[1]The bits in this register apply only in 10BASE-T mode, except for bit 22.13, which applies to both 10BASE-T and 100BASE-TX.

21.24 Register 23 (17h) – Extended PHY Control Register #1

Bit	Name	Access	States	Reset Value
	Register 23 (17h) – Extended PHY Control Register #1			
15:12	MAC Interface Mode Select	R/W	0000 = Enable GMII/MII (default) 0001 = Enable RGMII 0010 = Enable TBI 0011 = Enable RTBI 0100 to 1111 = Future use (reserved)	0000
11:9	MAC Interface and Digital I/O Power Supply Voltage Select	R/W	000 = I/O pins will operate from 3.3V supply 001 = I/O pins will operate from 2.5V supply 010 to 111 = Future use (reserved)	000
8	RGMII Skew Timing Compensation Enable	R/W	1 = Enable RGMII skew timing compensation 0 = Disable RGMII skew timing compensation	0
7	EWRAP Enable	R/W	1 = Enable EWRAP in TBI mode 0 = Disable EWRAP in TBI mode	0
6	TBI Bit Order Reversal Enable	R/W	1 = Enable TBI bit order reversal 0 = Disable TBI bit order reversal (default)	0
5	Reserved			
4:3	Activity LED Blink Rate Control	R/W	00 = 20Hz 01 = 10Hz 10 = 5Hz 11 = 2.5Hz	10
2	Activity LED Blink Enable	R/W	1 = Enable Activity LED Blink 0 = Disable Activity LED Blink	1
1	Link/Activity LED Combine	R/W	1 = Combine Link/Activity LED 0 = Link LED only	0
0	Reserved	RO		0

23.15:12 – MAC Interface Mode Select

When bits 23.15:12 are set per the values listed in the register table above, the respective MAC interfaces are enabled. The default system interface operating mode is GMII/MII.

23.11:9 – MAC Interface Voltage Select

Bits 23.11:9 specify the I/O voltage at which the MAC interface (GMII, MII, RGMII, TBI, or RTBI) and all other digital interface pins will be operated. Although each of the four PHYs can be *functionally operated* in different MII operating modes, all MII and I/O pins must be supplied with the same supply voltage, as the on-chip I/O power supply buses are common (tied together). By default, 3.3V GMII I/O operating conditions are used.[1] These bits are controlled by PHY0. These bits in PHY1:3 are ignored.

23.8 – Enable RGMII Timing Skew Compensation

Bit 23.8 enables a unique, on-chip timing circuit to compensate for sensitive RGMII timings, which normally must be addressed by using a “trombone shaped” timing delay on the PC board. See Section 24.9: "RGMII/RTBI Mode Timing" and the RGMII specification for more information. By default, this compensation circuit is disabled.

23.7 – EWRAP Enable

When bit 23.7 is set to “1” and bits 23.15:12 are set to “0010”, TBI loopback toward the MAC is enabled.

23.6 – TBI Bit Order Reversal Enable

Bit 23.6 allows the user to specify the bit order for the PCS only when TBI mode is selected. By default, reversing the TBI bit order, as defined in the IEEE standard, is disabled.

[1]To be compliant with the RGMII/RTBI standard, 23.11:9 must be set to “001” when the PHY is to be operated in RGMII/RTBI mode since the RGMII/RTBI standard specifies a 2.5V I/O supply.

23.5 – Reserved

23.4:3 – LED Activity Blink Rate Control

See Register 27 (1Bh) – Serial LED Control Register for other LED control bits.
Bits 23.4:3 specify the blink rate of the Link/Activity LED.

00 = 20Hz
01 = 10Hz
10 = 5Hz
11 = 2.5Hz

23.2 – Activity LED Blink Enable

When bit 23.2 is set to "1", the Link/Activity blink function is enabled. In the blinking state the Link/Activity LED operates as follows:

The LED is constantly on when the link is up and data is NOT being transmitted or recieved.
The LED will blink at the rate specified by bits 23.4:3 when the link is up AND data is being transmitted or received.

See Register 27 (1Bh) – Serial LED Control Register for other LED control bits.

23.1 – Combine LEDLink/Activity

When bit 23.1 is set to "1", the Link function is combined with the Activity function for the Link LED. For the Link LED to blink during data transfers (Activity), this bit and bit 23.2 must both be set to "1". See Register 27 (1Bh) – Serial LED Control Register for other LED control bits.

When this bit is set to "1" and bit 23.2 is set to "0", the Activity LED will come on when the link is up AND activity is detected.

23.0 – Reserved

21.25 Register 24 (18h) – Extended PHY Control Register #2

Bit	Name	Access	States	Reset Value
	Register 24 (18h) – Extended PHY Control Register #2			
15:13	100/1000BASE-T Edge Rate Control	R/W	011 = +3 edge rate (slowest) 010 = +2 edge rate 001 = +1 edge rate 000 = Nominal edge rate 111 = -1 edge rate 110 = -2 edge rate 101 = -3 edge rate 100 = -4 edge rate (fastest)	001
12:10	Reserved	R/W	Must write to 000	000
9:7	TX FIFO Depth Control for GMII, RGMII, TBI, and RTBI	R/W	000 = 5 symbols 001 = 4 symbols 010 = 3 symbols 011 = 2 symbols 100 = 1 symbol 101 to 111 = Reserved	100
6:4	RX FIFO Depth Control (TBI only)	R/W	000 = 5 symbols 001 = 4 symbols 010 = 3 symbols 011 = 2 symbols 100 = 1 symbol 101 to 111 = Reserved	100
3:1	Cable Length Status	RO	000 = cable length < 10m 001 = 10m < cable length < 20m 010 = 20m < cable length < 40m 011 = 40m < cable length < 80m 100 = 80m < cable length < 100m 101 = 100m < cable length <140m 110 = 140m < cable length <180m 111 = cable length > 180m	000
0	1000BASE-T Analog Loopback Control	R/W	1 = Enable 1000BASE-T analog loopback through the hybrid 0 = Disable 1000BASE-T analog loopback through the hybrid	0

24.15:13 – 100/1000BASE-T Edge Rate Control

Bits 24.15:13 control the transmit DAC slew rate in 100BASE-TX and 1000BASE-T modes only, as shown above. The difference between each setting is approximately 200ps to 300ps, with the “+3” setting resulting in the slowest edge rate, and the “-4” setting resulting in the fastest edge rate.

24.12:10 – Reserved - Must write to 000

24.9:7 – TX FIFO Depth Control[1]

Bits 24.9:7 control symbol buffering for the transmit synchronization FIFO used in GMII, RGMII, TBI, and RTBI modes.

During symbol transmission in GMII, RGMII, TBI, and RTBI modes, bits 24.9:7 control the depth of the FIFO, which directly determines the maximum transmittable packet size. An internal FIFO is used to synchronize the clock domains between the MAC transmit clock (e.g., GTX_CLK) and the PHY's clock (e.g., REFCLK), used to transmit symbols on the local PHY's twisted pair interface. By controlling the transmit synchronization FIFO depth with these three bits, the user sets the maximum packet size which can be successfully transmitted by the CIS8204.

$$\text{FIFO Setting} = \frac{\text{((Freq. Tolerance Error of MAC Clock + Freq. Tolerance Error of PHY Clock) x Max. Packet Size)}}{1{,}000{,}000},$$

where the frequency tolerance offset is in ppm, the maximum packet size is in bytes, and the FIFO setting is in symbols.[2]

For example, when GTX_CLK = 125MHz ±100ppm, REFCLK = 125MHz ±50ppm, and the maximum packet size is 9600 bytes (a jumbo packet):

FIFO Setting = ((100ppm+ 50ppm) x 9600 bytes)/1,000,000 = 2 symbols of FIFO buffering = Register bit setting of "011".

24.6:4 – RX FIFO Depth Control (TBI Mode Only)[1]

Used in TBI mode only, bits 24.6:4 control symbol buffering as determined by the receive synchronization FIFO.[2]

24.3:1 – Cable Quality Status

Valid only in 100/1000BASE-T modes, bits 24.3:1 indicate the *approximate* effective electrical length of the cable in meters, as shown in register 22.25.

[1]The TX and RX FIFOs are not used in MII mode for 10BASE-T and 100BASE-TX.

[2]When using standard 1518-byte packets and following the frequency tolerance for the clocks, a standard inter-packet gap (IPG) of twelve symbols is required by the IEEE 802.3 specification. When using larger, non-standard packets, a larger IPG is required due to the possible compression of the IPG at the output of the FIFO. Cicada recommends increasing the IPG size by one cycle for each additional symbol of buffering used in the FIFO. For the default FIFO buffering of 1 symbol, an IPG of 12 is recommended. For a FIFO buffering of 5 symbols, an IPG of 16 is recommended.

24.0 – 1000BASE-T Analog Loopback Control

This bit is valid only in 1000BASE-T mode. When asserted, bit 24.0 enables analog loopback through the CIS8204's internal hybrid. Because loopback occurs at the hybrid, the transmit/receive signal will be observed on the media (cable). This bit should always be disabled in normal operating modes. See MII Register bit 0.14 for information about the IEEE 802.3 specified loopback operation.[1]

[1]The use of this function requires special considerations. Please contact Application Support at Cicada for further information.

21.26 Register 25 (19h) – Interrupt Mask Register

Bit	Name	Access	States	Reset Value
	Register 25 (19h) – Interrupt Mask Register			
15	Interrupt Pin Enable	R/W	1 = Enable interrupt pin 0 = Disable interrupt pin	0
14	Speed State-Change Interrupt Mask	R/W	1 = Enable Speed interrupt 0 = Disable Speed interrupt	0
13	Link State-Change Interrupt Mask	R/W	1 = Enable Link interrupt 0 = Disable Link interrupt	0
12	FDX State-Change Interrupt Mask	R/W	1 = Enable FDX interrupt 0 = Disable FDX interrupt	0
11	Auto-Negotiation Error Interrupt Mask	R/W	1 = Enable Auto-Negotiation Error interrupt 0 = Disable Auto-Negotiation Error interrupt	0
10	Auto-Negotiation-Done Interrupt Mask	R/W	1 = Enable Auto-Negotiation-Done interrupt 0 = Disable Auto-Negotiation-Done interrupt	0
9	Page-Received Interrupt Mask	R/W	1 = Enable Page-Received interrupt 0 = Disable Page-Received interrupt	0
8	Symbol Error Interrupt Mask	R/W	1 = Enable Symbol Error interrupt 0 = Disable Symbol Error interrupt	0
7	Descrambler Lock-Lost Interrupt Mask	R/W	1 = Enable Lock-Lost interrupt 0 = Disable Lock-Lost interrupt	0
6	MDI Crossover Interrupt Mask	R/W	1 = Enable MDI Crossover interrupt 0 = Disable MDI Crossover interrupt	0
5	Polarity-Change Interrupt Mask	R/W	1 = Enable Polarity-Change interrupt 0 = Disable Polarity-Change interrupt	0
4	Jabber-Detect Interrupt Mask	R/W	1 = Enable Jabber-Detect interrupt 0 = Disable Jabber-Detect interrupt	0
3	False Carrier Interrupt Mask	R/W	1 = Enable False Carrier interrupt 0 = Disable False Carrier interrupt	0
2	Parallel-Detect Interrupt Mask	R/W	1 = Enable Parallel-Detect interrupt 0 = Disable Parallel-Detect interrupt	0
1	MASTER/SLAVE Interrupt Mask	R/W	1 = Enable MASTER/SLAVE interrupt 0 = Disable MASTER/SLAVE interrupt	0
0	RX_ER Interrupt	R/W	1 = Enable RX_ER interrupt 0 = Disable RX_ER interrupt	0

25.15 – Interrupt Pin Enable

When bit 25.15 is set to “1”, the hardware interrupt is enabled, meaning that the state of the external interrupt pin (MDINT#, which is active low) can be influenced by the state of the Interrupt Status bit (26.15). When bit 25.15 is set to “0”, the interrupt status bits (Register 26) continue to be set in response to interrupts, but the interrupt hardware pin MDINT# on the CIS8204 will not be influenced by this particular PHY. The MDINT# hardware pin is essentially a logical AND-OR-INVERT function of the four individual pairs of Register bits (25.15 and 26.15).

25.14 – Speed State-Change Interrupt Mask

When bit 25.14 is set to “1”, the Speed State-Change interrupt is enabled.

25.13 – Link State-Change Interrupt Mask

When bit 25.13 is set to “1”, the Link State-Change interrupt is enabled.

25.12 – FDX State-Change Interrupt Mask

When bit 25.12 is set to “1”, the FDX State-Change interrupt is enabled.

25.11 – Auto-Negotiation Error Interrupt Mask

When bit 25.11 is set to "1", the Auto-Negotiation Error interrupt is enabled.

25.10 – Auto-Negotiation-Done Interrupt Mask

When bit 25.10 is set to "1", the Auto-Negotiation-Done interrupt is enabled.

25.9 – Page-Received Interrupt Mask[1]

When bit 25.9 is set to "1", the Page-Received interrupt is enabled.

25.8 – Symbol Error Interrupt Mask[1]

When bit 25.8 is set to "1", the Symbol Error interrupt is enabled.

25.7 – Descrambler Lock-Lost Interrupt Mask[1]

When bit 25.7 is set to "1", the Descrambler Lock-Lost interrupt is enabled.

25.6 – MDI-Crossover Interrupt Mask[2]

When bit 25.6 is set to "1", the MDI Crossover Status- interrupt is enabled.

25.5 – Polarity-Change Interrupt Mask

When bit 25.5 is set to "1", the Polarity-Change interrupt is enabled.

25.4 – Jabber-Detect Interrupt Mask[3]

When bit 25.4 is set to "1", the Jabber-Detect interrupt is enabled.

25.3 – False Carrier Interrupt Mask[1]

When bit 25.3 is set to "1", the False Carrier interrupt is enabled.

25.2 – Parallel-Detect Error Interrupt Mask[3]

When bit 25.2 is set to "1", the Parallel-Detect error interrupt is enabled,

25.1 – MASTER/SLAVE Resolution Error Interrupt Mask[4]

When bit 25.1 is set to "1", the MASTER/SLAVE Resolution Error interrupt is enabled.

25.0 – RX_ER Interrupt[3]

When bit 25.0 is set to "1", the RX_ER interrupt is enabled.

[1]This bit applies only in 100BASE-TX and 1000BASE-T modes.

[2]Consistent with 10/100/1000BASE-T PHYs on the market today, this bit applies only when Auto-Negotiation is enabled.

[3]This bit applies only in 10BASE-T mode.

[4]This bit applies only in 1000BASE-T mode.

21.27 Register 26 (1Ah) – Interrupt Status Register

Bit	Name	Access	States	Reset Value
	Register 26 (1Ah) – Interrupt Status Register			
15	Interrupt Status	RO SC	1 = Interrupt pending 0 = No interrupt pending	0
14	Speed State-Change Interrupt Status	RO SC	1 = Speed interrupt pending	0
13	Link State-Change Interrupt Status	RO SC	1 = Link state-change pending	0
12	FDX State-Change Interrupt Status	RO SC	1 = FDX interrupt pending	0
11	Auto-Negotiation Error Interrupt Status	RO SC	1 = Auto-Negotiation Error interrupt pending	0
10	Auto-Negotiation-Done Interrupt Status	RO SC	1 = Auto-Negotiation-Done interrupt pending	0
9	Page-Received Interrupt Status	RO SC	1 = Page-Received interrupt pending	0
8	Symbol Error Interrupt Status	RO SC	1 = Symbol Error interrupt pending	0
7	Descrambler Lock-Lost Interrupt Status	RO SC	1 = Lock-Lost interrupt pending	0
6	MDI Crossover Interrupt Status	RO SC	1 = MDI Crossover interrupt pending	0
5	Polarity-Change Interrupt Status	RO SC	1 = Polarity-Change interrupt pending	0
4	Jabber-Detect Interrupt Status	RO SC	1 = Jabber-Detect interrupt pending	0
3	False Carrier Interrupt Status	RO SC	1 = False Carrier interrupt pending	0
2	Parallel-Detect Interrupt Status	RO SC	1 = Parallel-Detect error interrupt pending	0
1	MASTER/SLAVE Interrupt Status	RO SC	1 = MASTER/SLAVE Error interrupt pending	0
0	RX_ER Interrupt Status	RO	1 = RX_ER interrupt pending 0 = No RX_ER interrupt pending	0

26.15 – Interrupt Status

When bit 26.15 is set to “1”, an unacknowledged interrupt is pending. The cause of the interrupt can be determined by reading the interrupt status bits in this register. This bit is automatically cleared when read.

26.14 – Speed State-Change Interrupt Status

When the operating speed of the PHY changes, bit 26.14 is set to “1” if bit 25.14 is also set to “1”. This bit is automatically cleared when read.

26.13 – Link State-Change Interrupt Status

When the link status of the PHY changes, bit 26.13 is set to “1” if bit 25.13 is also set to “1”. This bit is automatically cleared when read.

26.12 – FDX State-Change Interrupt Status

When the FDX/HDX status of the PHY changes, bit 26.12 is set to “1” if bit 25.12 is also set to “1”. This bit is automatically cleared when read.

26.11 – Auto-Negotiation Error Interrupt Status

When an error is detected by the Auto-Negotiation state machine, bit 26.11 is set to “1” if bit 25.11 is also set to “1”. This bit is automatically cleared when read.

26.10 – Auto-Negotiation-Done Interrupt Status

When the Auto-Negotiation state machine finishes a negotiation process, bit 26.10 is set to “1” if bit 25.10 is also set to “1”. This bit is automatically cleared when read.

26.9 – Page-Received Interrupt Status

When a new Next-Page is received, bit 26.9 is set to “1” if bit 25.9 is also set to “1”. This bit is automatically cleared when read.

26.8 – Symbol Error Interrupt Status[1]

When a symbol error is detected by the descrambler, bit 26.8 is set to “1” if bit 25.8 is also set to “1”. This bit is automatically cleared when read.

26.7 – Descrambler Lock-Lost Interrupt Status[1]

When the descrambler loses lock, bit 26.7 is set to “1” if bit 25.7 is also set to “1”. This bit is automatically cleared when read.

26.6 – MDI Crossover Interrupt Status[2]

When the MDI crossover status of the PHY changes, bit 26.6 is set to “1” if bit 25.6 is also set to “1”. This bit is automatically cleared when read.

26.5 – Polarity-Change Interrupt Status

When a polarity status error of the PHY changes, bit 26.5 is set to “1” if bit 25.5 is also set to “1”. This bit is automatically cleared when read.

26.4 – Jabber-Detect Interrupt Status[3]

When “jabber” is detected, bit 26.4 is set to “1” if bit 25.4 is also set to “1”. This bit is automatically cleared when read.

26.3 – False Carrier Interrupt Status[1]

When a false carrier is detected, bit 26.3 is set to “1” if bit 25.3 is also set to “1”. This bit is automatically cleared when read,

26.2 – Parallel-Detect Error Interrupt Status

When a Parallel-Detect error is detected, bit 26.2 is set to “1” if bit 25.2 is also set to “1”. This bit is automatically cleared when read.

26.1 – MASTER/SLAVE Resolution Error Interrupt Status[4]

When a MASTER/SLAVE resolution error is detected, bit 26.1 is set to “1” if bit 25.1 is also set to “1”. This bit is automatically cleared when read.

26.0 – RX_ER Interrupt Status

When an RX_ER condition occurs, bit 26.0 is set to “1”. This bit is automatically cleared when read.

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[1] This bit applies only in 100BASE-TX and 1000BASE-T modes.

[2] Consistent with 10/100/1000BASE-T PHYs on the market today, this bit applies only when Auto-Negotiation is enabled; Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

[3] This bit applies only in 10BASE-T mode.

[4] This bit applies only in 1000BASE-T mode.

21.28 Register 27 (1Bh) – Serial LED Control Register

See Register 23 (17h) – Extended PHY Control Register #1 for other LED control bits.

Register 27 (1Bh) – Serial LED Control Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Reserved	RO		0
14	LED Preamble Enable	R/W	1 = Enable preamble in frame 0 = Disable preamble in frame	0
13	FDX/HDX LED Force On	R/W	1 = FDX/HDX LED forced on 0 = FDX/HDX LED not forced on	0
12	FDX/HDX LED Disable	R/W	1 = Disable FDX/HDX LED 0 = Enable FDX/HDX LED	0
11	Link 10, 100, 1000 LEDs Force On	R/W	1 = Link 10, 100, 1000 LEDs forced on 0 = Link 10, 100, 1000 LEDs not forced on	0
10	Link 10, 100, 1000 LEDs Disable	R/W	1 = Disable Link 10, 100, 1000 LEDs 0 = Enable Link 10, 100, 1000 LEDs	0
9	Link Status LED Force On	R/W	1 = Link LED forced on 0 = Link LED not forced on	0
8	Link Status LED Disable	R/W	1 = Disable Link Quality LED 0 = Enable Link Quality LED	1
7	Link/Activity LED Force On	R/W	1 = Link/Activity LED forced on 0 = Link/Activity LED not forced on	0
6	Link/Activity LED Disable	R/W	1 = Disable Activity LED 0 = Enable Activity LED	0
5	Transmit LED Force On	R/W	1 = Transmit LED forced on 0 = Transmit LED not forced on	0
4	Transmit LED Disable	R/W	1 = Disable Transmit LED 0 = Enable Transmit LED	1
3	Receive LED Force On	R/W	1 = Receive LED forced on 0 = Receive LED not forced on	0
2	Receive LED Disable	R/W	1 = Disable Receive LED 0 = Enable Receive LED	1
1	Collision-Detect LED Force On	R/W	1 = Collision-Detect LED forced on 0 = Collision-Detect LED not forced on	0
0	Collision-Detect LED Disable	R/W	1 = Disable Collision-Detect LED 0 = Enable Collision-Detect LED	1

27.15 – Reserved

27.14 – Preamble Enable[1]

When bit 27.14 is set to “1” (preambled mode), the serial LED interface will transmit a preamble of thirty-six “1”s followed by one “0” before commencing LED data transmission. This preamble can be used by an external LED driver circuit to detect a new frame and change the state of the LEDs only after a new frame is received.

When bit 27.14 is set to “0” (un-preambled mode), a maximum of thirty-six data bits are clocked out sequentially without a preamble. At the end of a frame, the clock is stopped for 10ms. This pattern is repeated indefinitely. For the un-preambled mode, this data could be clocked into a shift register, whose outputs drive LEDs directly. In this case, the shift register outputs will flicker as the data is clocked in. However, since the clock is stopped for 10ms after the shift register is loaded, the flicker would not be perceptible to a human observer.

27.13 – FDX/HDX LED Force On[2]

When bit 27.13 is set to “1”, the FDX/HDX LED status bit is asserted (set to “1”).

[1] If this bit is set in the MII register of **any** PHY on the CIS8204, LED preamble transmission will be enabled.

[2] This control has effect only if the corresponding LED status bit is enabled.

27.12 – FDX/HDX LED Disable

When bit 27.12 is set to “1”, the FDX/HDX LED status bit is disabled. If this bit is set, the data bit is not transmitted, so the transmit frame length is reduced by one bit.

27.11 – Link 10, 100, 1000 LEDs Force On[1]

When bit 27.11 is set to “1”, the three LED status bits (Link10, Link100, and Link1000) are asserted.

27.10 – Link 10, 100, 1000 LEDs Disable

When bit 27.10 is set to “1”, the Link10, Link100, Link1000 LED status bits are disabled. If this bit is set, the data bit is not transmitted, so the transmit frame length is reduced by three bits.

27.9 – Link Status LED Force On[1]

When bit 27.9 is set to “1”, the Link Status LED bit is asserted. This bit is valid in both 1000BASE-T and 100BASE-T modes.

27.8 – Link Status LED Disable

When bit 27.8 is set to “1”, the Link Status LED is disabled, which is the default state. If this bit is set, the data bit is not transmitted, so the transmit frame length is reduced by one bit. Enabled by writing this bit to a “0”, the Link Status LED bit is asserted whenever a link has been established. This bit is valid in both 1000BASE-T and 100BASE-T modes.

27.7 – Link/Activity LED Force On[1]

When bit 27.7 is set to “1”, the Link/Activity LED is forced on. See Register 23 (17h) – Extended PHY Control Register #1 for blink and Link/Activity control.

27.6 – Link/Activity LED Disable

When bit 27.6 is set to “1”, the Link/Activity LED is disabled. If this bit is set, the data bit is not transmitted, so the transmit frame length is reduced by one bit. See Register 23 (17h) – Extended PHY Control Register #1 for blink and Link/Activity control.

27.5 – Transmit LED Force On[1]

When bit 27.5 is set to “1”, the Transmit LED is forced on.

27.4 – Transmit LED Disable

When bit 27.4 is set to “1”, the Transmit LED is disabled. If this bit is set, the data bit is not transmitted, so the transmit frame length is reduced by one bit.

27.3 – Receive LED Force On[1]

When bit 27.3 is set to “1”, the Receive LED is forced on.

27.2 – Receive LED Disable

When bit 27.2 is set to “1”, the Receive LED is disabled. If this bit is set, the data bit is not transmitted, so the transmit frame length is reduced by one bit.

27.1 – Collision-Detect LED Force On[1]

When bit 27.1 is set to “1”, the Collision-Detect LED is forced on.

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[1]This control bit has effect only if the corresponding LED status bit is enabled.

27.0 – Collision-Detect LED Disable

When bit 27.0 is set to “1”, the Collision-Detect LED is disabled. If this bit is set, the data bit is not transmitted, so the transmit frame length is reduced by one bit.

Note: For simplicity, the default states of the LED bits have been chosen to enable the five most commonly needed LEDs in a triple speed Ethernet application:

- FDX/HDX
- Link10
- Link100
- Link1000
- Activity

Since preamble suppression is the default operating mode, this results in the normal length of a serial LED data frame of twenty bits (five bits per PHY x four PHYs).

21.29 Register 28 (1Ch) – Auxiliary Control & Status Register

Bit	Name	Access	States	Reset Value
	Register 28 (1Ch) – Auxiliary Control & Status Register			
15	Auto-Negotiation Complete	RO	1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete	0
14	Auto-Negotiation Disabled	RO	1 = Auto-Negotiation was disabled 0 = Auto-Negotiation is enabled	0
13	MDI/MDI-X Crossover Indication	RO	1 = MDI/MDI-X crossover detected 0 = MDI/MDI-X crossover not detected	0
12	CD Pair Swap	RO	1 = CD pairs are swapped 0 = CD pairs are not swapped	0
11	A Polarity Inversion	RO	1 = Polarity swapped on pair A 0 = Polarity not swapped on pair A	0
10	B Polarity Inversion	RO	1 = Polarity swapped on pair B 0 = Polarity not swapped on pair B	0
9	C Polarity Inversion	RO	1 = Polarity swapped on pair C 0 = Polarity not swapped on pair C	0
8	D Polarity Inversion	RO	1 = Polarity swapped on pair D 0 = Polarity not swapped on pair D	0
7:6	Reserved	RO		00
5	FDX Status	RO	1 = FDX 0 = HDX	0
4:3	Speed Status	RO	00 = Speed is 10BASE-T 01 = Speed is 100BASE-TX 10 = Speed is 1000BASE-T 11 = Reserved	00
2	MODE/DUPLEX Pin Priority Select	R/W	1 = SMI registers have priority over MODE and DUPLEX pins 0 = MODE and DUPLEX pins have priority over SMI register settings, *unless* MODE[1:0]_n = 11b and DUPLEX_n = don't care.	0
1:0	Reserved	RO		00

28.15 – Auto-Negotiation Complete

This bit is a copy of bit 1.5, duplicated here for convenience.

28.14 – Auto-Negotiation Disabled

When bit 28.14 is read as a “1”, this bit indicates that the Auto-Negotiation process has been disabled. This happens only when register bit 0.12 is set to “0”.

28.13 – MDI/MDI-X Crossover Indication

When bit 28.13 returns a “1”, the Auto-Negotiation state machine has determined that crossover does not exist in the signal path. The crossover will therefore be performed internally to the PHY, as described by the MDI/MDI-X crossover specification.[1]

28.12 – CD Pair Swap[2]

When bit 28.12 returns a “1”, the PHY has determined that subchannel cable pairs C and D have been swapped between the far-end transmitted and the receiver. When bit 28.12 returns a “1”, the PHY internally swaps pairs C and D (as long as bit 18.5 is set to “0”).[1]

[1]This bit is valid only after descrambler lock has been achieved and as long as bit 18.5 is set to “0”.

[2]This bit applies only in 1000BASE-T mode.

28.11 – A Polarity Inversion

When bit 28.11 returns a “1”, the PHY has determined that the polarity of subchannel cable pair A has been inverted between the far-end transmitter and the near-end receiver. When bit 28.11 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.11 is valid only when bit 1.5 is set to “1”.

28.10 – B Polarity Inversion

When bit 28.10 returns a “1”, the PHY has determined that the polarity of subchannel cable pair B has been inverted between the far-end transmitter and the near-end receiver. When bit 28.10 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.10 is valid only when bit 1.5 is set to “1”.

28.9 – C Polarity Inversion[1]

When bit 28.9 returns a “1”, the PHY has determined that the polarity of subchannel cable pair C has been inverted between the far-end transmitter and the near-end receiver. When bit 28.9 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.9 is valid only when bit 1.5 is set to “1”.

28.8 – D Polarity Inversion[1]

When bit 28.8 returns a “1”, the PHY has determined that the polarity of subchannel cable pair D has been inverted between the far-end transmitter and the near-end receiver. When bit 28.8 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.8 is valid only when bit 1.5 is set to “1”.

28.7:6, 28.1:0 – Reserved

28.5 – FDX Status

Bit 28.5 indicates the actual FDX/HDX operating mode of the PHY.

28.4:3 – Speed Status

Bits 27.4:3 indicate the actual operating speed of the PHY.

28.2 – MODE/DUPLEX Pin Priority Select

Bit 28.2 determines whether the “MODE” and “DUPLEX” pins have priority over the MII register settings in determining the operating characteristics of the PHY. If bit 28.2 is a “0” (default value), then the MODE and DUPLEX pins have priority over any MII register settings, *unless* MODE[1:0]_n and DUPLEX_n = 11Xb, as shown in Table 21-4. If bit 28.2 is a “1”, then the MII register settings take precedence over the operating mode specified by the state of the MODE[1:0]_n and DUPLEX_n pins.

[1]This bit applies only in 1000BASE-T mode.

Table 21-4. MODE[1:0]_n and DUPLEX_n Pin Settings

MODE[1]_n	MODE[0]_n	DUPLEX_n	Effect
0	0	0	Force 10BASE-T, HALF duplex
0	0	1	Force 10BASE-T, FULL duplex
0	1	0	Force 100BASE-TX, HALF duplex
0	1	1	Force 100BASE-TX, FULL duplex
1	0	0	Force 1000BASE-T with SLAVE timing mode
1	0	1	Force 1000BASE-T with MASTER timing mode
1	1	X	Normal operating mode. Allow all PHY characteristics to be determined by the MII registers and the Auto-Negotiation or Parallel-Detect processes. These pins should be tied to VDDIO for normal operating mode.

Using the MODE and DUPLEX pins as described above does *not* change the state of any of a PHY's MII capability register bits (e.g., MII Registers 0, 1, 4, and 9). As specified by MII Registers 0, 1, 4, and 9, when bit 28.2 is set to "0", the MODE and DUPLEX pins effectively override the local PHY's operating capabilities for use in any subsequent Auto-Negotiation or Parallel-Detect process. These three pins affect only the following on a per-PHY basis:

- link speed: 10/100/1000
- duplex: full or half, for 10BASE-T and 100BASE-TX modes
- force MASTER or SLAVE modes for 1000BASE-T mode.

If the MII register settings are desired to take precedence over the MODE[1:0]_n and DUPLEX_n pins, then bit 28.2 must be written to a "1" after a hardware or software reset is completed.

21.30 Register 29 (1Dh) – Delay Skew Status Register

Bit	Name	Access	States	Reset Value
	Register 29 (1Dh) – Delay Skew Status Register			
15	Reserved	RO		0
14:12	Pair A Delay Skew	RO	Skew in integral symbol times	000
11	Reserved	RO		0
10:8	Pair B Delay Skew	RO	Skew in integral symbol times	000
7	Reserved	RO		0
6:4	Pair C Delay Skew	RO	Skew in integral symbol times	000
3	Reserved	RO		0
2:0	Pair D Delay Skew	RO	Skew in integral symbol times	000

29.15, 29.11, 29.7, 29.3 – Reserved

29.14:12 – Pair A Delay Skew[1]

Bits 29.14:12 indicate the additional delay (measured in integral symbol times) added internally at the pair A receiver input to align received symbols at pair A with the received symbols at the other three pairs.

29.10:8 – Pair B Delay Skew[1]

Bits 29.10:8 indicate the additional delay (measured in integral symbol times) added internally at the pair B receiver input to align received symbols at pair B with the received symbols at the other three pairs.

29.6:4 – Pair C Delay Skew[1]

Bits 29.6:4 indicate the additional delay (measured in integral symbol times) added internally at the pair C receiver input to align received symbols at pair C with the received symbols at the other three pairs.

29.2:0 – Pair D Delay Skew[1]

Bits 29.2:0 indicate the additional delay (measured in integral symbol times) added internally at the pair D receiver input to align received symbols at pair D with the received symbols at the other three pairs.

[1]This value is valid only in 1000BASE-T mode.

21.31 Register 30 (1Eh) – Reserved Register

Bit	Name	Access	States	Reset Value
	Register 30 (1Eh) – Reserved Register			
15:0	Reserved	RO		00000000 00000000

30.15:0 – Reserved

21.32 Register 31 (1Fh) – Reserved Register

Bit	Name	Access	States	Reset Value
	Register 31 (1Fh) – Reserved Register			
15:0	Reserved	RO		00000000 00000000

31.15:0 – Reserved

22 Electrical Specifications

22.1 Absolute Maximum Ratings

Temporary or prolonged operating conditions beyond those listed below may result in device failure and/or compromise long-term device reliability.

Table 22-1. Absolute Maximum Ratings

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{Storage}$	-65		150	°C	Storage temperature range.
T_J			+125	°C	Absolute maximum junction temperature.
T_A	0		70	°C	Ambient free-air operating temperature.
$V_{DD(Analog)}$	-0.5		4.0	V	DC voltage on analog I/O supply pin.
$V_{DD(IO)}$	-0.5		4.0	V	DC voltage on any digital I/O supply pin.
$V_{DD(5V)}$	-0.5		5.5	V	DC voltage on any 5V-tolerant digital input pin.
$V_{DD(Dig\text{-}Core)}$	-0.5		1.8	V	DC voltage on any digital core supply pin.
$V_{DD(Analog\text{-}Core)}$	-0.5		1.8	V	DC voltage on any analog core supply pin.
$V_{Pin(DC)}$	-0.5		V_{DD} + 0.5	V	DC voltage on any non-supply pin.
$V_{ESD(HBM)}$	2			kV	ESD voltage on any pin, per event, according to the Human Body Model.
$V_{ESD(MM)}$	200			V	ESD voltage on any pin, per event, according to the Machine Model.
CESD	4			kV	Cable-sourced ESD tolerance, per event, at 100 meters.
$I_{LATCHUP}$	-200		+200	mA	T = +85°C, valid for all I/O signal pins.

22.2 Recommended Operating Conditions

Table 22-2. Recommended Operating Conditions

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$VDDIO_{G,T,M}$	3.1	3.3	3.5	V	Digital I/O DC power supply voltage (GMII, TBI, and MII modes).
$VDDIO_{RGMII}$	2.3	2.5	2.7	V	Optional digital I/O DC power supply voltage (RGMII, RTBI modes only).[1]
VDDDIG	1.42	1.5	1.58	V	Digital core logic DC power supply voltage.
VDDPLL33 VDDLD VDDREC VREFP	3.135	3.3	3.465	V	Analog 3.3V DC power supply voltage.[2]
VDD15_n VDDPLL15	1.42	1.5	1.58	V	Analog 1.5V DC power supply voltage.
F_{REFCLK}	25	N/A	125	MHz	Local reference clock (REFCLK) nominal frequency.
$F_{TOL\ (REFCLK)}$	-50		+50	ppm	Reference clock frequency offset tolerance over specified temperature range (25MHz or 125MHz).
$F_{TOL\ (LINK)}$	-1500		+1500	ppm	Link partner frequency offset tolerance (for any link speed).
R_{EXT}		2.26		kΩ	External reference circuit bias resistor (1% tolerance).
C_{REF_FILT}		1.0		µF	External reference generator filter capacitor (10% tolerance).
N		1:1			Transformer nominal turns ratio (primary : secondary).

1 The CIS8204 is compliant with v1.3 of the RGMII specification.

2 VREFP provides the primary analog voltage reference. Careful attention to the PCB layout for this supply pin must be observed in order to avoid any bus drops, which would cause inaccuracy in the voltage reference generator. Separate traces for VREFP and VREFN to the 3.3V power regulator output and ground, respectively, are recommended. For compliance with the IEEE 802.3-2002 specification in regards to 100BASE-T amplitude, the tolerance of the 3.3V supply must be 2% or better. See Applications Note “CIS8204 Design and Layout Guidelines” for more information.

22.3 Thermal Application Data

Table 22-1. Thermal Application Data

Printed Circuit Board Conditions (JEDEC JESD51-9)	
PCB Layers	6
PCB Dimensions (mm x mm)	7602 x 114.3
PCB Thickness (mm)	1.6
Environment Conditions	
Maximum operation junction temperature (ºC)	125
Ambient free-air operating temperature (ºC)	70
Worst Case Power Dissipation (W)	5

Table 22-2. Thermal Application Data - 35mm Package

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
θ_{JA} (0 m/s airflow)		12.8		ºC/W	Junction-to-ambient thermal resistance
θ_{JA} (1 m/s airflow)		11.6		ºC/W	Junction-to-ambient thermal resistance
θ_{JA} (2 m/s airflow)		10.4		ºC/W	Junction-to-ambient thermal resistance

Table 22-3. Thermal Application Data - 27mm Package

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
θ_{JA} (0 m/s airflow)		13.9		ºC/W	Junction-to-ambient thermal resistance
θ_{JA} (1 m/s airflow)		12.9		ºC/W	Junction-to-ambient thermal resistance
θ_{JA} (2 m/s airflow)		11.5		ºC/W	Junction-to-ambient thermal resistance

22.4 Package Thermal Specifications

Table 22-4. Thermal Specifications - 388 pin HSBGA 35mm package

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_A	0		70	°C	Ambient free-air operating temperature
T_J			125	°C	Maximum operating junction temperature
θ_{JC}		5		°C/W	Junction-to-case thermal resistance
Ψ_{JT}		3.8		°C/W	Junction-to-top center of case thermal resistance

Table 22-5. Thermal Specifications - 388 pin HSBGA 27mm package

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_A	0		70	°C	Ambient free-air operating temperature
T_J			125	°C	Maximum operating junction temperature
θ_{JC}		5.4		°C/W	Junction-to-case thermal resistance
Ψ_{JT}		3.7		°C/W	Junction-to-top center of case thermal resistance

22.5 Current and Power Consumption - Application Scenarios

Operating Conditions, VDDPLL33/VDDLD/VDDREC/VREFP = 3.3V, VDDIO = 2.5V, VDDDIG/VDDPLL15/VDD15 = 1.5V, T_A = 25ºC, full duplex, 1000BASE-T RGMII 64 Byte Random data, R_{ext} = 2.26K.

Table 22-6. Current and Power Consumption - Application I

Symbol	Min	Typ	Max[1]	Unit	Parameter Description & Conditions
I_{VDDIO}		75	100	mA	Total 2.5V digital I/O supply current
I_{VDDDIG}		1584	1976	mA	Total 1.5V digital core supply current
$I_{VDDPLL33} + I_{VDDLD} + I_{VDDREC33} + I_{VREFP}$		392	428	mA	Total analog 3.3V supply current
$I_{VDDPLL15} + I_{VDDREC15}$		196	232	mA	Total analog 1.5V supply current
P_D		4190	5022	mW	Total power dissipation

[1] Max ratings at TA = 70ºC and supplies at +5%.

Operating Conditions, VDDPLL33/VDDLD/VDDREC33/VREFP = 3.3V, VDDIO = 3.3V, VDDDIG/VDDPLL15/VDD15 = 1.50V, T_A = 25ºC, full duplex, 1000BASE-T GMII 64 Byte Random data, R_{ext} = 2.26K.

Table 22-7. Current and Power Consumption - Application II

Symbol	Min	Typ	Max[1]	Unit	Parameter Description & Conditions
I_{VDDIO}		100	132	mA	Total 3.3V digital I/O supply current
I_{VDDDIG}		1584	1976	mA	Total 1.5V digital core supply current
$I_{VDDPLL} + I_{VDDLD} + I_{VDDREC33} + I_{VREFP}$		392	428	mA	Total analog 3.3V supply current
$I_{VDDPLL15} + I_{VDDREC15}$		196	232	mA	Total analog 1.5V supply current
$P_{D(VDDIO)}$		4297	5160	mW	Total digital I/O power dissipation

[1] Max ratings at TA = 70ºC and supplies at +5%.

22.6 Crystal Specifications

The following component specifications should be used to select a crystal for use with the CIS8204.

Table 22-8. Crystal Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{REF}		25		MHz	Fundamental mode, AT-cut type, parallel resonant crystal reference frequency.
$F_{STABILITY}$	-50		+50	ppm	Fundamental mode, AT-cut type, parallel resonant crystal frequency stability.
F_{OFFSET}	-30		+30	ppm	Fundamental mode, AT-cut type, parallel resonant crystal frequency offset.
C_L	18		20	pF	Crystal load capacitance.
C_{L-EXT}		33		pF	Crystal external load capacitors.
ESR		10	30	Ω	Equivalent Series Resistance of crystal.
P_D			0.5	mW	Crystal drive level.

A suitable crystal for use with the CIS8204 is:

- Fox Electronics, HC49S 250F-20.

23 DC Specifications (T_A = 0°C - 70°C)

23.1 Digital Pins

Table 23-1. Digital Pins Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$V_{OH(3.3)}$	2.4		VDDIO + 0.3	V	High Level Output High Voltage VDDIO = min, I_{OH} = -1.5mA, for $VDDIO_{(nom)}$= 3.3V
$V_{OH(2.5)}$	2.0		VDDIO + 0.3	V	High Level Output High Voltage VDDIO = min, I_{OH} = -1.0mA, for $VDDIO_{(nom)}$= 2.5V
V_{OL}	GND		0.5	V	Output Low Level Output Voltage
$V_{IH(3.3)}$	2.0			V	High Level Input Voltage, for $VDDIO_{(nom)}$= 3.3V
$V_{IH(2.5)}$	1.7			V	High Level Input Voltage, for $VDDIO_{(nom)}$= 2.5V
$V_{IL(3.3)}$			0.8	V	Low Level Input Voltage, for $VDDIO_{(nom)}$= 3.3V
$V_{IL(2.5)}$			0.7	V	Low Level Input Voltage, for $VDDIO_{(nom)}$= 2.5V
I_{Leak}	-10		10	µA	Input Leakage Current
V_{OLeak}	-10		10	µA	Output Leakage Current.

23.2 Twisted Pair Interface Pins

Table 23-1. TPI Transmitter DC Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$V_{OUT\text{-}DIFF}$ TX-10M	2.2		2.8	V	10Mb differential peak transmit output voltage.
$V_{OUT\text{-}DIFF}$ TX-100M	.95		1.05	V	100Mb differential peak transmit output voltage at nominal supply.
$V_{OUT\text{-}DIFF}$ TX-1000M	.95		1.05	V	1000Mb differential peak transmit output voltage at nominal supply.

24 AC Timing Specifications

24.1 GMII Mode Transmit (from MAC to PHY) Timing (1000BASE-T)

For GMII mode, the following specifications are valid only when the I/O power supply (VDDIO) is 3.3V, ±5%, and the MAC I/F selection bits have been set to GMII mode. See MII Register 23 for more information.

Table 24-1. GMII Mode Transmit AC Timing Specifications (1000BASE-T)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{GTX\_CLK\text{-}Period}$		8.0		ns	GTX_CLK_n clock period.
$F_{TOL\text{-}GTX\_CLK}$	-100		+100	ppm	GTX_CLK_n frequency offset tolerance.
$T_{GTX\_CLK\text{-}High}$	2.5			ns	GTX_CLK_n minimum pulse width high.
$T_{GTX\_CLK\text{-}Low}$	2.5			ns	GTX_CLK_n minimum pulse width low.
$T_{GTX\_CLK\text{-}Setup}$	2.0			ns	GMII data TXD[7:0]_n, TX_ER_n, TX_EN_n setup time.
$T_{GTX\_CLK\text{-}Hold}$	0.0			ns	GMII data TXD[7:0]_n, TX_ER_n, TX_EN_n hold time.
t_R			1.0	ns	GTX_CLK_n clock rise time, measured from 0.7V to 1.9V.
t_F			1.0	ns	GTX_CLK_n clock fall time, measured from 0.7V to 1.9V.

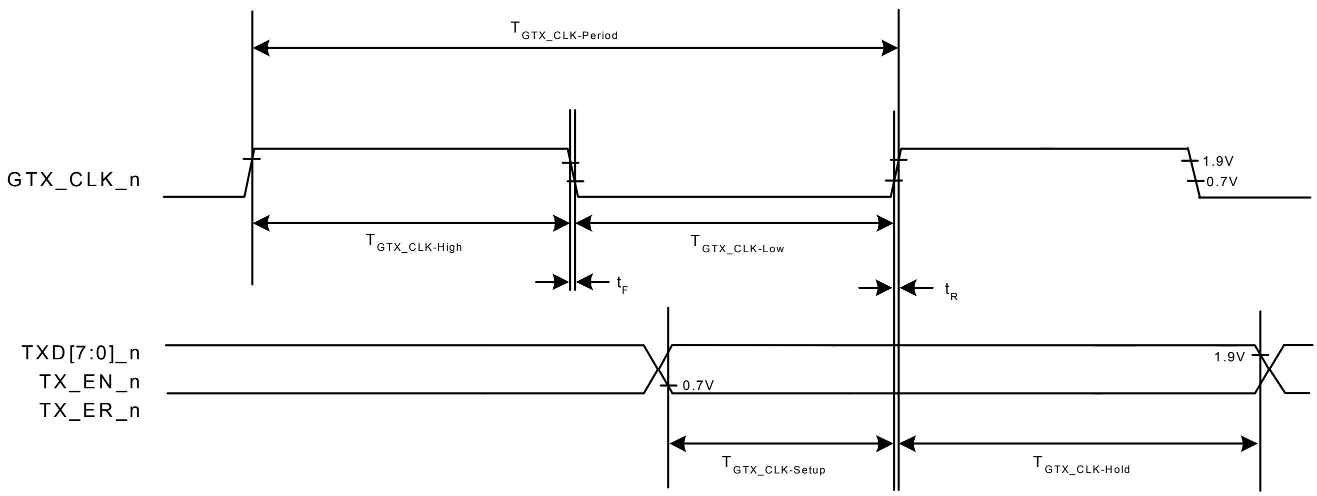


Figure 24-1. GMII Transmit AC Timing in 1000BASE-T Mode

24.2 GMII Mode Receive (from PHY to MAC) Timing (1000BASE-T)

For GMII mode, the following specifications are valid only when the I/O power supply (VDDIO) is 3.3V, ±5%, and the MAC I/F selection bits have been set to GMII mode. See MII Register 23 for more information.

Table 24-2. GMII Mode Receive AC Timing Specifications (1000BASE-T)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{RX\_CLK-Period}$		8.0		ns	RX_CLK_n clock period.
F_{TOL-RX_CLK}	-100		+100	ppm	RX_CLK_n frequency offset tolerance.
$T_{RX\_CLK-High}$	2.5			ns	RX_CLK_n minimum pulse width high.
$T_{RX\_CLK-Low}$	2.5			ns	RX_CLK_n minimum pulse width low.
$T_{RX\_CLK-Setup}$	2.5			ns	RXD[7:0]_n, RX_DV_n, RX_ER_n setup time to RX_CLK_n
$T_{RX\_CLK-Hold}$	0.5			ns	RXD[7:0]_n, RX_DV_n, RX_ER_n hold time to RX_CLK_n
t_R			1.0	ns	RX_CLK_n clock rise time, measured from 0.7V to 1.9V.
t_F			1.0	ns	RX_CLK_n clock fall time, measured from 0.7V to 1.9V.

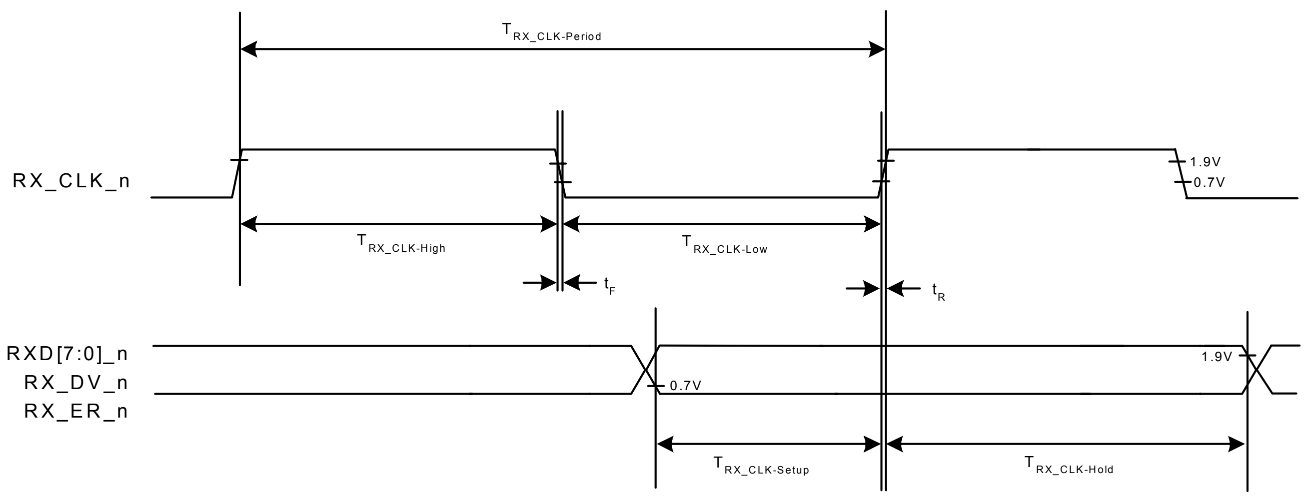


Figure 24-2. GMII Receive AC Timing in 1000BASE-T Mode

24.3 MII Transmit Timing (100Mb/s)

The following specifications are valid only when the I/O power supply (VDDIO) is 3.3V, ±5%, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 24-3. MII Transmit AC Timing Specifications (100Mb/s)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TX\_CLK-Delay}$	0		25	ns	Delay from TX_CLK_n to TXD[3:0]_n, TX_EN_n, TX_ER_n.
$T_{TX\_CLK-Duty}$	35		65	%	TX_CLK_n duty cycle.

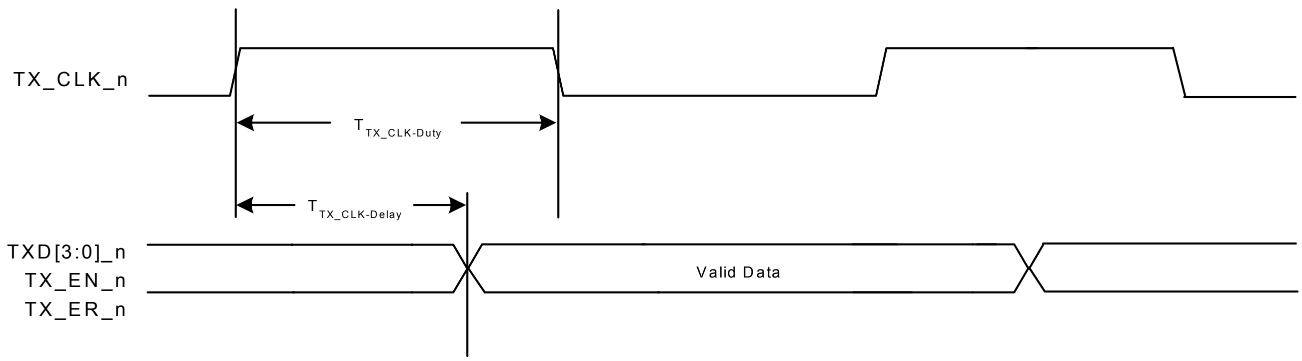


Figure 24-3. MII Transmit AC Timing (100Mb/s)

24.4 MII Receive Timing (100Mb/s)

The following specifications are valid only when the I/O power supply (VDDIO) is 3.3V, ±5%, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 24-4. MII Receive AC Timing Specifications (100Mb/s)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{RX\_CLK-Setup}$	10			ns	RXD[3:0]_n,RX_DV_n, RX_ER_n setup time to RX_CLK_n.
$T_{RX\_CLK-Hold}$	10			ns	RXD[3:0]_n, RX_DV_n, RX_ER_n hold time to RX_CLK_n.

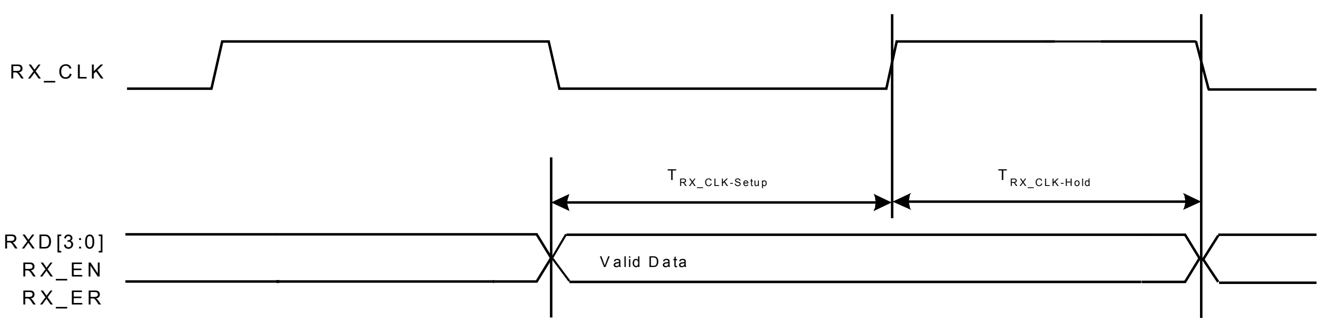


Figure 24-4. MII Receive AC Timing (100Mb/s)

24.5 100BASE-TX Transmit Packet Deassertion Timing

The following specifications are valid only when the I/O power supply (VDDIO) is 3.3V, ±5%, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 24-5. 100BASE-TX Transmit Packet Deassertion AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TPI\_A\text{-}Delay}$			6.0	bits	TX_CLK_n to TPI transmit channel “A” idling time.[1]

[1] For symbol mode, because TX_EN_n has no meaning, deassertion is measured from the first rising edge of TX_CLK_n occurring after the deassertion of a data nibble on the transmit MII to the last bit (LSB) of that nibble when it deasserts on the wire. 1 bit time = 10ns in 100Mb/s mode.

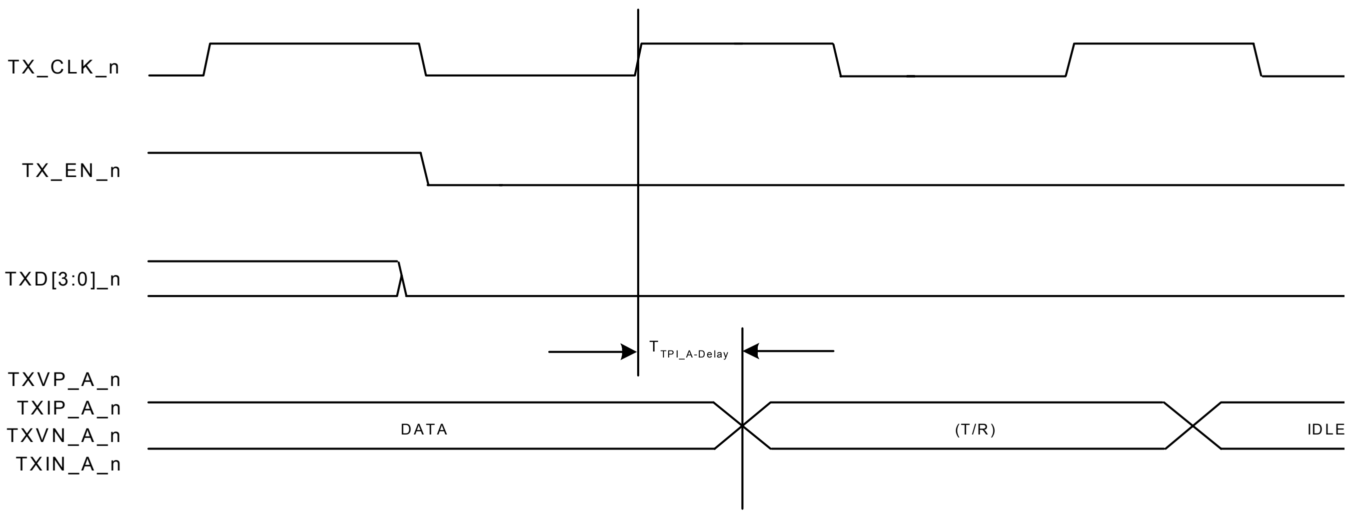


Figure 24-5. 100BASE-TX Transmit Packet Deassertion AC Timing

24.6 100BASE-TX Transmit Timing ($t_{R/F}$ & Jitter)[1]

The following specifications are valid only when the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 24-6. 100BASE-TX Transmit AC Timing Specifications ($t_{R/F}$ & Jitter)[1]

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
t_R, t_F	3	4	5	ns	TPI transmit channel “A” rise and fall times taken at 10% and 90% of the +1 or -1 amplitude.
$t_{Mismatch}$			500	ps	Difference between the maximum and minimum of all rise and fall times of TPI transmit channel “A”.
J_{TPI_A}			1.4	ns	TPI transmit channel “A” jitter.

[1] Worst case, supplies ±5%, T_A = 70°C

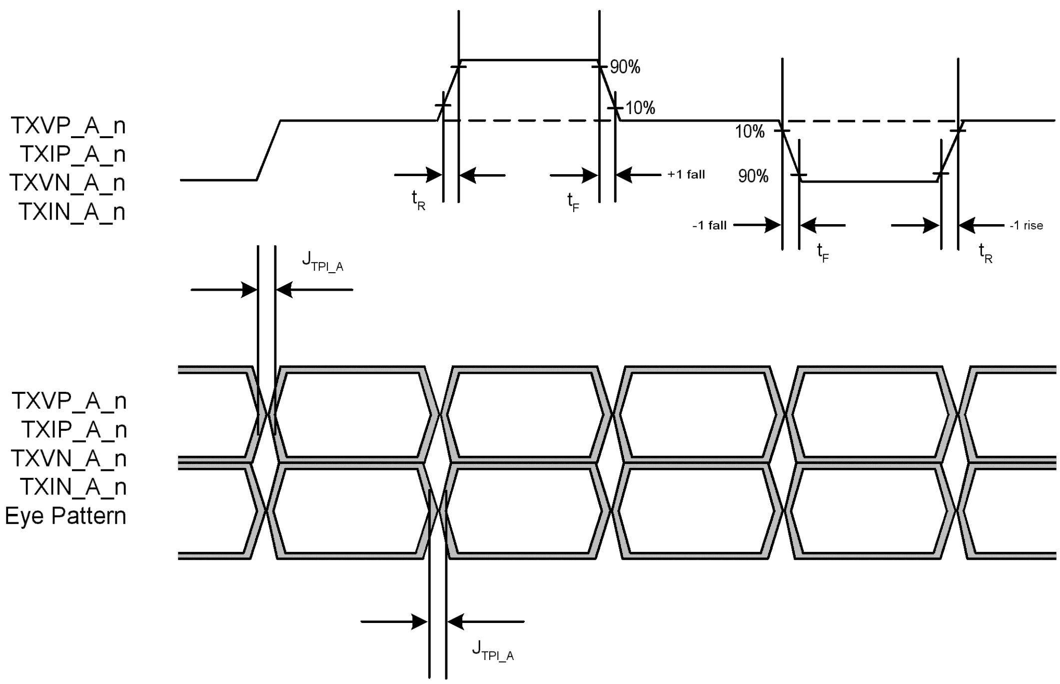


Figure 24-6. 100BASE-TX Transmit AC Timing ($t_{R/F}$ & Jitter)

24.7 100BASE-TX Receive Packet Latency Timing

The following specifications are valid only when the I/O power supply (VDDIO) is 3.3V, ±5%, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 24-7. 100BASE-TX Receive Packet Latency AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{CRS\_ON\text{-}Delay}$			17.5	bits[1]	Carrier Sense ON delay.
$T_{RXD\text{-}Delay}$			21	bits	Receive data latency.

[1] 1 bit time = 10ns in 100Mb/s mode.

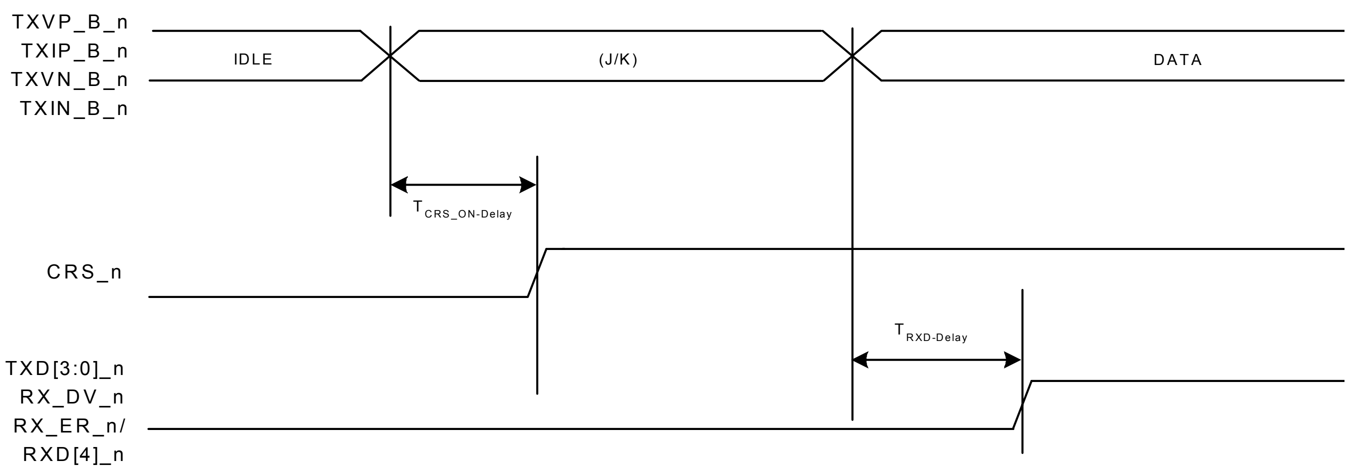


Figure 24-7. 100BASE-TX Receive Packet Latency AC Timing

24.8 100BASE-TX Receive Packet Deassertion Timing

The following specifications are valid only when the I/O power supply (VDDIO) is 3.3V, ±5%, and the MAC I/F selection bits have been set to GMII/MII mode. See MII Register 23 for more information.

Table 24-8. 100BASE-TX Receive Packet Deassertion AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{CRS\_OFF\text{-}Delay}$			21.5	bits[1]	Carrier Sense OFF delay.

[1] 1 bit time = 10ns in 100Mb/s mode.

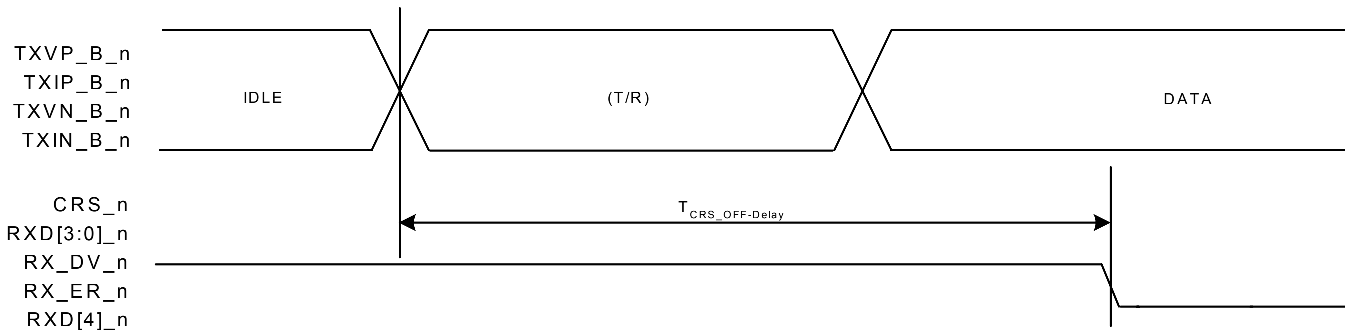


Figure 24-8. 100BASE-TX Receive Packet Deassertion AC Timing

24.9 RGMII/RTBI Mode Timing

For RGMII mode, the following specifications are valid when the I/O power supply (VDDIO) is 2.5V or 3.3V, ±5%, per the RGMII specification, and the MAC I/F selection bits have been set to RGMII mode. See MII Register 23 and the RGMII specification for more information. All timing specifications are referenced to a switching threshold of 1.25V or 1.65V (i.e., 50% of VDDIO).

Table 24-1. RGMII/RTBI Mode AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{skew}T$	-500	0	500	ps	Data to clock output skew (at PHY) – uncompensated mode.
$T_{skew}R$	1.0	1.8	2.6	ns	Data to clock output skew (at receiver) – uncompensated mode.[1]
$T_{setup}T$		2.0[2]		ns	Data to clock output Setup (at PHY integrated delay)[3]
$T_{hold}T$		2.0[2]		ns	Data to clock output Setup (at transmitter integrated delay)[3]
$T_{setup}R$		2.0[2]		ns	Data to clock output Setup (at receiver integrated delay)[3]
$T_{hold}R$		2.0[2]		ns	Data to clock output Setup (at PHY integrated delay)[3]
T_{CYC}	7.2	8.0	8.8	ns	Clock cycle duration.[4]
Duty_G	45	50	55	%	Duty cycle for 1000BASE-T.[5]
Duty_T	40	50	60	%	Duty cycle for 10BASE-T and 100BASE-TX.[5]
T_R, T_F			0.75	ns	Rise, fall time (20% to 80%).

[1] This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. This is normal operating mode (RGMII timing is *not* compensated). To enable RGMII timing compensation, see MII Register bit 23.8.

[2] This delay is 2.5ns for the GTX_CLK when VDDIO = 3.3V. This requires all TXD and TX_CTL traces to have a 500ps delay added by using a trombone-structure when operating in compensated (RGMII-ID) mode with VDDIO = 3.3V.

[3] RGMII-ID mode - a 2ns delay is added to the TXC and RXC signals inside the PHY.

[4] For 10Mbps and 100Mbps, T_{CYC} will scale to 400ns (±40ns), and 40ns (±4ns), respectively.

[5] Duty cycle may be stretched or shrunk during speed changes or while transitioning to a received packet's clock domain, as long as the minimum duty cycle is not violated, and stretching occurs for no more than three T_{CYC} of the lowest speed transitioned between.

Figure 24-1 diagrams RGMII timing and multiplexing in uncompensated mode.

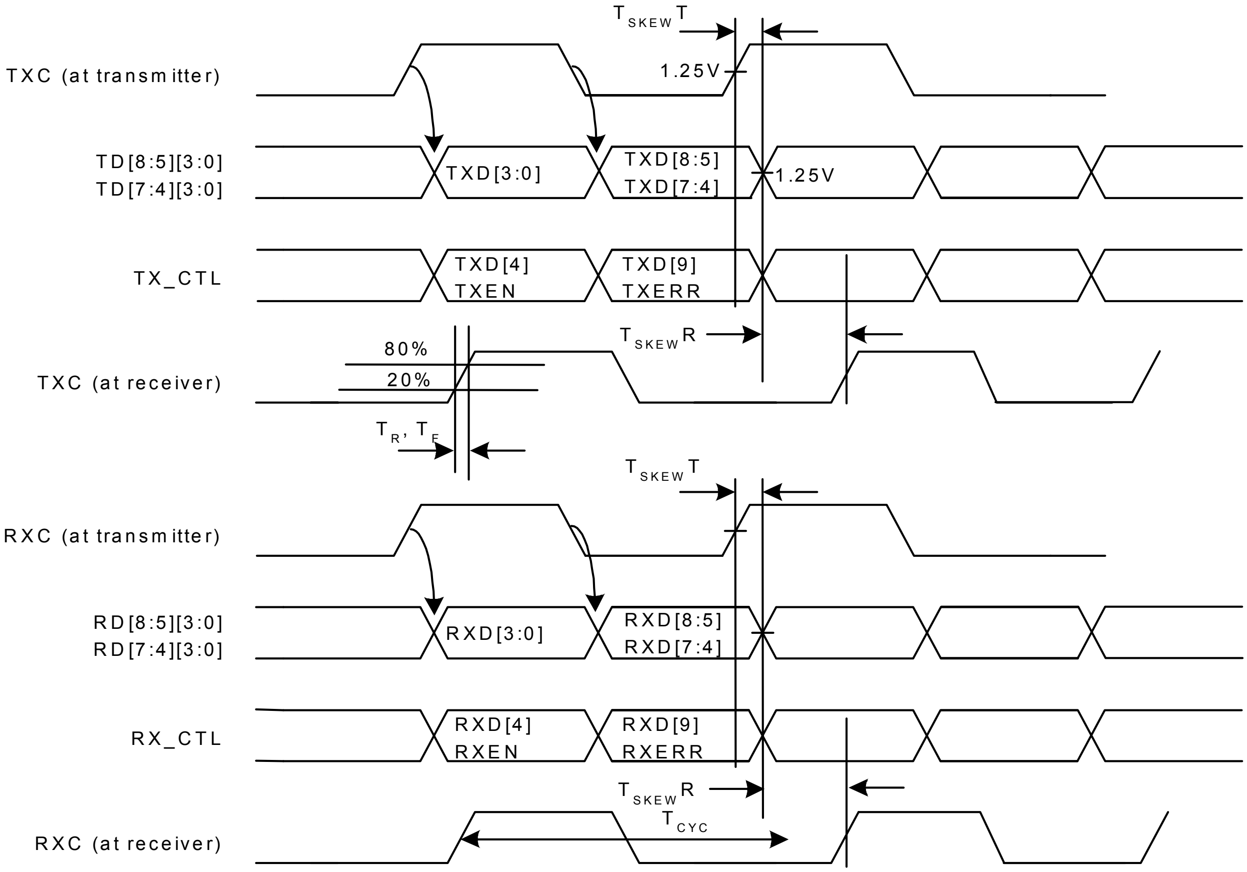


Figure 24-1. RGMII/RTBI Uncompensated AC Timing and Multiplexing

The RGMII specification (v1.3) defines the following relationship between the clock and data signals at the MAC/PHY interface:

To meet this timing specification, a 1.5ns delay to the TXC and RXC signals is typically added on the PC board using a long "trombone shaped" trace.

While the CIS8204's default RGMII operation mode conforms to the RGMII v1.3 specification, the device also includes an optional mode of operation where the addition of this delay is handled internally to the CIS8204. This operation mode can be enabled by setting MII Register bit 23.8 high. In this operation mode, the CIS8204 expects the following relationship between TXC and TD on the transmit side:

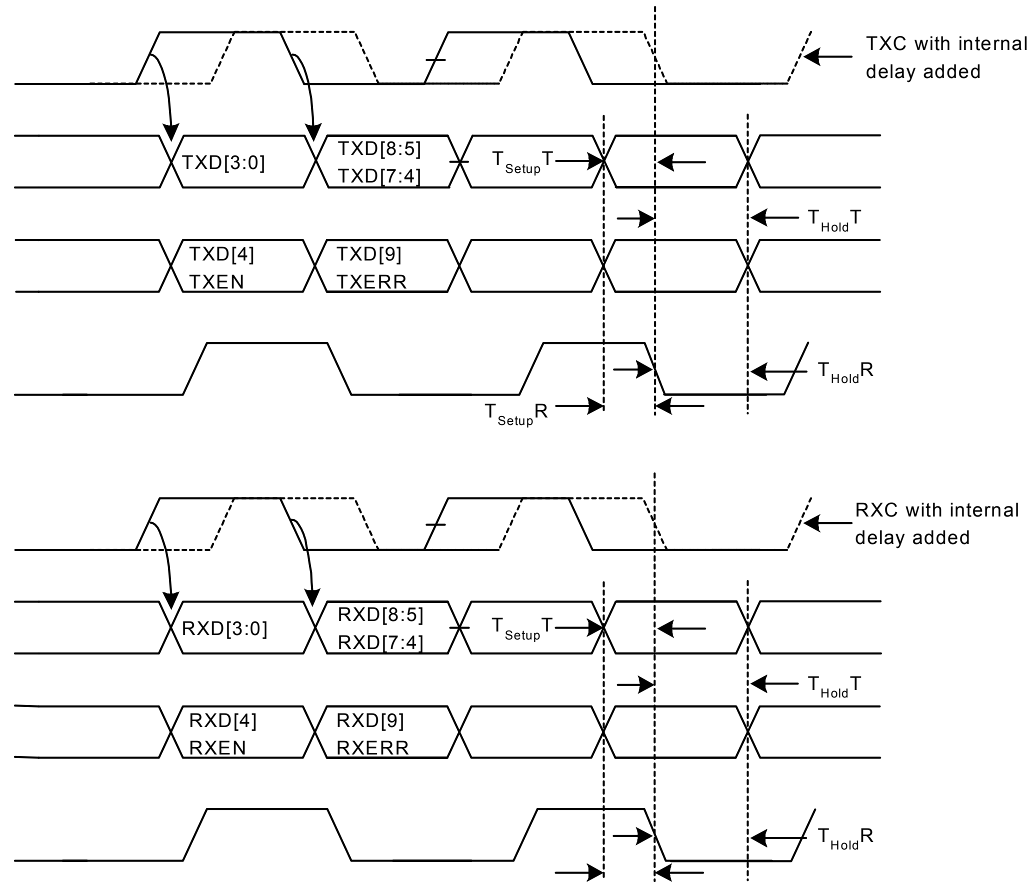


Figure 24-2. RGMII/RTBI Compensated AC Timing and Multiplexing

TXC is internally delayed by ~2ns when VDDIO = 2.5V.

TXC is internally delayed by ~2.5ns when VDDIO = 3.3V.

On the receive side, RXC is delayed internally by ~2ns for VDDIO = 2.5V or VDDIO = 3.3V.

Since no “trombone shaped” trace is required with this approach, the advantages of this compensated timing over RGMII v1.3 include:

- Simplified board design
- More compact routes; less board area
- Lower EMI emissions
- Greater distance possible between the MAC and PHY
- Improved signal integrity for a given distance between the MAC and PHY.

24.10 TBI Mode Transmit Timing

For TBI mode, the following specifications are valid only when the I/O power supply (VDDIO) is 3.3V, ±5%, and the MAC I/F selection bits have been set to TBI mode. See MII Register 23 for more information.

Table 24-1. TBI Mode Transmit AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{PMA\_TX\_CLK}$	8.0 - 100ppm	8.0	8.0 + 100ppm	ns	PMA transmit clock period
T_{SETUP}	2			ns	Transmit data setup time to rising edge of PMA_TX_CLK_n.
T_{HOLD}	1			ns	Transmit data hold time to rising edge of PMA_TX_CLK_n.
T_{DUTY}	40		60	%	PMA_TX_CLK_n duty cycle.
t_R	0.7		2.4	ns	Clock rise time (0.8V to 2.0V).
t_F	0.7		2.4	ns	Clock fall time (2.0V to 0.8V).
t_R	0.7			ns	Data rise time (0.8V to 2.0V).
t_F	0.7			ns	Data fall time (2.0V to 0.8V).

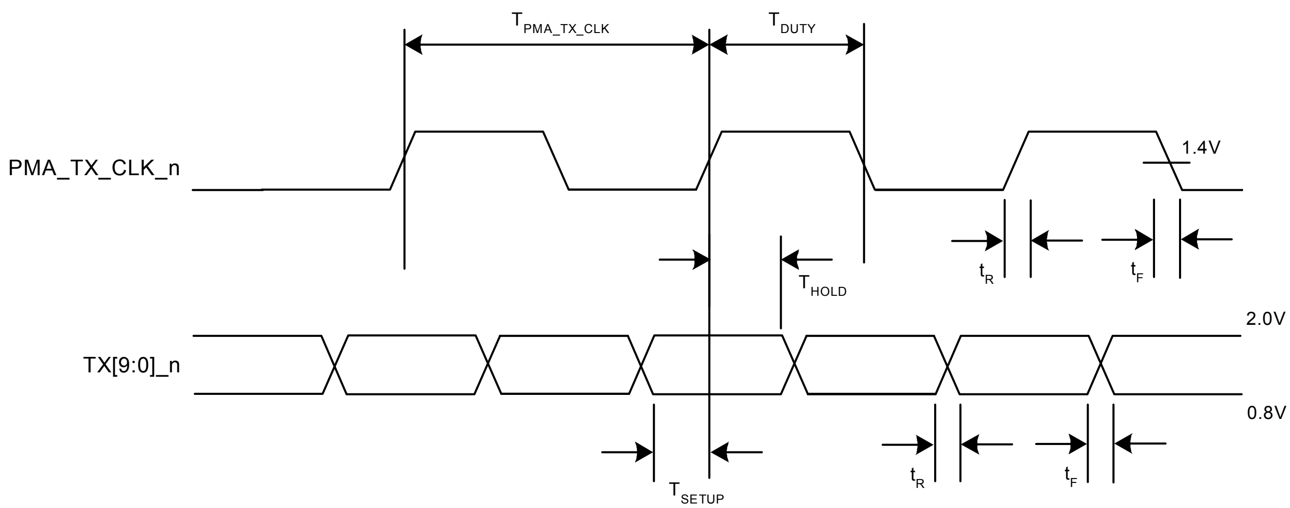


Figure 24-3. TBI Transmit AC Timing

24.11 TBI Mode Receive Timing

For TBI mode, the following specifications are valid only when the I/O power supply (VDDIO) is 3.3V, ±5%, and the MAC I/F selection bits have been set to TBI mode. See MII Register 23 for more information.

Table 24-2. TBI Mode Receive AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{PMA\_RX\_CLK}$		62.5		MHz	PMA receive clock frequency (PMA_RX_CLK1_n and PMA_RX_CLK0_n).
T_{DRIFT}	0.2			µs/MHz	PMA_RX_CLK drift rate.[1]
T_{A-B}	7.5		8.5	ns	PMA_RX_CLK skew.
T_{SETUP}	2.5			ns	Receive data setup time to rising edge of PMA_RX_CLK.
T_{HOLD}	1.5			ns	Receive data hold time to rising edge of PMA_RX_CLK.
T_{DUTY}	40		60	%	PMA_RX_CLK duty cycle.
t_R	0.7		2.4	ns	Clock rise time (0.8V to 2.0V).
t_F	0.7		2.4	ns	Clock fall time (2.0V to 0.8V).
t_R	0.7			ns	Data rise time (0.8V to 2.0V).
t_F	0.7			ns	Data fall time (2.0V to 0.8V).

[1] The drift rate is the (minimum) time for PMA_RX_CLK to drift from 63.5MHz to 64.5MHz or 60MHz to 59MHz from the PMA_RX_CLK lock value. It is applicable under all input signal conditions (except during code-group alignment), provided that the receiver clock recovery unit was previously locked to PMA_TX_CLK or to a valid input signal.

The following figure diagrams TBI receive AC timing.

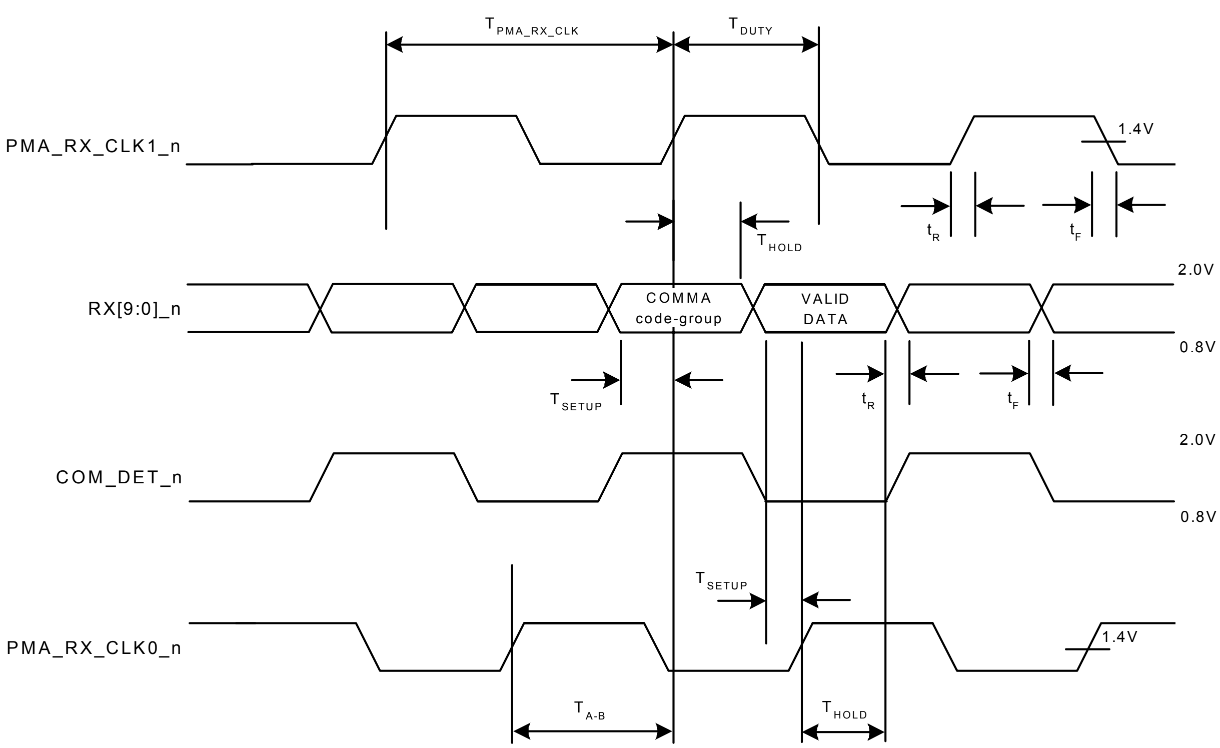


Figure 24-4. TBI Receive AC Timing

24.12 Auto-Negotiation Fast Link Pulse (FLP) Timing

The following specifications represent both transmit and receive timings. They are valid only when the I/O power supply (VDDIO) is at either 3.3V, ±5%, or 2.5V, ±5%. See MII Register 23 for more information.

Table 24-3. Auto-Negotiation FLP AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{CLK\text{-}Period}$	111	125	139	µs	Clock pulse to clock pulse period.
$T_{CLK/DATA}$		100		ns	Clock/Data pulse width.
$T_{CLK/DATA\text{-}Period}$	55.5	62.5	69.5	µs	Clock pulse to data pulse period (Data = 1).
$T_{BURST\text{-}Period}$	8		24	ms	FLP burst to FLP burst period.
T_{BURST}		2		ms	FLP burst width.
n_{BURST}	17		33	#	Number of pulses in an FLP burst.

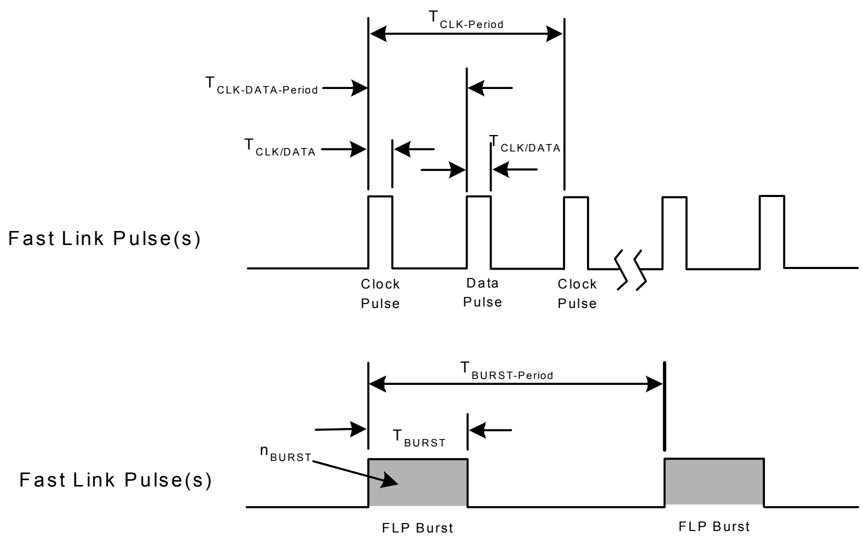


Figure 24-5. Auto-Negotiation FLP AC Timing

24.13 JTAG Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.3V, ±5%, or 2.5V, ±5%. See MII Register 23 for more information.

Table 24-4. JTAG Interface AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TCK\text{-}Period}$	100			ns	TCK period.
$T_{TCK\text{-}High}$	45			ns	TCK minimum pulse width high.
$T_{TCK\text{-}Low}$	45			ns	TCK minimum pulse width low.
$T_{TDI/TMS\text{-}Setup}$	10			ns	(TMS or TDI) to TCK setup time.
$T_{TDI/TMS\text{-}Hold}$	10			ns	(TMS or TDI) to TCK hold time.
$T_{TDO\text{-}Delay}$	0		15	ns	TDO delay from TCK.

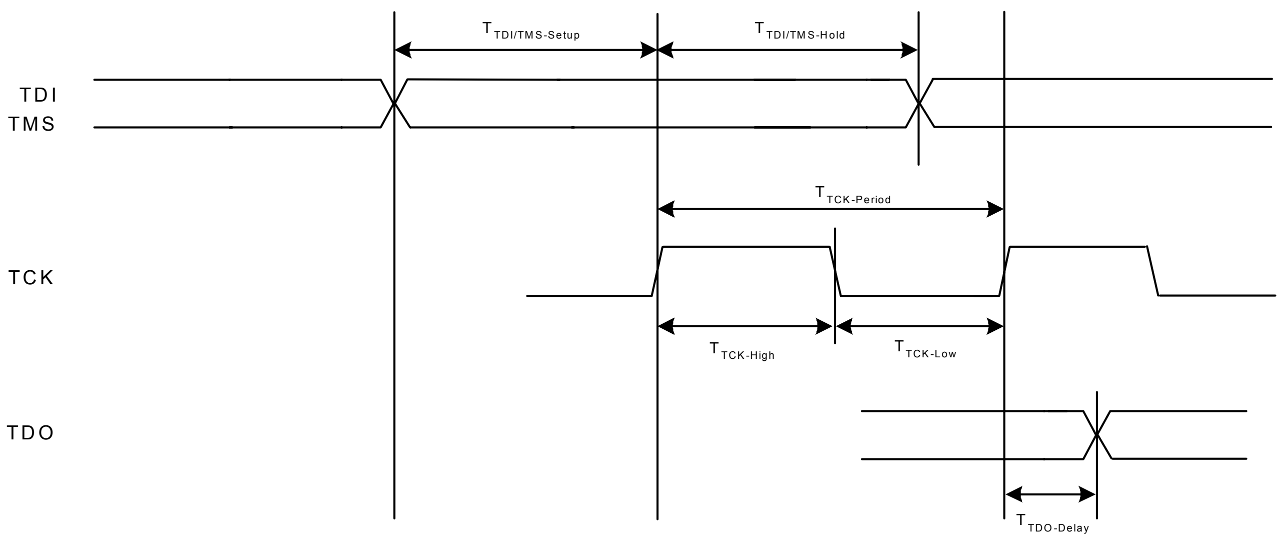


Figure 24-6. JTAG Interface AC Timing

24.14 SMI Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.3V, ±5%, or 2.5V, ±5%. See MII Register 23 for more information.

Table 24-5. SMI AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{MDC}	0	2.5	25	MHz	MDC clock frequency.
$T_{MDC\text{-}High}$	20	50		ns	MDC clock pulse width high.
$T_{MDC\text{-}Low}$	20	50		ns	MDC clock pulse width low.
$T_{MDIO\text{-}Setup}$	10			ns	MDIO to MDC setup time when sourced by Station Manager.
$T_{MDIO\text{-}Hold}$	10			ns	MDIO to MDC hold time when sourced by Station Manager.
$T_{MDIO\text{-}Delay}$		10	300	ns	MDC to MDIO delay time from CIS8204. Delay will depend on value of external pull-up resistor on MDIO pin.

Note: At 16MHz, a 400Ω pull-up resistor on the MDIO pin is recommended; otherwise, a 2kΩ pull-up resistor is recommended at 2MHz.

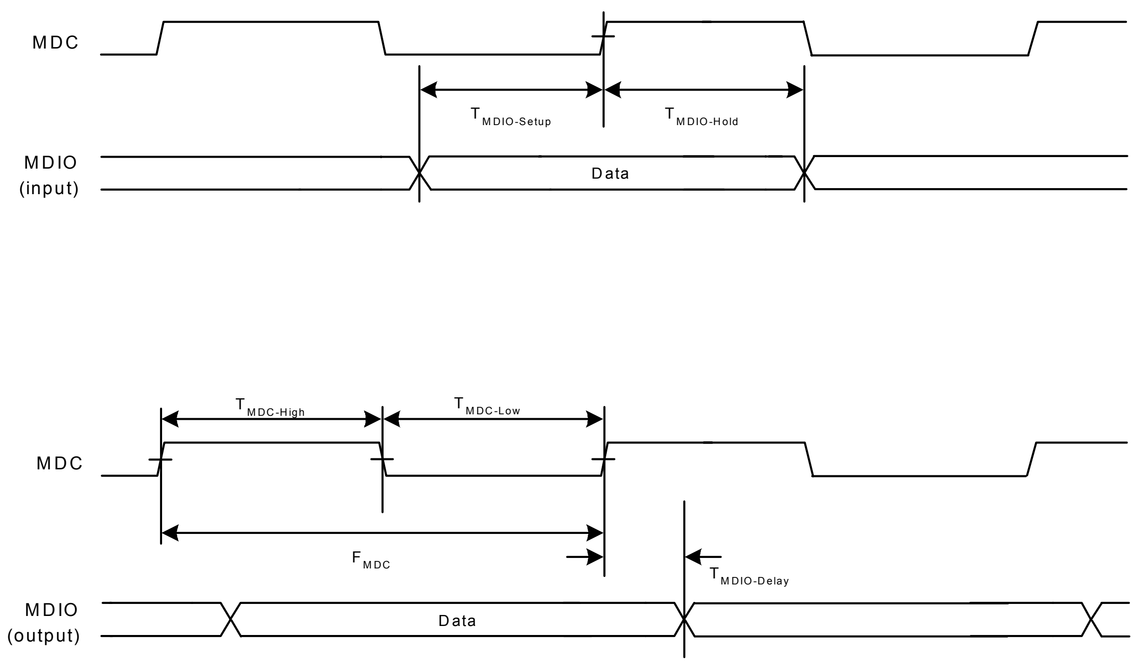


Figure 24-7. SMI AC Timing

24.15 MDINT# Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.3V, ±5%, or 2.5V, ±5%. See MII Register 23 for more information.

Table 24-6. MDINT# AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
t_F			110	ns	MDINT# fall time, assuming a 2.2kΩ external pull-up resistor and a 50pF total capacitive load.

24.16 Power-Down and Reset Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.3V, ±5%, or 2.5V, ±5%. See MII Register 23 for more information.

Table 24-7. Power-Down and Reset AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{RESET\#1}$	2			µs	RESET# assertion time after device power supplies are stable.
$T_{RESET\#2}$	1			µs	RESET# assertion time while device is powered up.
T_{PLL_LOCK}			10	µs	PLL lock time.

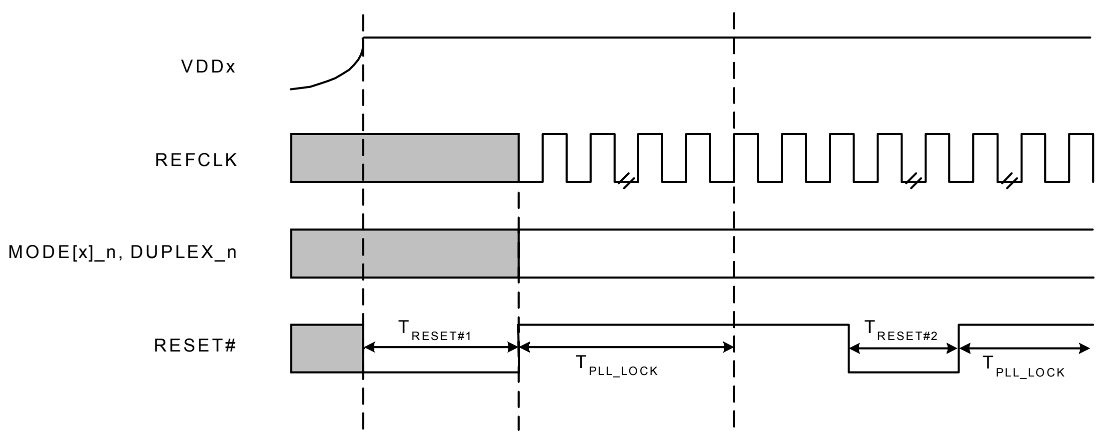


Figure 24-8. Power-Down and Reset AC Timing

24.17 LED_CLK and LED_DATA Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.3V, ±5%, or 2.5V, ±5%. See MII Register 23 for more information.

Table 24-8. LED_CLK and LED_DATA Output AC Timing Specification

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{LED_CLK}	1			µs	LED_CLK output period.
$T_{LED\_CLK\text{-}Pause}$	10			ms	LED_CLK pause between LED bit sequence repeat (un-preambled mode).
$T_{LED\_DATA\text{-}Delay}$			15	ns	LED_DATA propagation delay from rising edge of LED_CLK.

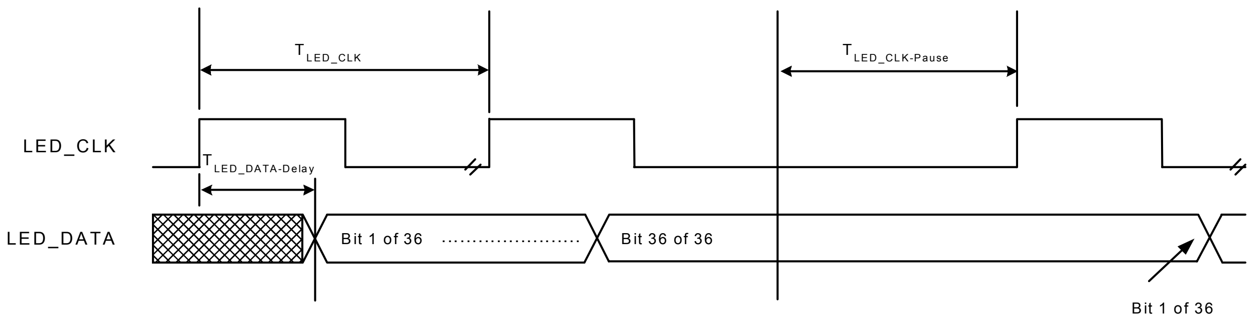


Figure 24-9. LED_CLK and LED_DATA Output AC Timing
(Un-preambled mode with all 36 LED status bits enabled)

24.18 REFCLK Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.3V, ±5%, or 2.5V, ±5%. See MII Register 23 for more information.

Table 24-9. REFCLK AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{REFCLK25}$		40		ns	Reference clock period, PLLMODE = 0 (25MHz reference).
$T_{REFCLK125}$		8		ns	Reference clock period, PLLMODE = 1 (125MHz reference).
$F_{STABILITY}$	-50		+50	ppm	Reference clock frequency stability (0°C to 70°C).
T_{DUTY}	40		60	%	REFCLK duty cycle in both 25MHz and 125MHz modes.
$J_{REFCLK25}$, $J_{REFCLK125}$			300	ps	Total jitter of 25MHz or 125MHz reference clock (peak-to-peak).
$t_{R/F\ (REFCLK25)}$			4	ns	Reference clock rise time, 25MHz mode (20% to 80%).
$t_{R/F\ (REFCLK125)}$			1	ns	Reference clock rise time, 125MHz mode (20% to 80%).

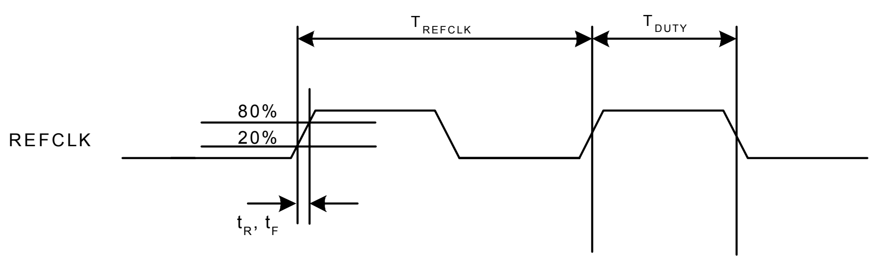


Figure 24-10. REFCLK AC Timing

24.19 CLK125 Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.3V, ±5%, or 2.5V, ±5%. See MII Register 23 for more information.

Table 24-10. CLK125 AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{CLK125}		8		ns	Reference clock period.
$F_{STABILITY}$	-50		+50	ppm	Reference clock frequency stability (0°C to 70°C).
T_{DUTY}	40		60	%	Reference clock duty cycle.
J_{CLK125}			300	ps	Total jitter of reference clock (peak-to-peak).
$t_{R/F\ (CLK125)}$			1	ns	Reference clock rise time (20% to 80%).

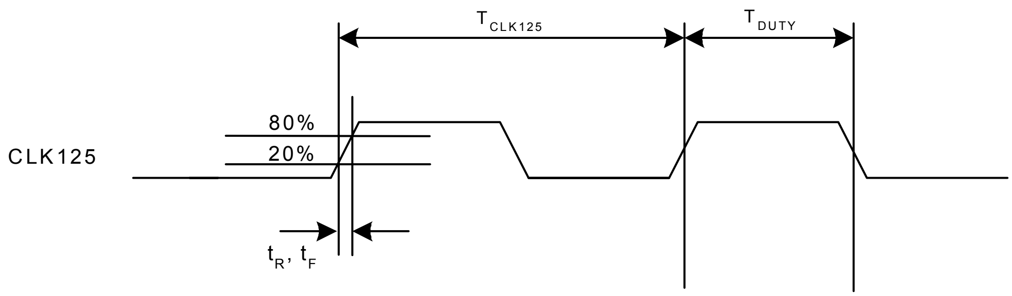


Figure 24-11. CLK125 AC Timing

24.20 Isolation Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.3V, ±5%, or 2.5V, ±5%. See MII Register 23 for more information.

Table 24-11. Isolation AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{ISOL\text{-}Reg}$			100	µs	Time from the software clear of Register bit 0.10 to the transition from Isolate to Normal mode.
$T_{ISOL\text{-}Reset}$			500	µs	Time from the deassertion of a hardware or software reset to the transition from Isolate to Normal mode.

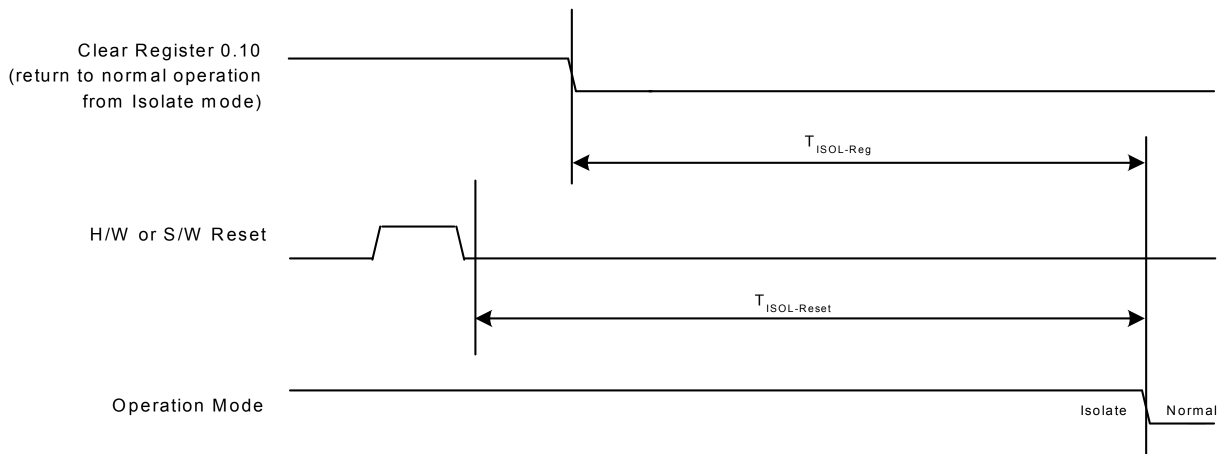


Figure 24-12. Isolation AC Timing

25 Magnetics Specifications

Two of the recommended transformer modules[1] for the CIS8204's twisted pair interface are:

- Pulse Model #H5007
- Pulse Model #H5008

Table 25-1. Magnetics Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
N		1:1		N/A	Transformer turns ratio.
-			1.0	dB	Insertion loss (60MHz to 100MHz).
-	-16			dB	Return loss, @ 85, 100, 115Ω (1MHz to 40MHz).
-	$10 - 20\log_{10}$ (f/80MHz)			dB	Return loss, @ 85, 110, 115Ω (40MHz to 100MHz).
-			1.5	kV	Isolation.
L_{PRI}	350			µH	Primary inductance.
-	40			dB	Differential to common mode rejection (0.1MHz to 60MHz).

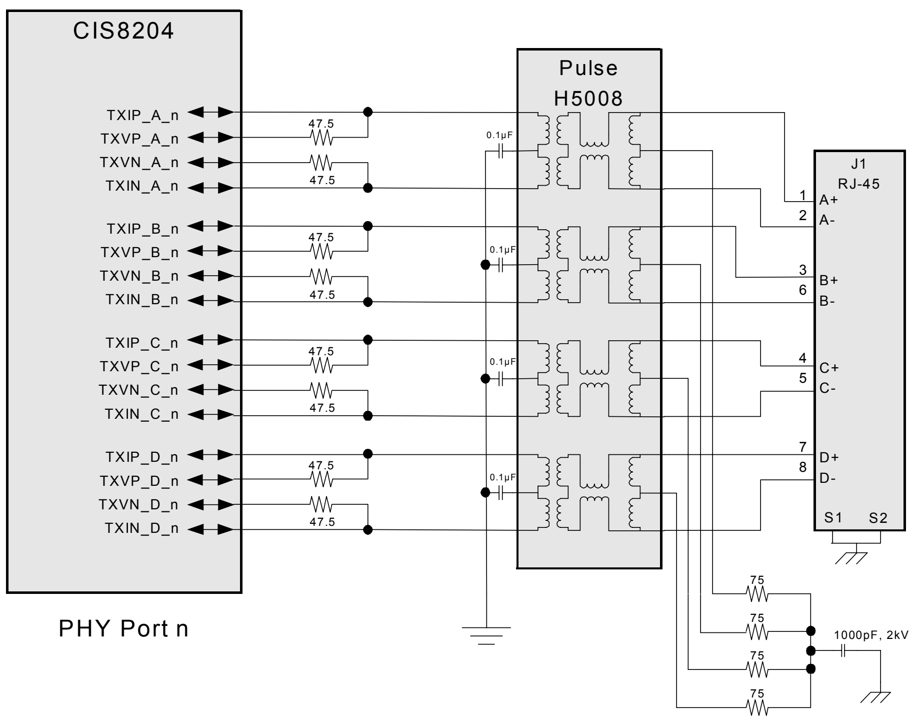


Figure 25-1. PHY-Transformer Connections

[1]Please contact Cicada regarding the use of alternate transformer modules.

26 Packaging Specifications

26.1 35mm HS-BGA Mechanical Specification

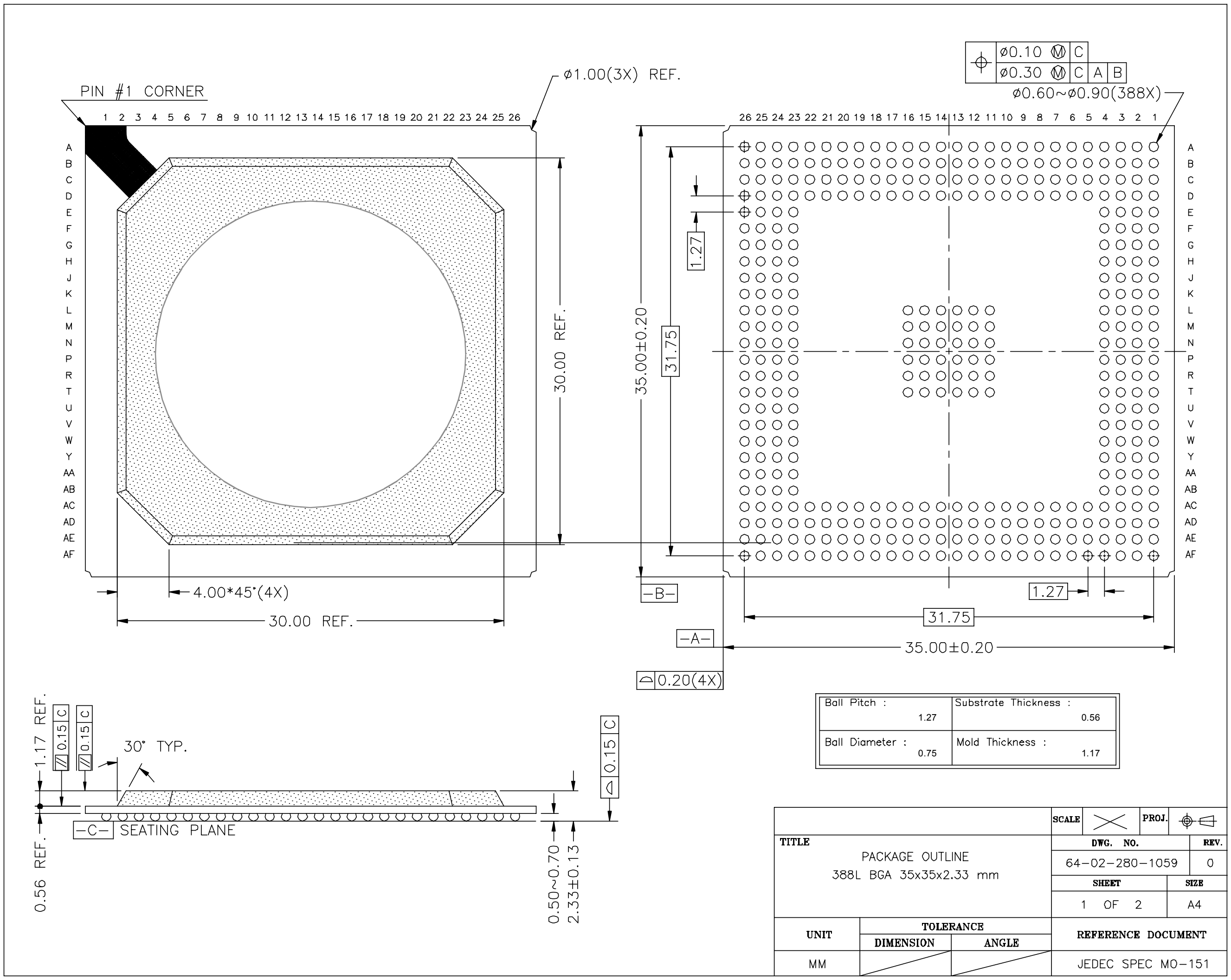


Figure 26-1. 35mm HS-BGA Mechanical Specification

Marking Codes: P: Temperature Range, YY: Date Code Year, WW: Date Code Week, wabbbb: lot code

Figure 26-2. 35mm HS_BGA Chip Markings

26.2 27mm HS-BGA Mechanical Specification

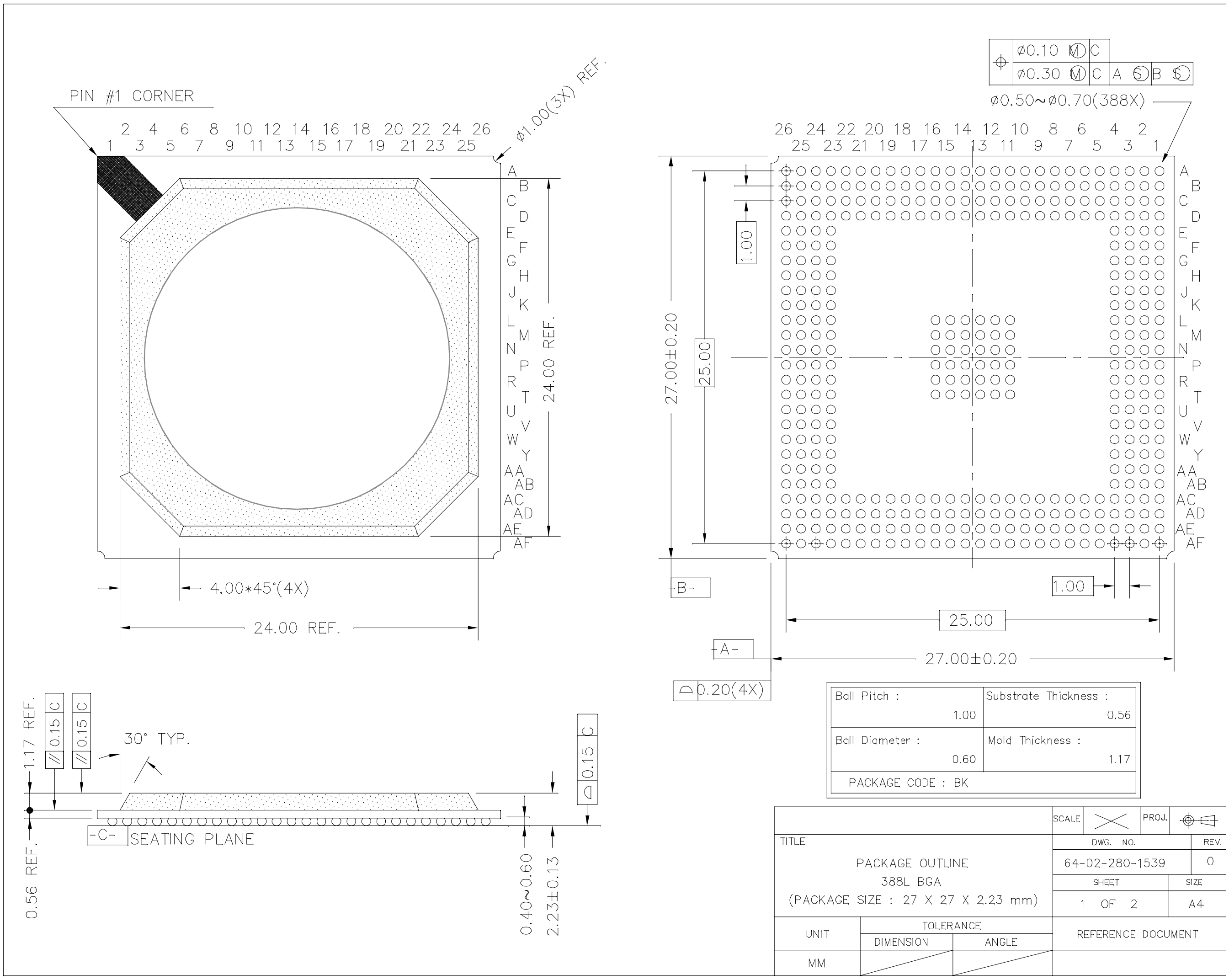
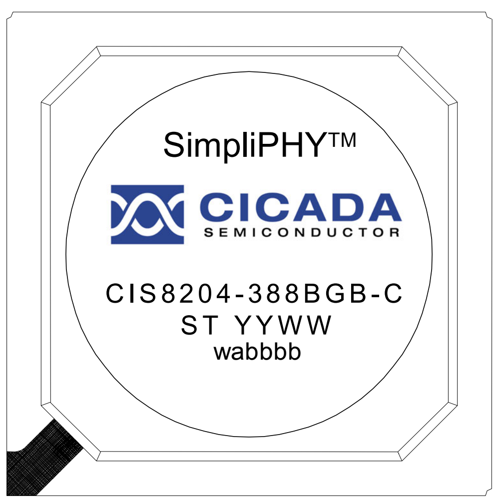


Figure 26-3. 27mm HS-BGA Mechanical Specification



Marking Codes: P: Temperature Range, YY: Date Code Year, WW: Date Code Week, wabbbb: lot code

Figure 26-4. 27mm HS_BGA Chip Markings

27 Ordering Information

27.1 Devices

Table 27-1. Device Ordering Information

Part Number	Container[1]	Package Type	Description	Temperature Range
CIS8204-388BGA-C	Tray	388 Ball HS-BGA 35mm x 35mm	SimpliPHY™ Quad 10/100/1000BASE-T PHY with: GMII / MII, RGMII, TBI, RTBI interfaces.	Commercial: 0°C to +70°C
CIS8204-388BGA-CR	Tape & Reel	388 Ball HS-BGA 35mm x 35mm	SimpliPHY™ Quad 10/100/1000BASE-T PHY with: GMII / MII, RGMII, TBI, RTBI interfaces.	Commercial: 0°C to +70°C
CIS8204-388BGB-C	Tray	388 Ball HS-BGA 27mm x 27mm	SimpliPHY™ Quad 10/100/1000BASE-T PHY with: GMII / MII, RGMII, TBI, RTBI interfaces.	Commercial: 0°C to +70°C
CIS8204-388BGB-CR	Tape & Reel	388 Ball HS-BGA 27mm x 27mm	SimpliPHY™ Quad 10/100/1000BASE-T PHY with: GMII / MII, RGMII, TBI, RTBI interfaces.	Commercial: 0°C to +70°C

[1] One of the container options must be specified when ordering. All orders for tape and reel must be for an entire reel.

27.2 Evaluation Systems

Table 27-2. Evaluation System Ordering Information

Part Number	System Type	Description
CEB8204-388BGA-G	Evaluation Board	Quad Port Customer Evaluation Board for CIS8204 – for GMII / MII / RGMII interface evaluation with 35mm HS-BGA device.
CRD8204-388BGA-T	Reference Design	8 Port Gigabit Ethernet Switch Reference Design using the CIS8204 – with 35mm HS-BGA device.
CRD8204-388BGB-G	Reference Design	8 Port Gigabit Ethernet Switch Reference Design using the CIS8204 – with 27mm HS-BGA device.

28 Applications Support

28.1 Available Documents and Application Notes

Product Brief - **CRD8204 8 Port Gigabit Ethernet Switch Reference Design**
Design Package - **CRD8204 8 Port Gigabit Ethernet Switch Reference Design**

Package Includes: Bill of Materials, PCB Gerber files, PADS PCB layout database, OrCAD Schematics, User guide, CIS8204 Data Sheet and Application Notes.

AN004 - **SimpliPHY™ CIS8204 PCB Design and Layout Application Note**
User Guides - **Evaluation Kit CEB8204**

CRD8204 8 Port Gigabit Ethernet Switch Reference Design

28.2 Contact Information

Device data sheets, user guides, and application notes should be requested through email via info@cicada-semi.com

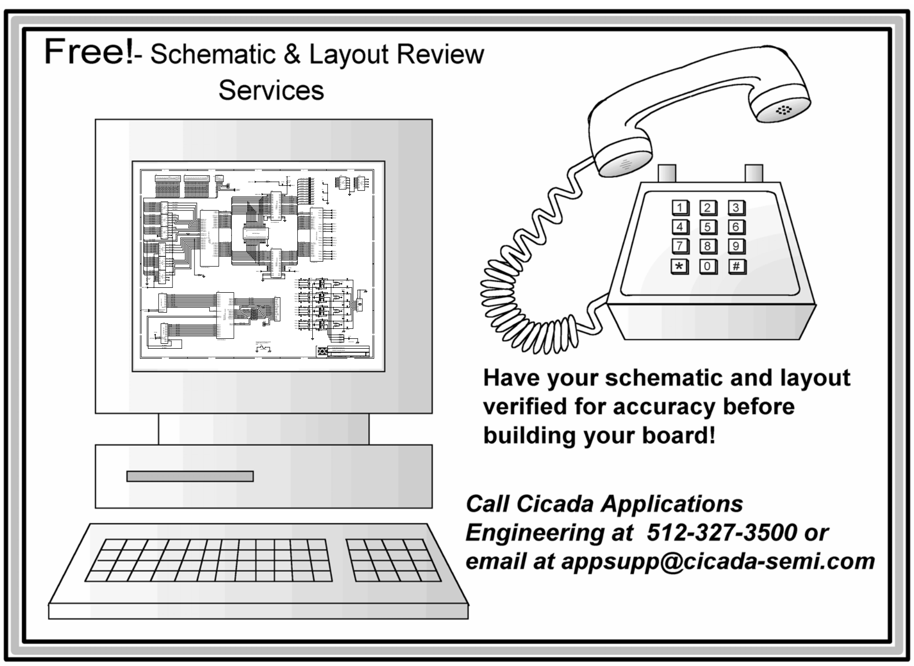
For Application questions and support send email to appsupp@cicada-semi.com or call 512-327-3500.

28.3 Application Support Services

These services are provided free of charge to Cicada Semiconductor customers. Customers are strongly urged to make use of these services as many potential issues and problems can be caught early in the design cycle, thus minimizing costly redesigns.

Schematic Review - Cicada Application Engineers will review your schematics for technical accuracy. Schematics can be submitted via the appsupp@cicada-semi.com email address in either Orcad or .pdf formats.

PCB Layout Review - Cicada Application Engineers will review your PCB layout for technical accuracy. PCB layout plots can be submitted via the appsupp@cicada-semi.com email address in either standard gerber file or .pdf formats.



29 Document History & Notices

Table 29-1. Document History & Notices

Revision Number	Date	Comments
1.0.0	11 Jul 02	Complete and approved documentation for Silicon Revision B4.
1.1.0	Jan 03	Complete and approved documentation for Silicon Revision B5.