SOLID STATE SCIENTIFIC

SCM23C65 883/23C65

8192 x 8 Static CMOS ROM

Features

- Fast Access Time Selection: 150ns/200ns/300ns
- Low Operating Current: 10mA Max.
- Low Standby Current: 50μA Max.
- Commercial, Industrial and Military Temperature Ranges
- 883 Qualified Version: 883/23C65M
- 28 Pin JEDEC Approved Pinout: Compatible with 2564 and 2764 EPROMs and 2365 and 37000 NMOS ROMs
- Two Mask-programmable Chip Selects (CS1/$\overline{CS1}$, CS2/$\overline{CS2}$)
- Mask-programmable Output Enable (OE/$\overline{OE}$)
- Mask-programmable Chip Enable (CE/$\overline{CE}$) with Power Down Feature
- Single 5V ± 10% Supply
- Completely Static Operation
- Three-State Outputs for Direct Bus Interface
- Completely TTL Compatible

Description

The Solid State Scientific SCM23C65 is a high performance 65,536 bit static Read Only Memory (ROM) organized 8,192 words by eight bits and is fabricated using the SSS scaled silicon gate CMOS process, HCMOS II. With HCMOS II, all the operating features of NMOS ROMs are achieved (high speed, density, TTL compatibility), but with the added benefit of low CMOS operating power (approx. 1/10 the equivalent NMOS power).

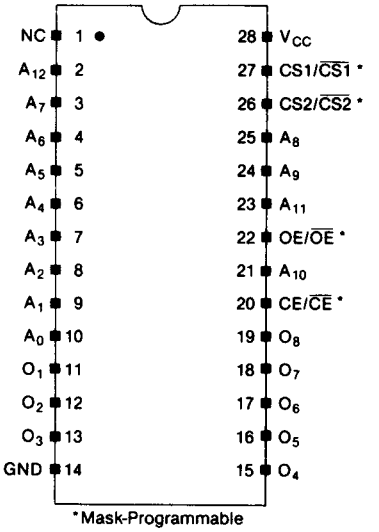
The SCM23C65 operates from a single 5 Volt supply and features fully static operation requiring no clock. Four mask programmable "chip selects" are provided (OE, CE, CS1, CS2) for system expansion and output bus control. The Output Enable input (OE/$\overline{OE}$) provides direct control of the three-state outputs for bus control and fast access to data. The Chip Enable input (CE/$\overline{CE}$) also controls the three-state outputs and, in addition, provides a "power down" feature to reduce chip current to less than 50μA. Since the access time to enable the ROM is the same as the address access time, no performance need be sacrificed to achieve reduced system power. The additional Chip Selects (CS1/$\overline{CS1}$, CS2/$\overline{CS2}$) may be programmed to allow up to four 64K ROMs to be OR-tyed without external decoding while still retaining the desirable functions of the Output Enable and Chip Enable inputs.

Designed to replace equivalent EPROMs and NMOS ROMs, the Solid State Scientific SCM23C65 is one of a family of state-of-the-art CMOS ROMs with densities of 32K, 64K, 128K and 256K bits with industry standard 24 and 28 lead pinouts.

Operating Characteristics Summary

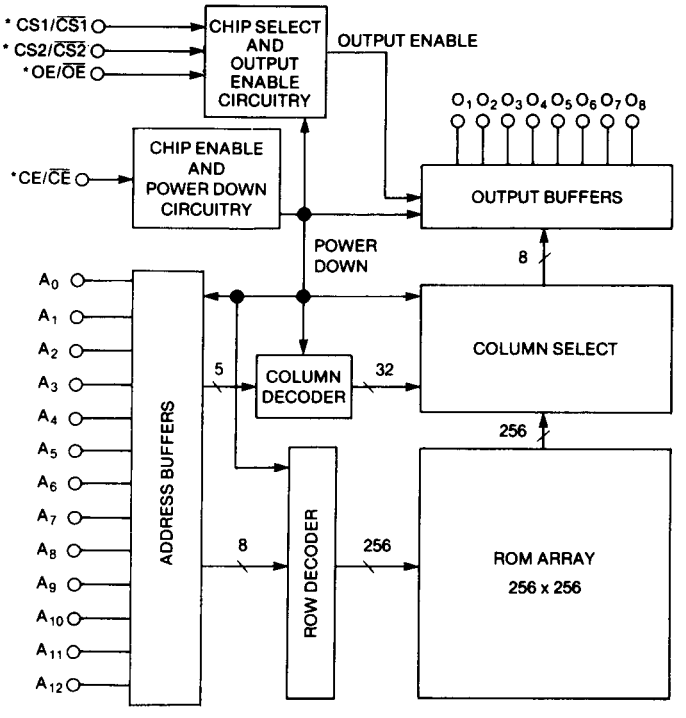
Type	Operating Temperature Range	Address/ Chip Enable Access Time	Output Enable Access Time
SCM23C65-3	0° to +70°C	150ns	85ns
SCM23C65-4	0° to +70°C	200ns	100ns
SCM23C65	−40° to +85°C	300ns	120ns
SCM23C65M	−55° to +125°C	300ns	120ns
883/23C65M	−55° to +125°C	300ns	120ns

Pin Configuration



*Mask-Programmable

Block Diagram



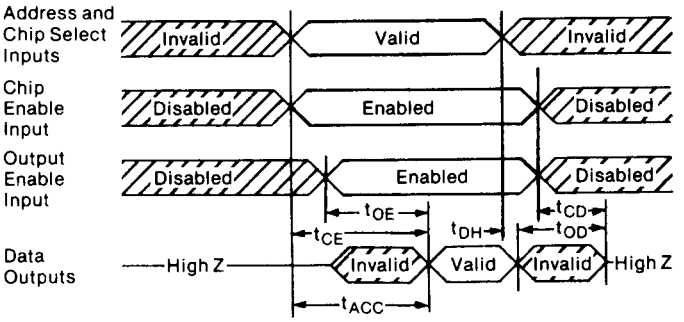
Absolute Maximum Limits

Storage Temperature	T_S	−65° to +150°C
DC Supply Voltage	V_{CC}	−0.5 to +7.0V
Input Voltage	V_{IN}	$-0.3 \le V_{IN} \le V_{CC} + 0.3$
Power Dissipation Per Package	P_T	500mW

Recommended Operating Conditions

Parameter		Limits
DC Supply Voltage	V_{CC}	5V ± 10%
Operating Temperature	(T_A)	
23C65:		−40° to +85°C
23C65M:		−55° to +125°C
23C65-4/-3:		0° to +70°C

Timing Diagram



D.C. Characteristics (V_{CC} = 5V ± 10%)

Symbol	Parameter	Min.	Typ.(1)	Max.	Units	Conditions
V_{IH}	Input High Voltage	2.2			V	23C65, 23C65M
V_{IH}	Input High Voltage	2.0			V	23C65-3/-4
V_{IL}	Input Low Voltage			0.8	V	
I_{LI}	Input Leakage Current			1.0	μA	$0V \le V_{IN} \le 5.5V$
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −1.0mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2mA(4)
I_{LO}	Output Leakage Current			1.0	μA	Outputs Disabled
I_{CC}	Operating Current		5	10	mA	
I_{CCL1}	Standby Current		0.5	1	mA	Chip Disabled(2)
I_{CCL2}	Standby Current, 23C65/-3/-4		10	50	μA	Chip Disabled(2)
I_{CCL2}	Standby Current, 23C65M		10	100	μA	Chip Disabled(2)

A.C. Characteristics (V_{CC} = 5V ± 10%)

Symbol	Parameter	23C65 (−40°to+85°C) Min.	23C65 Max.	23C65M (−55° to +125°C) Min.	23C65M Max.	23C65-4 (0° to +70°C) Min.	23C65-4 Max.	23C65-3 (0° to +70°C) Min.	23C65-3 Max.	Units	Conditions
t_{ACC}	Address/Chip Select Access Time		300		300		200		150	ns	Note 3
t_{DH}	Previous Data Valid After Address Change	10		10		10		10		ns	Note 3
t_{CE}	Chip Enable Access Time		300		300		200		150	ns	Note 3
t_{CD}	Chip Disable to Output Float		30		30		30		30	ns	Note 3
t_{OE}	Output Enable Access Time		120		120		100		85	ns	Note 3
t_{OD}	Output Disable to Output Float		30		30		30		30	ns	Note 3

1. T_A = 25°C; V_{CC} = 5.0V
2. Two limits of standby current are applicable, the choice of which depends on the voltage level applied to the Chip Enable input ($\overline{CE}$ or CE, as programmed):

Applicable Standby Current	$\overline{CE}$ (V_{IH}min.)	OR	CE (V_{IL}max.)
I_{CCL1}	2.0V		0.8V
I_{CCL2}	V_{CC} − 0.4V		0.4V

3. A.C. TEST CONDITIONS
   Input Pulse Levels: 0.8 to 2.4V
   Input Rise/Fall Times: ≤10ns
   Time Measurement Reference Level: 1.5V
   Output Load: 1 TTL Load and C_L = 100 pF
4. The SCM23C65R version is available for RFI and noise sensitive applications. It meets all specifications for the 23C65 except I_{OL}; which is specified at 1.6mA.