



Intel® IXF1010 10-Port 100/1000 Mbps Ethernet Media Access Controller

Preliminary Datasheet

The Intel® IXF1010 is a 10-port Ethernet Media Access Controller (MAC) that supports IEEE 802.3 100 and 1000 Mbps applications. The device supports a System Packet Interface Level 4 Phase 2 (SPI4-2) system interface to the network processor or ASIC, and implements the Reduced Gigabit Media Independent Interface (RGMII), as defined in Version 1.2a of the Hewlett-Packard specification for PHY connectivity. The RGMII reduces the interface pin count from GMII to allow for higher port densities.

Applications

In general, the IXF1010 is appropriate for high-end switching applications where MAC and PHY functions are not integrated into the system ASIC.

- High-End Ethernet Switches
- Multi-Service Ethernet Switches
- High-End Ethernet LAN/WAN Routers

Product Features

- Supports 10 independent 100/1000 Mbps full-duplex Ethernet MAC ports
- System Packet Interface Level 4 Phase 2 (SPI4-2)
 - Capable of data transfers from 10.24 Gbps up to 12.8 Gbps
 - Supports dynamic phase alignment
 - Integrated termination
- RGMII interface with MDIO for Ethernet physical connectivity
- 32-bit CPU interface
- RMON statistics
- JTAG boundary scan capable
- Compliance with IEEE 802.3 MII Management Interface (MDIO)
- Compliance with IEEE 802.3x Standard for flow control
- Jumbo frame support for 9.6 KB packets
- .18 μ CMOS process technology
- Internal 17.0 KB receive FIFO and 4.5 KB transmit FIFO per channel
- Independent enable/disable of any port
- Detection of short or overly large packets
- Error counters for dropped and errored packets
- CRC calculation and error detection
- Programmable option to:
 - Filter packets with errors
 - Filter, broadcast, multicast, and unicast address packets
 - Automatically pad transmitted packets less than the minimum frame size
- 552-Ceramic Ball Grid Array (CBGA)
- 1.8 V and 2.5 V operation
- Power consumption: 480 mW per-port typical

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Revision History

Revision: 004 Revision Date: December 6, 2002	
Page #	Description
1	Modified first paragraph Modified first line under Applications. Added text under Product Features on title page.
22	Modified Table 2 "IXF1010 Power Supply Signal Descriptions" : added D22 and D24 to GND.
23	Modified Figure 5 "Power Sequencing Diagram"
25	Changed heading from "Features" to Section 3.1.2, "MAC Functions" .
26	Modified Section 3.1.2.3.1, "Filter on Unicast Packet Match" , Section 3.1.2.3.2, "Filter on Multicast Packet Match" , Section 3.1.2.3.3, "Filter Broadcast Packets" .
n/a	Deleted old Table 9: Interface Timing
40	Modified Section 3.2.2.7, "DIP4_UnLock" and Section 3.2.2.8, "DIP4_Lock" .
41	Modified Section 3.2.2.10, "MaxBurst2" (MaxBurst1 to MaxBurst2).
62	Modified Section 3.7.6, "LED Clock" : changed 500 MHz to 720 MHz.
65	Modified Section 4.2, "Reset and Initialization" : changed 220 us to 4.11 ms in third paragraph.
77	Modified Table 30 "Hardware Reset Timing Parameters" : changed min value for Reset Recovery Time.
79	Modified Figure 35 "SPI4-2 Transmit FIFO Status Bus Timing Diagram" and Table 32 "SPI4-2 Transmit FIFO Status Bus Timing Parameters" : modified Parameters.
80	Modified Figure 36 "SPI4-2 Receive FIFO Status Bus Timing Diagram" and Table 33 "SPI4-2 Receive FIFO Status Bus Timing Parameters" : modified Parameters.
88	Added JTAG Register to Table 38 "Global Status and Configuration Register Map" .
98	Modified RxSymbolErrors description in Table 60 "MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)" .
114	Modified Table 75 "LED Flash Rate Register (Addr: 0x50A)" .
116	Added Table 77 "JTAG ID Revision Register (Addr: 0x50C)" .
128	Changed Default value in Table 85 "TX FIFO MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D)" .
137	Modified bits 12 and 28 descriptions in Table 95 "SPI4-2 RX Calendar Register (Addr: 0x702)"
138	Changed default value for bits 15:8 in Table 96 "SPI4-2 TX Synchronization Register (Addr: 0x703)" .
140	Added marking diagram under Section 7.2.1, "Markings" .

Revision: 003 Revision Date: October 7, 2002	
Page #	Description
1	Modified Product Features on front page: Added "Integrated termination" under SPI4-2 Interface
15	Modified Figure 3 "IXF1010 552-Ball CBGA Assignments (Top View)" .

Revision: 003 Revision Date: October 7, 2002	
Page #	Description
17	Modified Table 1 "IXF1010 Signal Pins":
22	Modified Table 2 "IXF1010 Power Supply Signal Descriptions".
23	Added new section: Section 2.2 , "Power Sequencing" including Figure 5 "Power Sequencing Diagram" and Table 4 "Power Sequencing".
26	Added Note under Section 3.1.2.3 , "Filtering of Receive Packets" regarding jumbo frames.
29	Modified text under Section 3.1.4 , "Jumbo Packet Support".
35	Added new section: Section 3.2.1.1 , "Control Words", including Table 9 "Control Word Format" and Table 10 "Control Word Definitions".
37	Added new section: Section 3.2.1.2 , "DIP4".
43	Modified Figure 12 "FIFO Status State Diagram".
60	Updated Table 22 "Read Timing Diagram - Asynchronous Interface" and Table 23 "Write Timing Diagram - Asynchronous Interface".
61	Added bullet to Section 3.7.2 , "SPI4-2 Receive and Transmit Data Path Clocks": "TSCLK frequency is 1/4 TDCLK frequency."
69	Modified Table 23 "RGMII 1000 Mbps Timing Specifics": Data-to-Clock Input skew Typ = 1.5 ns. Removed "Duty cycle for 100T" line.
71	Modified Table 25 "RGMII 100 Mbps Timing Specifics": Typ value for Data-to-Clock Input Skew. Removed "Duty Cycle for Gigabit" line.
67	Added Note 2 to Table 21 "2.5 V LVTTTL and CMOS I/O Electrical Characteristics".
77	Modified Table 30 "Hardware Reset Timing Parameters": Min value of Reset Recovery Time.
77	Modified Table 30 "Hardware Reset Timing Parameters": Reset Pulse Wide Min = 100 ns. Reset Recovery Time Min = 220 μ s.
88	Modified Table 38 "Global Status and Configuration Register Map".
94	Added text to bits 9:0 description under Table 50 – "Specified in multiples of 512 bit times.
94	Added text to bits 9:0 description under Table 51 – "Specified in multiples of 512 bit times.
93	Added text to bits 9:0 description under Table 49 "IPG Transmit Time Register (Addr: Port_Index + 0x0C)" – "Specified in multiples of 512 bit times.
93	Added text to bits 15:0 description under Table 50 "Pause Threshold Register (Addr: Port_Index + 0x0E)" – "Specified in multiples of 512 bit times.
95	Added "table note 3" to Table 57 "RX Packet Filter Control Register (Addr: Port_Index + 0x19)".
102	Table 61 "MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)": Changed "TXOctetsTransmittedOK" to "TXOctetsTotalOK". TxPkts1519toMaxOctets: changed 1526 to 1523.
112	Modified Register Description under Table 70 "Port Enable Register (Addr: 0x500)": Change "Setting the bit to 0 de-asserts the reset." to "Setting the bit to 0 disables the port."
114	Modified Table 74 "LED Control Register (Addr: 0x509)": Bit 0: Changed "LED Control" to "LED_SEL_mode".
136	Modified bit 31 description under Table 93 "SPI4-2 RX Burst Size Register (Addr: 0x700)".
137	Modified Table 95 "SPI4-2 RX Calendar Register (Addr: 0x702)": Modified descriptions for bits 19:16, 11:8, and 3:0.

Revision: 003 Revision Date: October 7, 2002	
Page #	Description
138	Modified Table 96 "SPI4-2 TX Synchronization Register (Addr: 0x703)": Added new description for bits 7:4.

Revision: 002 Revision Date: July 2002	
Page #	Description
20	Modified Figure 8 "IXF1110 552-Ball CBGA Assignments (Top View)".
22	Modified Table 1 "IXF1010/IXF1110 Signal Pins".
31	Modified Table 3 "IXF1110 Power Supply Signal Descriptions".
28	Added Section 3.1.4, "Jumbo Packet Support".
30	Replaced Section 3.1.5, "RMON Statistics Support".
46	Added Figure 12 "IXF1010/IXF1110 SPI4-2 Interfacing with the Network Processor or Forwarding Engine".
62	Modified sections under Section 3.7, "Clocks".
66	Added Section 4.3, "Extras and Back up".
89	Modified all register maps under Section 6.5, "Memory Map".

Related Documents

Title	Order
IXF1010 and IXF1110 10-Port Gigabit Ethernet Media Access Controllers Design and Layout Guide	250676
IXF1010 Demo Board Development Kit Manual	250709
SPI4 Phase 2 Performance in Gigabit Ethernet Media Access Controllers Application Note	250643
Interfacing with IXF1010 and IXF1110 10-Port Gigabit Ethernet Media Access Controllers Application Note	250856
IXF1010 Thermal Design Considerations Application Note	250288
Flow Control in IXF1010 and IXF1110 10-Port Gigabit Ethernet Media Access Controllers Application Note	250236

1.0 General Description

The Intel® IXF1010 is a 10-port 100/1000 Mbps Ethernet Media Access Controller (MAC). The 10 Gigabit interface to the network processor is supported through a System Packet Interface Level 4 Phase 2 (SPI4-2), while the PHY interface is RGMII (Reduced Gigabit Media Independent Interface). Figure 1 represents the IXF1010 block diagram and Figure 2 illustrates the IXF1010 system block diagram.

Figure 1. IXF1010 Block Diagram

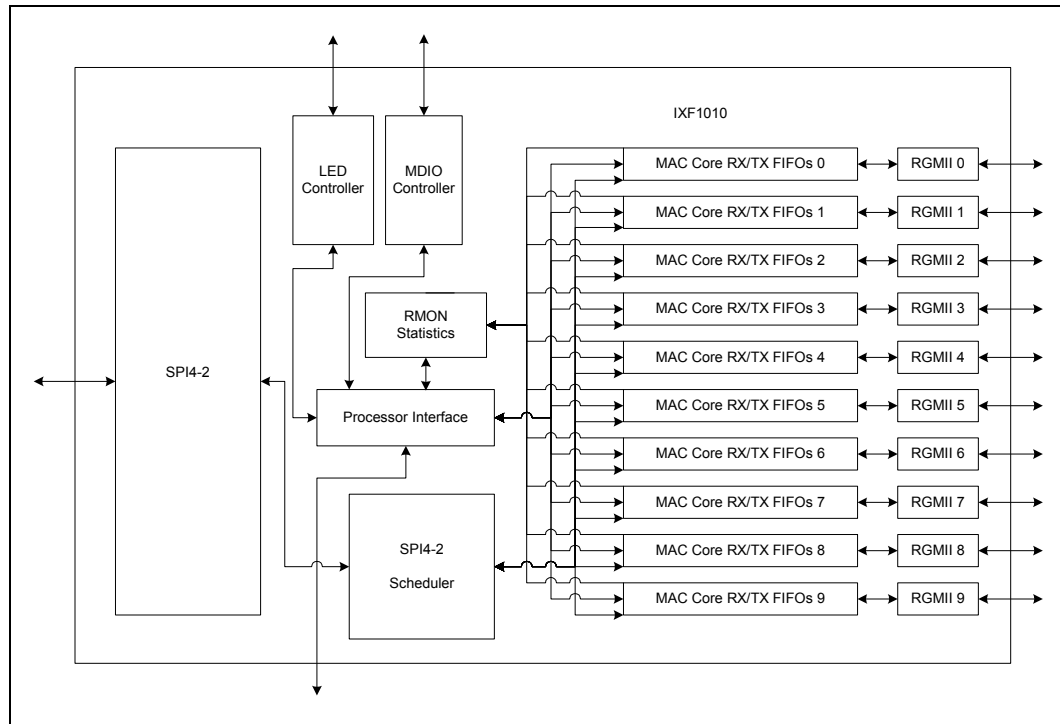


Figure 2. IXF1010 System Block Diagram

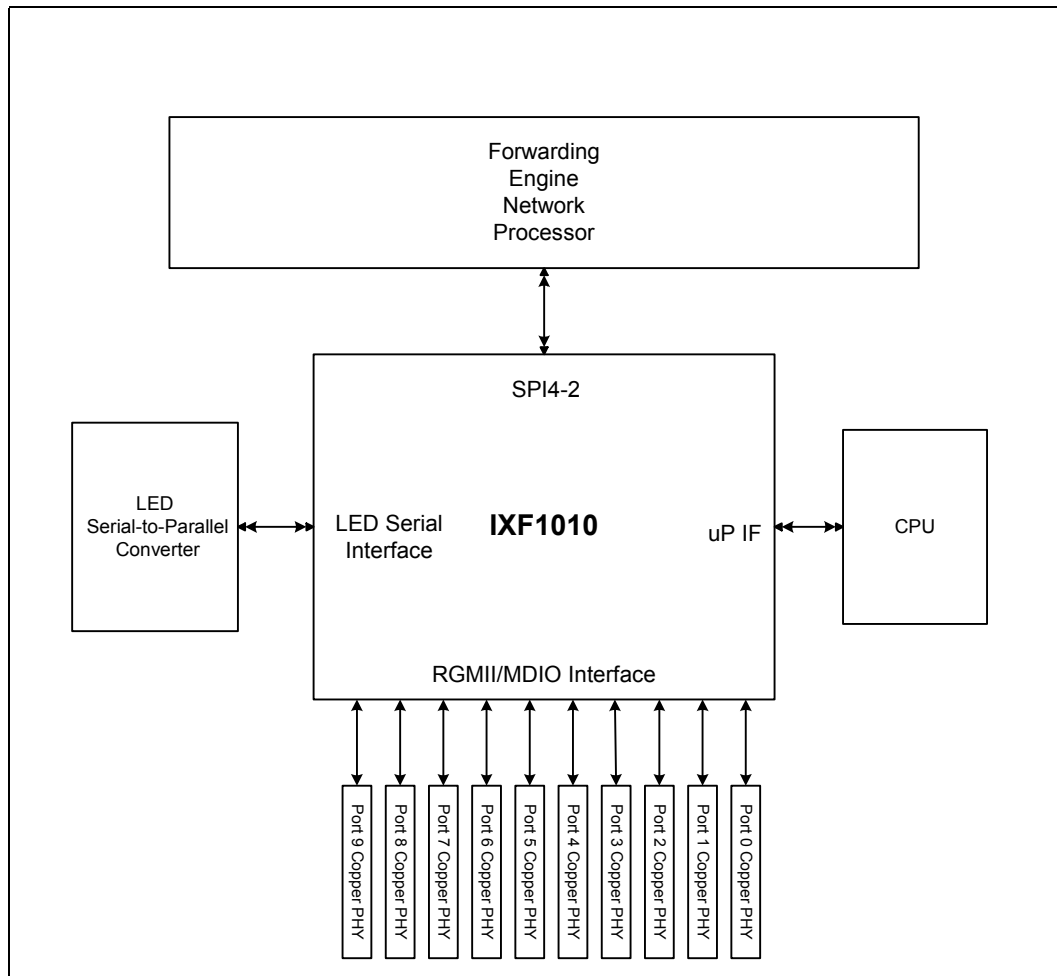




Figure 3 provides the physical layout of the balls, labeled with their ball number (matrix layout) and signal name.

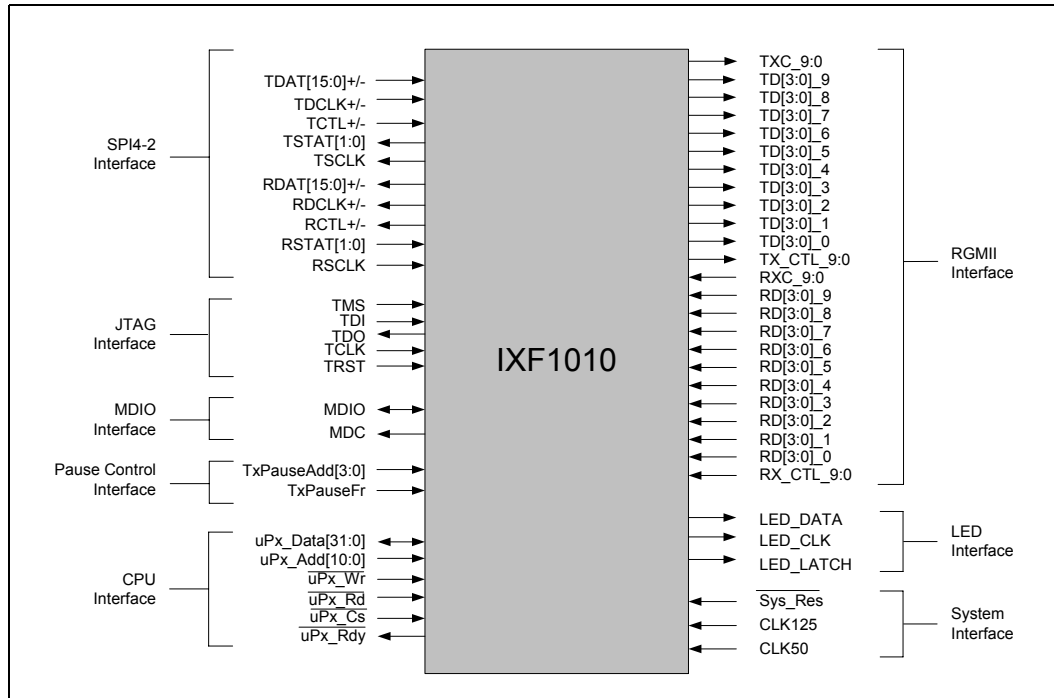
Figure 3. IXF1010 552-Ball CBGA Assignments (Top View)

AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	No Ball	No Ball	GND	A/VD2	NC	NC	NC	NC	RXC.9	RZ2.9	TXC.9	TD2.9	TX_CTL.9	TxFuse_A05	uPA_A00	uP_A03	uPA_A06	uPA_A05	GND	A/VD2	No Ball	No Ball	No Pd
2	No Ball	TX_CTL.7	VD2	GND	GND	RZ3.6	VD2	TD3.8	GND	TD3.9	VD2	VD2	TD1.9	GND	TxFuse_A02	VD2	TxFuse_A01	GND	uPA_A05	VD2	uPA_A01	No Ball	No Ball
3	No Ball	TD3.7	NC	GND	GND	GND	NC	NC	RZ3.9	NC	NC	RD1.9	RX_CTL.9	VD	TDAT1-	TDAT1+	TxFuse_A00	uPA_A02	uPA_A04	TDCLK+	uPA_A07	uPA_Dat0	No Ball
4	TD2.7	VD2	GND	Sys_Res	VD	GND	GND	TX_CTL.6	VD	TD1.9	GND	GND	RD0.9	VD	VD	GND	uPA_A01	VD	TDCLK	GND	GND	VD2	uPA_Dat1
5	TD0.7	TD1.7	NC	CLK125	RD3.8	GND	NC	NC	TD2.8	NC	TXC.8	TDATB+	TDATB+	VD	TDAT0-	TDAT5-	TDAT5+	uPA_A08	TS1A10	GND	TDAT2+	NC	5
6	TXC.7	GND	RXC.8	VD	GND	NC	VD2	TD0.8	GND	NC	VD2	VD2	RD1.6	GND	TDAT0+	VD2	TDAT4-	GND	TS1A11	VD	TDAT7-	GND	NC
7	NC	RD1.7	RD2.7	TX_CTL.7	TD0.6	RD0.8	RD1.8	RD2.8	TX_CTL.8	NC	NC	NC	TDATB-	NC	TxFuseFF	TDAT12+	NC	TDAT4+	TDAT11-	uPA_Dat15	TDAT7+	TDAT9-	uPA_Dat3
8	NC	VD2	TD2.6	GND	VD2	NC	GND	RX_CTL.6	VD	TD1.8	GND	GND	TDATB+	VD	TDAT12-	GND	NC	VD2	TDAT11+	GND	TDAT9-	VD2	uPA_Dat7
9	NC	NC	RD0.7	TD3.6	TD1.6	TD2.5	VD2	RD2.6	GND	VD	VD2	VD2	VD	GND	TDAT13-	TDAT3-	TDAT3+	TDAT10-	TDAT10+	TDAT14-	TDAT14+	uPA_Dat2	uPA_Dat9
10	NC	GND	RD2.5	TD0.5	GND	NC	VD	GND	RXC.6	GND	TCIL-	TCIL+	GND	TDAT13-	GND	VD	VD2	GND	uPA_Dat13	VD	NC	GND	uPA_Dat6
11	NC	RX_CTL.5	NC	TXC.5	TD1.5	NC	TX_CTL.5	VD	GND	VD	GND	GND	VD	GND	VD	TDAT15+	TDAT15+	uPA_Dat14	uPA_Dat6	VD	TSCLK	NC	uPA_Dat11
12	NC	VD2	GND	RD3.5	VD2	TD3.5	GND	VD2	TD3.3	GND	VD2	VD2	GND	RDAT15+	VD2	GND	uPA_Dat12	VD2	uPA_Dat10	GND	uPA_Dat4	VD2	uPA_Dat19
13	GND	VD2	GND	RD1.5	VD2	RD3.4	GND	VD2	TD2.3	GND	VD2	VD2	GND	RDAT15-	VD2	GND	uPA_Dat21	VD2	RDAT13+	GND	uPA_Dat6	VD2	RDAT12+
14	GND	TX_CTL.4	GND	RX_CTL.4	NC	TD1.4	RD0.4	VD	GND	VD	GND	GND	VD	GND	VD	uPA_R0	uPA_Dat24	uPA_Dat18	RDAT13-	uPA_Dat16	uPA_Dat17	NC	RDAT12-
15	GND	GND	TD3.4	VD	GND	NC	VD	GND	TD1.3	GND	RDAT7-	RDAT7+	GND	RDAT11-	GND	VD	NC	GND	uPA_Dat23	VD	NC	GND	uPA_Dat20
16	GND	GND	TX_CTL.2	RD1.4	TXC.4	RD2.4	RD3.3	TD3.3	GND	VD	VD2	VD2	VD	GND	RDAT11+	RDCL+	RDAT14+	RDAT14+	RDAT6+	RDAT6-	RDAT8+	uPA_Dat22	uPA_Dat25
17	NC	VD2	RD0.5	TD1.2	VD2	TD3.1	GND	RD2.3	VD	TD1.1	GND	GND	RDAT5+	VD	RZCLK	GND	RDAT10+	VD2	RDAT6-	GND	uPA_Dat26	VD2	uPA_Dat27
18	TD3.2	TD1.2	TD0.5	RXC.4	TD1.4	NC	RD0.3	RX_CTL.3	NC	NC	TRST	RD3.0	RDAT5-	LED_LATCH	RDAT4+	RDCL-	RDAT10-	RDAT2+	RDAT6-	RDAT8+	RDCLK+	uPA_Dat28	uPA_Dat27
19	TD2.2	GND	TXC.3	VD	GND	NC	VD2	RD1.3	GND	NC	VD2	VD2	NC	GND	RDAT4-	VD2	RDAT2-	GND	RDAT6+	VD	RDCLK	GND	LED_CLK
20	TXC.2	RD2.2	NC	TD2.4	NC	RX_CTL.2	GND	GND	TXC.1	NC	TD2.1	TX_CTL.3	RSTAT0	RDZ.0	RDAT3-	RDAT3+	NC	uPA_Cs	RDAT0-	VD	RDAT1+	LED_DATA	20
21	RD1.2	VD2	RD0.2	GND	TX_CTL.1	VD	GND	RD2.1	VD	RXC.3	GND	GND	TD2.0	VD	RXC.0	GND	RDAT3+	VD	VD	GND	CL60	VD2	uPA_Dat29
22	No Ball	RD0.2	NC	TD0.3	NC	NC	GND	GND	TXC.0	NC	NC	RD0.1	TD3.0	RD0.0	MDIO	NC	NC	NC	NC	GND	uPA_R0	uPA_Dat30	No Ball
23	No Ball	No Ball	RXC.2	VD2	NC	GND	VD2	RXC.1	GND	RD3.1	VD2	VD2	TD0.0	GND	GND	VD2	NC	GND	NC	VD2	uPA_Dat31	No Ball	No Ball
24	No Ball	No Ball	TDCLK	TD0	GND	GND	GND	GND	RX_CTL.1	RD1.1	TX_CTL.0	TD1.0	RX_CTL.0	RD1.0	NC	NC	NC	NC	A/VD2	GND	No Ball	No Ball	No Ball
AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A

2.0 Pin Assignments and Signal Descriptions

Figure 4 and Table 1 through Table 3 on page 23 provide the signal pins used by the IXF1010

Figure 4. IXF1010 Pinout Diagram



2.1 Signal Name Conventions

Signal names may contain either a port designation (PHY interface) or a serial designation (System Interface). Signal naming conventions are as follows:

Port Designation. Individual signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by an underscore and the Port Designation. For example, RGMII Transmit Control signals would be identified as TX_CTL_0, TX_CTL_1, TX_CTL_2, etc.

Serial Designation. A set of signals that are not tied to any specific port are designated by the Signal Mnemonic, followed by a bracketed serial designation. For example, SPI4-2 Transmit Data Bus signals would be identified as TDAT[15:0].

Port Bus Designation: A set of bus signals that apply to a particular port are designated by the Signal Mnemonic, immediately followed by a bracketed bus designation, followed by an underscore and the port designation. For example, RGMII transmit data bus signals would be identified as TD[3:0]_0, TD[3:0]_1, TD[3:0]_2, etc.

Table 1. IXF1010 Signal Pins

Ball Designator	Signal Name	Type	Standard	Signal Description
SPI4-2 Interface				
G11, H11 C9, D9 J9, K10 H7, J8 E8, E7 E9, F9 B7, C8 L5, M5 C7, C6 L8, L7 G5, H5 F7, G6 G9, H9 B5, C5 H3, J3 J6, J5	TDAT15+/- TDAT14+/- TDAT13+/- TDAT12+/- TDAT11+/- TDAT10+/- TDAT9+/- TDAT8+/- TDAT7+/- TDAT6+/- TDAT5+/- TDAT4+/- TDAT3+/- TDAT2+/- TDAT1+/- TDAT0+/-	Input	LVDS	Transmit Data Bus: Carries payload data and in-band control words to the IXF1010 link-layer device. Internally terminated differentially with 100 Ω.
D3, E4	TDCLK+, TDCLK-	Input	LVDS	Transmit Data Clock: Clock associated with TDAT[15:0] and TCTL. Data and control lines are driven off the rising and falling edges of the clock. Internally terminated differentially with 100 Ω.
M10, N10	TCTL+, TCTL-	Input	LVDS	Transmit Control: TCTL is High when a control word is present on TDAT[15:0]. Otherwise, TCTL is Low. Internally terminated differentially with 100 Ω.
C11	TSCLK	Output	2.5 V LVTTTL	Transmit Status Clock: Clock associated with TSTAT [1:0]. Frequency is equal to one-quarter TDCLK.
E6, E5	TSTAT1, TSTAT0	Output	2.5 V LVTTTL	Transmit FIFO Status: Carries round-robin FIFO status information, along with associated error detection and framing.
K12, K13 F16, G16 E13, E14 A13, A14 J16, K15 G17, G18 D18, E18 C16, D16 M15, N15 E16, E17 L17, L18 J18, J19 G21, H20 F18, G19 B20, C20 E19, E20	RDAT15+/- RDAT14+/- RDAT13+/- RDAT12+/- RDAT11+/- RDAT10+/- RDAT9+/- RDAT8+/- RDAT7+/- RDAT6+/- RDAT5+/- RDAT4+/- RDAT3+/- RDAT2+/- RDAT1+/- RDAT0+/-	Output	LVDS	Receive Data: Carries payload data and in-band control from the IXF1010 link-layer device.

Table 1. IXF1010 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
C18, C19	RDCLK+, RDCLK-	Output	LVDS	Receive Data Clock: Clock associated with RDATA[15:0] and RCTL. Data and control lines are driven off the rising and falling edges of the clock.
H16, H18	RCTL+, RCTL-	Output	LVDS	Receive Control: RCTL is High when a control word is present on RDATA[15:0]. Otherwise, RCTL is Low.
J17	RSCLK	Input	2.5 V LVTTTL	Receive Status Clock: Clock associated with RSTAT[1:0].
J20, L20	RSTAT1, RSTAT0	Input	2.5 V LVTTTL	Receive FIFO Status: Carries round-robin FIFO status information, along with associated error detection and framing.
RGMI Interface				
N1, N5, AD6, Y11, AA11, W16, AB19, AD20, R20, R22	TXC_9, TXC_8, TXC_7, TXC_6, TXC_5, TXC_4, TXC_3, TXC_2, TXC_1, TXC_0	Output	2.5 V CMOS	Transmit Reference Clock: Operates at: 125 MHz for 1 Gigabit operation 25 MHz for 100 Mbps operation
P2, M1, L2, P4, T2, R5, P8, T6, AC3, AD4, AC5, AD5, Y9, AB8, W9, Y7, V12, V9, W11, Y10, AB15, AA20, W14, W18, R12, R13, R15, AA22, AD18, AD19, Y17, AB18, V17, N20, V23, P17, L22, L21, M24, L23	TD[3:0]_9 TD[3:0]_8 TD[3:0]_7 TD[3:0]_6 TD[3:0]_5 TD[3:0]_4 TD[3:0]_3 TD[3:0]_2 TD[3:0]_1 TD[3:0]_0	Output	2.5 V CMOS	Transmit Data: This bus contains bits 3:0 on the rising edge of the TXC and bits 7:4 on the falling edge of TXC.
L1, R7, AB2, T4, U11, AC14, M20, AA16, Y21, N24	TX_CTL_9, TX_CTL_8, TX_CTL_7, TX_CTL_6, TX_CTL_5, TX_CTL_4, TX_CTL_3, TX_CTL_2, TX_CTL_1, TX_CTL_0	Output	2.5 V CMOS	Transmit Control: This signal is TXEN on the rising edge of TXC and a logical derivative of TXEN and TXERR on the falling edge.
R1, AB6, W7, R10, AB17, Y18, P21, AB23, T23, J21	RXC_9, RXC_8, RXC_7, RXC_6, RXC_5, RXC_4, RXC_3, RXC_2, RXC_1, RXC_0,	Input	2.5 V CMOS	Receiver reference clock: 125 MHz for 1 Gigabit operation 25 MHz for 100 Mbps operation

Table 1. IXF1010 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
R3, P1, M3, L4, W5, T7, U7, V7, Y8, AB7, AC7, AA9, V2, T9, L6, U9, Y12, AB10, Y13, AA18, V13, V16, Y16, U14, U16, T17, T19, U18, AB21, AC20, AD21, AC22, P23, T21, P24, M22, M18, K20, K24, K22	RD[3:0]_9 RD[3:0]_8 RD[3:0]_7 RD[3:0]_6 RD[3:0]_5 RD[3:0]_4 RD[3:0]_3 RD[3:0]_2 RD[3:0]_1 RD[3:0]_0	Input	2.5 V CMOS	Receive Data: This bus contains bits 3:0 on the rising edge of the clock and bits 7:4 on the falling edge.
L3, AA3, AA7, T8, AC11, AA14, T18, W20, R24, L24	RX_CTL_9, RX_CTL_8, RX_CTL_7, RX_CTL_6, RX_CTL_5, RX_CTL_4, RX_CTL_3, RX_CTL_2, RX_CTL_1, RX_CTL_0,	Input	2.5 V CMOS	Receive Control: This signal is RXDV on the rising edge of RXC and a logical derivative of RXDV and RXERR on the falling edge.
CPU Interface				
C2 F1 F5 C3 G1 E2 E3 H1 F3 G4 J1	uPx_Add10 uPx_Add9 uPx_Add8 uPx_Add7 uPx_Add6 uPx_Add5 uPx_Add4 uPx_Add3 uPx_Add2 uPx_Add1 uPx_Add0	Input	2.5 V CMOS	Address bus: 11-bit address bus
F20	$\overline{\text{uPx_Cs}}$	Input	2.5 V CMOS	Chip Select Signal: Active Low chip select

Table 1. IXF1010 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
C23 B22 A21 B18 A17 C17 A16 G14 E15 B16 G13 A15 A12 F14 C14 D14 D7 F11 E10 G12 A11 E12 A9 A10 A8 C13 E11 C12 A7 B9 A4 B3	uPx_Data31 uPx_Data30 uPx_Data29 uPx_Data28 uPx_Data27 uPx_Data26 uPx_Data25 uPx_Data24 uPx_Data23 uPx_Data22 uPx_Data21 uPx_Data20 uPx_Data19 uPx_Data18 uPx_Data17 uPx_Data16 uPx_Data15 uPx_Data14 uPx_Data13 uPx_Data12 uPx_Data11 uPx_Data10 uPx_Data9 uPx_Data8 uPx_Data7 uPx_Data6 uPx_Data5 uPx_Data4 uPx_Data3 uPx_Data2 uPx_Data1 uPx_Data0	Input/ Output	2.5 V CMOS	Bi-directional data bus: 32-bit bi-directional data bus
A18	$\overline{\text{uPx_Wr}}$	Input	2.5 V CMOS	Write Strobe: Active Low Write strobe
H14	$\overline{\text{uPx_Rd}}$	Input	2.5 V CMOS	Read Strobe: Active Low Read strobe
C22	$\overline{\text{uPx_Rdy}}$	Open Drain Output	2.5 V CMOS	Cycle complete indicator: Indicates that Read or Write is complete
Pause Control Interface				
J7	TxPauseFr	Input	2.5 V CMOS	Pause Strobe: Indicates when a Pause frame is to be sent
K1 J2 G2 G3	TxPauseAdd3 TxPauseAdd2 TxPauseAdd1 TxPauseAdd0	Input	2.5 V CMOS	Pause Address Bus: Selects the port for the Pause frames
MDIO Interface				
J22	MDIO	Input/ Output	2.5 V CMOS	Management Data Input/ Output: Data signal for MDIO.
H22	MDC	Output	2.5 V CMOS	Management Data Clock: Clock to external devices.
LED Interface				
A19	LED_CLK	Output	2.5 V CMOS	LED Clock: Clock output for the LED block.

Table 1. IXF1010 Signal Pins (Continued)

Ball Designator	Signal Name	Type	Standard	Signal Description
A20	LED_DATA	Output	2.5 V CMOS	LED Data: Data output for the LED block.
K18	LED_LATCH	Output	2.5 V CMOS	LED Latch: Latch enable for the LED block.
JTAG Interface				
AA24	TCLK	Input	2.5 V CMOS	JTAG Test Clock: Reference clock for JTAG.
T16	TMS	Input	2.5 V CMOS	JTAG Test Mode Select: Selects test mode for JTAG.
AC18	TDI	Input	2.5 V CMOS	JTAG Test Data Input: Test data sampled with respect to the rising edge of TCK.
N18	TRST	Input	2.5 V CMOS	JTAG Test Reset: Reset input for JTAG test.
Y24	TDO	Output	2.5 V CMOS	JTAG Test Data Output: Test data driven with respect to the falling edge of TCK.
System Interface				
AA5	CLK125	Input	2.5 V CMOS	125 MHz Reference Clock: Input clock to PLL.
C21	CLK50	Input	2.5 V CMOS	SPI4-2 Reference Clock: Input clock to SPI4-2 RX PLL. Input range is 40 MHz to 50 MHz. This clock multiplied by eight must equal the required SPI4-2 data clock frequency.
Y4	$\overline{\text{Sys_Res}}$	Input	2.5 V CMOS	System Reset: System hard reset (active Low).

Table 2. IXF1010 Power Supply Signal Descriptions

Ball Designator	Signal Name	Type	Standard	Signal Description
D1, E24	AVDD	–	–	1.8 V Analog Power Supply: 1.8 V supply for analog circuits.
Y1	AVDD2	–	–	2.5 V Analog Power Supply: 2.5 V supply for analog circuits.
D6, D10, D11, D15, D19, D20, E21, F4, F21, H10, H15, J4, J11, J14, K3, K4, K5, K8, K17, K21, L9, L11, L14, L16, P9, P11, P14, P16, R4, R8, R17, R21, T11, T14, U10, U15, W4, W21, AA6, AA10, AA15, AA19, AB4	VDD	–	–	1.8 V Digital Power Supply: 1.8 V core supply.
B4, B8, B12, B13, B17, B21, D2, D23, F8, F12, F13, F17, G10, H2, H6, H19, H23, J12, J13, M2, M6, M9, M12, M13, M16, M19, M23, N2, N6, N9, N12, N13, N16, N19, N23, T12, T13, U2, U6, U19, U23, W8, W12, W13, W17, AA2, AA23, AC4, AC8, AC12, AC13, AC17, AC21	VDD2	–	–	2.5 V Digital Power Supply: 2.5 V I/O supply.
B6, B10, B15, B19, C4, D4, D5, D8, D12, D13, D17, D21, D22, D24, E1, F2, F6, F10, F15, F19, F23, H4, H8, H12, H13, H17, H21, J10, J15, J23, K2, K6, K9, K11, K14, K16, K19, K23, L10, L12, L13, L15, M4, M8, M11, M14, M17, M21, N4, N8, N11, N14, N17, N21, P10, P12, P13, P15, R2, R6, R9, R11, R14, R16, R19, R23, T10, T15, T20, T22, T24, U4, U8, U12, U13, U17, U20, U21, U22, U24, V3, V4, V5, V24, W2, W3, W6, W10, W15, W19, W23, W24, Y2, Y3, Y5, Y6, Y15, AA1, AA4, AA8, AA12, AA13, AA17, AA21, AB13, AB14, AB16, AC6, AC10, AC15, AC16, AC19, AD13, AD14, AD15, AD16	GND	–	–	Ground: Ground return for all signals.

Table 3. IXF1010 Unused Balls/Reserved

Ball Designator	Signal Name	Type	Standard	Signal Description
A5, A6, B11, B14, C10, C15, E22, E23, F22, F24, G7, G8, G15, G20, G22, G23, G24, H24, J24, K7, L19, M7, N3, N7, N22, P3, P5, P6, P7, P18, P19, P20, P22, R18, T1, T3, T5, U1, U3, U5, V1, V6, V8, V10, V11, V14, V15, V18, V19, V20, V21, V22, W1, W22, Y14, Y19, Y20, Y22, Y23, AB3, AB5, AB9, AB11, AB12, AB20, AB22, AC9, AD7, AD8, AD9, AD10, AD11, AD12, AD17	N/C	–	–	No connection.
A2, A3, A22, A23, A24, B1, B2, B23, B24, C1, C24, AB1, AB24, AC1, AC2, AC23, AC24, AD1, AD2, AD3, AD22, AD23, AD24	No Ball	–	–	Balls removed from substrate.
A1	No Pad	–	–	Pad removed from substrate.

2.2 Power Sequencing

Correct operation requires a power-up and power-down sequence. Failure to follow this sequence can result in damage to the device. The sequence described in this section covers digital and analog supplies for the device.

Ensure that the 1.8 V supplies (VDD/AVDD) are applied and stable prior to the application of the 2.5 V supplies (VDD2/AVDD2).

Note: If the 2.5 V supplies (VDD2/AVDD2) exceed the 1.8 V core supplies (VDD/AVDD) by more than 2.0 V during power-up or power-down, damage can occur to the ESD structures within the Analog IOs.

Since the power-down sequence is the reverse of the power-up sequence, remove the 2.5 V supplies (VDD2/AVDD2) prior to the removal of the 1.8 V core supplies (VDD/VDD2).

Figure 5. Power Sequencing Diagram

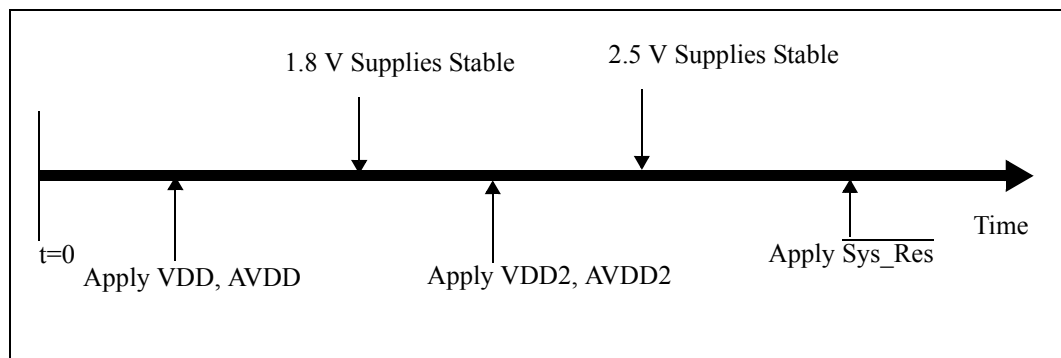


Table 4. Power Sequencing

Power Supply	Power-Up Order	Time Delta to Next Supply ¹	Description
VDD, AVDD	First	0	1.8 V supplies
VDD2, AVDD2	Second	10 μ s	2.5 V supplies

1. The value of 10 μ s given is a nominal value only. The exact time difference between the application of the 2.5 V analog supply will be determined by a number of factors dependent on the power management method used. The key requirement that must be met to avoid damage to the device is that the AVDD2 supply must not exceed the VDD supply by more than 2 V at any time during the power-up or power-down sequence.

3.0 Functional Descriptions

3.1 Media Access Controller

3.1.1 General Description

The Intel® IXF1010 main functional block consists of a 100/1000 Mbps Ethernet Media Access Controller (MAC), supporting the following features:

- 100/1000 Mbps full-duplex operation
- Independent enable/disable of any port
- Detection of length error, runt, or overly large packets
- RMON statistics and error counters
- Cyclic Redundancy Check (CRC) calculation and error detection
- Programmable option to:
 - Filter packets with errors
 - Filter, broadcast, multicast, and unicast address packets
 - Automatically pad transmitted packets less than the minimum frame size
- Compliance with IEEE 802.3x Standard for Flow Control (symmetric pause capability)
- Full compliance with the HP version 1.2a Reduced Gigabit Media Independent Interface (RGMII)

The MAC is fully integrated, designed for use with Ethernet 802.3 Frame types, and is compliant with all of the required IEEE 802.3 MAC requirements.

The MAC adds preamble and Start-of-Frame Delimiter (SFD) to all frames sent to it (transmit path) and removes preamble and SFD on all frames received by it (receive path). A CRC check is also applied to all transmit and receive packets. Packets with a bad CRC are marked, counted in the statistics block, and may be optionally dropped or sent to the SPI4-2 interface.

Note: The MAC operates in full-duplex mode only. The PHY, to which the MAC is attached, must advertise full-duplex mode during any auto-negotiation process.

3.1.2 MAC Functions

Section 3.1.2.1, “Padding of Undersized Frames on Transmit” on page 25 through Section 3.1.2.4, “PAUSE Command Frames” on page 28 cover the MAC functions.

3.1.2.1 Padding of Undersized Frames on Transmit

The padding feature allows Ethernet frames smaller than 64 bytes to be transferred across the SPI4-2 interface and automatically padded up to 64 bytes by the MAC. This feature is enabled by setting bit 7 of the Diverse Config Register = 1 (Address Port_Index + 0x18h). See [Table 56 on page 95](#).

3.1.2.2 Automatic CRC Generation

The Automatic CRC Generation is used in conjunction with the padding feature to generate and append a correct CRC to any incoming frame from the SPI4-2 interface. This feature is enabled by setting bit 6 of the Diverse Config Register = 1 (Address Port_Index + 0x18h) (see [Table 56 on page 95](#)).

Note: When padding of undersized frames on transmit is enabled, the automatic CRC generation must be enabled for proper operation of the IXF1010.

3.1.2.3 Filtering of Receive Packets

This feature allows the MAC to filter receive packets under various conditions and drop the packets via an interaction with the Receive FIFO control.

Note: Jumbo frames (1519 - 9600 bytes) matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, are not dropped. Instead, jumbo frames that are expected to be dropped by the RX FIFO, based on the filter settings in [Table 57, “RX Packet Filter Control Register \(Addr: Port_Index + 0x19\)” on page 95](#), are sent across the SPI4-2 interface as an EOP abort frame. Jumbo frames matching the filter conditions are not counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in the “RX Packet Filter Control Register (Addr: Port_Index + 0x19)” are actually dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.

3.1.2.3.1 Filter on Unicast Packet Match

This feature is enabled when bit 0 of the RX Packet Filter Control Register = 1. Any frame received in this mode containing a Unicast Destination Address which does not match the Station Address is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all unicast frames are sent to the SPI4-2 interface.

3.1.2.3.2 Filter on Multicast Packet Match

This feature is enabled when bit 1 of the RX Packet Filter Control Register = 1. Any frame received in this mode containing a Multicast Destination Address which does not match the Port Multicast Address is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable register = 1. Otherwise, all multicast frames are sent to the SPI4-2 interface.

3.1.2.3.3 Filter Broadcast Packets

This feature is enabled when bit 2 of the RX Packet Filter Control Register = 1. Any broadcast frame received in this mode is marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all broadcast frames are sent to the SPI4-2 interface.

3.1.2.3.4 Filter VLAN Packets

This feature is enabled when bit 3 of the RX Packet Filter Control Register = 1. VLAN frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all VLAN frames are sent to the SPI4-2 interface.

3.1.2.3.5 Filter PAUSE Packets

This feature is enabled when bit 4 of the RX Packet Filter Control Register = 0. PAUSE frames received in this mode are marked by the MAC to be dropped. The frame is dropped if the appropriate bit in the RX FIFO Errored Frame Drop Enable Register = 1. Otherwise, all PAUSE frames are sent to the SPI4-2 interface.

Table 5. Pause Packets Drop Enable Behavior

Pause Frame Pass	Frame Drop En	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and sent to the switch or Network Processor, regardless of the Frame Drop En setting.
0	1	PAUSE Packets are marked as bad, are dropped in the RX FIFO, and never appear at the SPI4-2 interface.

3.1.2.3.6 Filter CRC Errored Packets

This feature is enabled when bit 5 of the RX Packet Filter Control Register = 0. Frames received with an errored CRC are marked as bad frames and may optionally be dropped in the RX FIFO. Otherwise, the frames are sent to the SPI4-2 interface and may be dropped by the switch or system controller (see [Table 6](#)).

Table 6. CRC Errored Packets Drop Enable Behavior

CRC Errored PASS	Frame Drop En	Actions
1	0	Packets are passed to the SPI4-2 interface. They are not marked as bad and are sent to the switch or Network Processor.
0	0	Packets are marked as bad but not dropped in the RX FIFO. These packets are sent to the SPI4-2 interface, but with an EOP Abort code to the switch or Network Processor.
1	1	Packets are not marked as bad and are sent to the switch or Network Processor regardless of the Frame Drop En setting.
0	1	CRC errored packets are marked as bad, dropped in the RX FIFO, and never appear at the SPI4-2 interface.

3.1.2.4 PAUSE Command Frames

The MAC acts on any PAUSE command frames received from the link partner by checking the entire frame and verifying that it is a valid PAUSE control frame addressed to either the Multicast Address (01-80-c2-00-00-01 as specified in IEEE 802.3, Annex 31B) or the Station Address. If the PAUSE frame is valid, the Transmit side of the MAC pauses for the required number of Pause Quanta, as specified in IEEE 802.3u, Clause 31 (see [Table 5](#)).

Note: PAUSE does not begin until completion of the frame currently being transmitted.

3.1.3 Auto-Negotiation

Auto-negotiation is carried out by the PHY connected to the RGMII interface. The PHY registers should be configured to select the desired advertisements based upon the MAC supported abilities and enable auto-negotiation.

The MDIO interface block contains the logic through which the registers in the connected PHYs can be accessed. For more information on the MDIO interface of the IXF1010, refer to [Section 3.4, “MDIO Control and Interface”](#) on page 49.

The following IXF1010 capabilities should be advertised during auto-negotiation in the connected PHY Auto-Negotiation Advertisement Register.

- Speed
 - The IXF1010 supports both 100 and 1000 Mbps operation. All required speed adjustments, clocks, etc., are supplied by the IXF1010. The operating speed of the MAC is programmable via the RGMII Speed Register ([Table 52 on page 94](#)).
- Duplex
 - The IXF1010 supports full-duplex only, and this must be the only mode advertised by the connected PHY during auto-negotiation. If the IXF1010 is connected to a link partner that does not support auto-negotiation and the PHY reverts to parallel detection, the duplex setting between the IXF1010 MAC and the local and remote PHYs become out of step, leading to a link collision.
- Flow Control
 - The connected PHY should advertise that IXF1010 supports the ability to send and receive flow control frames (symmetric).

The IXF1010 polls the PHY via the CPU interface to determine when auto-negotiation is complete. After completion of auto-negotiation by the PHY, the IXF1010 reads the PHY Auto-Negotiation Link Partner Base Page Ability Register. From the settings in this register, the following IXF1010 registers must be programmed to match the connected PHY configuration:

- Speed: The IXF1010 Speed should be set to either 100 or 1000 Mbps in the RGMII Speed Register (Addr: Port Index + 0x10) (see [Table 52 on page 94](#)).
- Link: While link is established, the user must write Link LED Enable Register (Addr: 0x502) (link to register). Note: This register controls link LED (refer to [Section 3.5, “LED Interface”](#) on page 54). The link LED does not update automatically. The Link LED Register should be updated anytime there is a change in link status in order to have the link LED Green show expected behavior.
- Flow Control: If the link partner does not support flow control, the FC Enable Register (Addr: Port Index + 0x12) must be updated to reflect this change (see [Table 53 on page 94](#)).

Note: If any changes in the speed, duplex, or flow control capabilities of the link partner are detected, the user must once again update the IXF1010 registers.

3.1.4 Jumbo Packet Support

The IXF1010 supports the concept of jumbo frames. The jumbo frame length is dependent on the application, and the IXF1010 design has been optimized for 9.6 K jumbo frame length. Lengths larger than this can be programmed, but will limit system performance.

The value programmed into the Max Frame Size Register (Addr: Port_Index + 0x0F) determines the maximum length frame size the MAC can receive or transmit without activating any error counters, and without truncation.

The Max Frame Size Register (Addr: Port_Index + 0x0F) bits 13:0 set the frame length. The default value programmed into this register is 0x05EE (1518). The value is internally adjusted by +4 if the frame has a VLAN tag. The overall programmable maximum is 0x3FFF or 16383 bytes. The register should be programmed to 0x2667 for the 9.6 K length jumbo frame for which the IXF1010 is optimized.

The RMON counters are also affected for jumbo frame support as follows:

RX Statistics:

- RXOctetsTotalOK (Addr: Port_Index + 0x20)
- RXPkts1519toMaxOctets (Addr: Port_Index + 0x2B)
- RXFCSErrors (Addr: Port_Index + 0x2C)
- RXDataError (Addr: Port_Index + 0x02E)
- RXAlignErrors (Addr: Port_Index + 0x2F)
- RXLongErrors (Addr: Port_Index + 0x30)
- RXJabberErrors (Addr: Port_Index + 0x31)
- RXVeryLongErrors (Addr: Port_Index + 0x34)

TX Statistics:

- TXOctetsTotalOK (Addr: Port_Index + 0x40)
- TxPkts1519toMaxOctets (Addr: Port_Index + 0x4B)
- TxExcessiveLengthDrop (Addr: Port_Index + 0x53)
- TXCRCError (Addr: Port_Index + 0x56)

The IXF1010 device checks the CRC for all legal length jumbo frames (frames between 1519 and the Max Frame Size). On transmission, the MAC can be programmed to append the CRC to the frame or check the CRC and increment the appropriate counter. On reception, the MAC transmits these frames across the SPI4-2 interface (jumbo frames with a bad CRC cannot be dropped and are sent across the SPI4-2 interface). If the receive frame has a bad CRC, the appropriate counter is incremented and the EOP Abort code is set in the SPI4-2 control word.

Jumbo frames also impact flow control. The maximum frame size needs to be taken into account when determining the FIFO watermarks. The current transmission must be completed before a Pause frame can be transmitted (needed when the receiver FIFO high watermark has been exceeded). If the current transmission is a jumbo frame, the delay may be significant and increase data loss due to insufficient available FIFO space.

3.1.5 RMON Statistics Support

3.1.5.1 RMON Statistics

The IXF1010 supplies RMON statistics via the CPU interface. These statistics are available in the form of counter values that can be accessed at specific addresses in the IXF1010 memory map. Once read, these counters automatically reset and begin counting from zero. A separate set of RMON statistics is available for each MAC device in the IXF1010.

Implementation of the RMON Statistics block is similar to the functionality provided by existing Intel switch and router products. This implementation allows the IXF1010 to provide all of the RMON Statistics group as defined by RFC2819.

The IXF1010 supports the RMON RFC2819 Group 1 statistics counters. [Table 7](#) notes the differences and additional statistics registers supported by the IXF1010 that are outside the scope of the RMON RFC2819 document.

Table 7. RMON Additional Statistics Registers

RMON Ethernet Statistics Group 1 Statistics	Type	IXF1010 Equivalent Statistics	Type	Definition of RMON Versus IXF1010 Documentation
etherStatsIndex	Integer32	N/A	N/A	N/A
etherStatsDataSource	OBJECT IDENTIFIER	N/A	N/A	N/A
etherStatsDropEvents	Counter32	RX/TX FIFO Number of Frames Removed	Counter 32	See table note 1.
etherStatsOctets	Counter32	RXOctetsTotalOK RXOctetsBad TXOctetsTotalOK TXOctetsBad	Counter 32	Note: The IXF1010 has two counters for RX and TX that use different naming conventions for total Octets and Octets bad. These counters need to be combined to meet the RMON spec.
<p>1. The RMON spec requires that this is, "The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected." The RX/TX FIFO Number of Frames Removed Register in the IXF1010 supports this and will increment when either an RX or TX FIFO has overflowed. If any IXF1010 programmable packet filtering is enabled, the RX/TX Number of Frames Removed Register increments with every frame removed in addition to the existing frames counted due to FIFO overflow.</p> <p>2. The IXF1010 has an extra counter RX/TXUCPkts that can be used.</p> <p>3. The IXF1010 has an extra counter RX/TXPktsToMaxOctets that can be used in addition to the RMON stats. This is required to accommodate the Jumbo packet frames requirement.</p>				

Table 7. RMON Additional Statistics Registers (Continued)

etherStatsPkts	Counter32	RX/TXUCPkts RX/TXBCPkts RX/TXMCPkts	Counter 32	Note: The IXF1010 has three counters for etherStatsPkts that need to be combined to give the total packets as defined by the RMON spec.
etherStatsBroadcastPkts	Counter32	RX/TXBCPkts	Counter 32	OK
etherStatsMulticastPkts	Counter32	RX/TXMCPkts	Counter 32	See table note 2.
etherStatsCRCAAlignErrors	Counter32	RXAlignErrors RXFCSErrors TXCRCErrors	Counter 32	Note: The IXF1010 has two counters for alignment and CRC errors for the RX side only. The IXF1010 has CRCErrors for the TX side.
etherStatsUndersizePkts	Counter32	RXRuntErrors RXShortErrors RX Statistic ONLY	Counter 32	Note: The IXF1010 has two counters for RuntErrors and ShortErrors for the RX side only.
etherStatsOversizePkts	Counter32	RXLongErrors TXExcessiveLengthDrop	Counter 32	OK
etherStatsFragments	Counter32	RXRuntErrors	Counter 32	OK
etherStatsJabbers	Counter32	RXJabberErrors	Counter 32	OK
etherStatsCollisions	Counter32	TXSingleCollisions TXMultipleCollisions TXLateCollisions TXTotalCollisions	Counter 32	OK Note: Registers exist on the TX side but should not increment since the IXF1010 only supports full-duplex.
<p>1. The RMON spec requires that this is, "The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected." The RX/TX FIFO Number of Frames Removed Register in the IXF1010 supports this and will increment when either an RX or TXFIFO has over flowed. If any IXF1010 programmable packet filtering is enabled, the RX/TX Number of Frames Removed Register increments with every frame removed in addition to the existing frames counted due to FIFO overflow.</p> <p>2. The IXF1010 has an extra counter RX/TXUCPkts that can be used.</p> <p>3. The IXF1010 has an extra counter RX/TXPktstoMaxOctets that can be used in addition to the RMON stats. This is required to accommodate the Jumbo packet frames requirement.</p>				

Table 7. RMON Additional Statistics Registers (Continued)

etherStatsPkts64Octets	Counter32	RX/TXPkts64Octets	Counter32	OK
etherStatsPkts65to127Octets	Counter32	RX/TXPkts65to127Octets	Counter32	OK
etherStatsPkts128to255Octets	Counter32	RX/TXPkts128to255Octets	Counter32	OK
etherStatsPkts256to511Octets	Counter32	RX/TXPkts256to511Octets	Counter32	OK
etherStatsPkts512to1023Octets	Counter32	RX/TXPkts512to1023Octets	Counter32	OK
etherStatsPkts1024to1518Octets	Counter32	RX/TXPkts1024to1518Octets	Counter32	See table note 3.
etherStatsOwner	OwnerString	N/A	N/A	N/A
etherStatsStatus	EntryStatus	N/A	N/A	N/A
<p>1. The RMON spec requires that this is, "The total number of events where packets were dropped by the probe due to a lack of resources. Note that this number is not necessarily the number of packets dropped; it is the number of times this condition has been detected." The RX/TX FIFO Number of Frames Removed Register in the IXF1010 supports this and will increment when either an RX or TXFIFO has overflowed. If any IXF1010 programmable packet filtering is enabled, the RX/TX Number of Frames Removed Register increments with every frame removed in addition to the existing frames counted due to FIFO overflow.</p> <p>2. The IXF1010 has an extra counter RX/TXUCPkts that can be used.</p> <p>3. The IXF1010 has an extra counter RX/TXPktsToMaxOctets that can be used in addition to the RMON stats. This is required to accommodate the Jumbo packet frames requirement.</p>				

3.1.5.2 Conventions

The following conventions are used throughout the RMON MIB and its companion documents.

- **Good Packets:** Error-free packets that have a valid frame length. For example, on Ethernet, good packets are error-free packets that are between 64 octets long and 1518 octets long. They follow the form defined in IEEE 802.3, Section 3.2.
- **Bad Packets:** Packets that have proper framing and are therefore recognized as packets, but contain errors within the packet or have an invalid length. For example, on Ethernet, bad packets have a valid preamble and SFD, but have a bad CRC, or are either shorter than 64 octets or longer than 1518 octets.

3.1.5.3 Additional Statistics

The following lists additional IXF1010 registers that support features not documented in RMON.

- MAC (flow) control frames
- VLAN tagged frames
- Sequence errors
- Symbol errors
- CRC errors

These additional counters allow for additional differentiation over and above standard RMON probes.

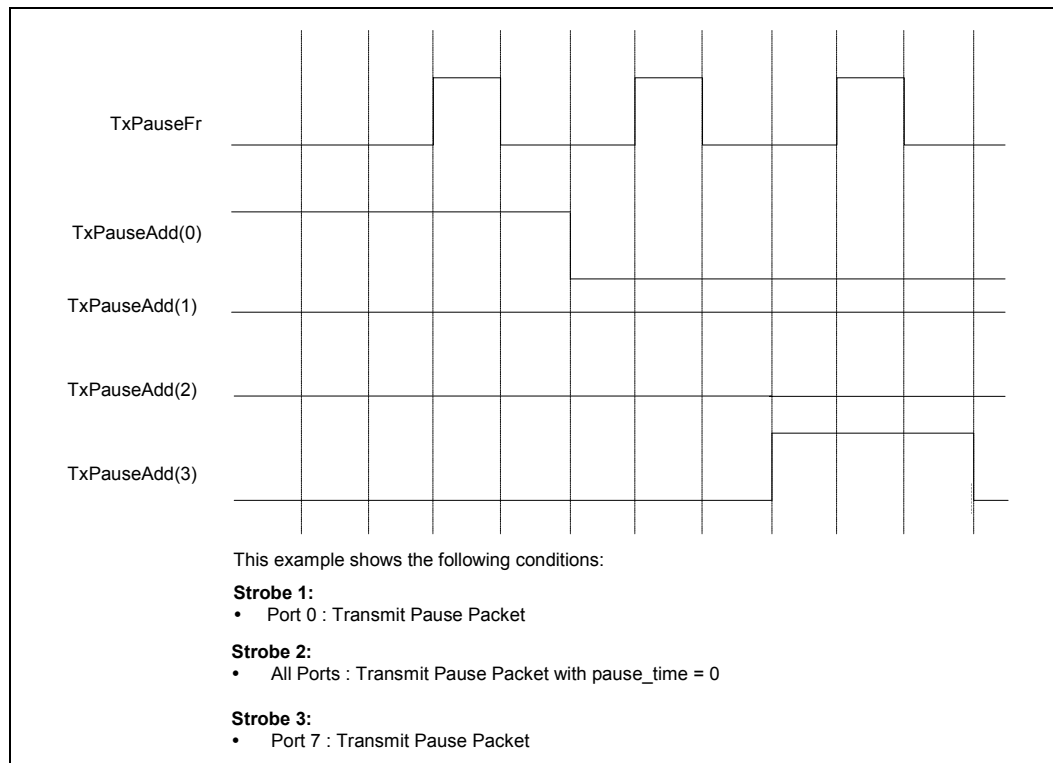
3.1.6 Transmit Pause Control Interface

The Transmit Pause Control interface is completely asynchronous. It consists of four address signals (TxPauseAdd[3:0]) and a strobe signal (TxPauseFr). The required address for this interface operation is placed on the TxPauseAdd[3:0] pins and the TxPauseFr is pulsed High and then returned Low. Refer to Figure 32, “Transmit Pause Control Interface Diagram” on page 76 and Table 29, “Transmit Pause Control Interface Parameters” on page 76. The valid decodes for the TxPauseAdd[3:0] signals are shown in Table 8. Figure 6 illustrates the transmit pause control interface.

Table 8. Valid Decodes for TxPauseAdd[3:0]

TxPauseAdd[3:0]	Operation of Tx Pause Interface
00h	Sends out a PAUSE frame on every port with a pause_time = ZERO (cancels all previous pause commands).
01h to 0Ah	Sends a PAUSE frame out on the selected port with pause_time = to the value programmed into that port's register set
0Bh to 0Eh	Reserved. These are invalid decodes and should not be used. The Tx Pause Interface will not operate under these conditions.
0Fh	Sends a PAUSE frame out on every port with pause_time = to the value programmed into that ports register set.

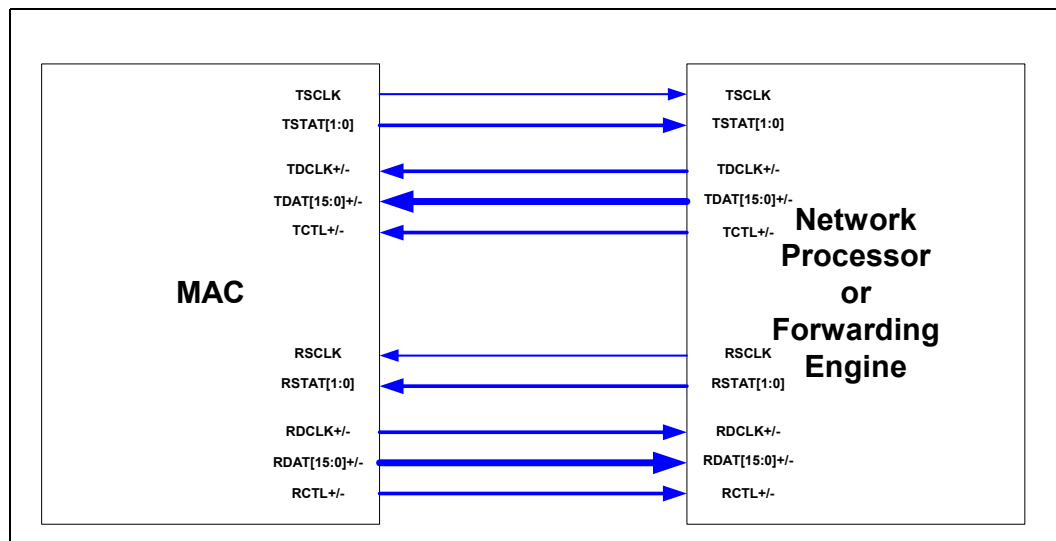
Figure 6. Transmit Pause Control Interface



3.2 System Packet Interface Level 4 Phase 2

The System Packet Interface Level 4 Phase 2 (SPI4-2) provides a high-speed connection to a network processor or an ASIC. The interface implemented on the IXF1010 operates at data rates up to 12.8 Gbps and supports up to ten 1 Gbps MAC channels. The data path is 16 lanes wide in each direction, with each lane operating from 640 Mbps up to 800 Mbps. Port addressing, start/end packet control, and error control codes are all transferred “in-band” on the data bus. In-band addressing supports up to 10 ports. Separate transmit and receive FIFO status lines are used for flow control. By keeping the FIFO status information out-of-band, the transmit and receive interfaces may be de-coupled to operate independently. Figure 7 provides an overview of the IXF1010 SPI4-2 interface.

Figure 7. IXF1010 SPI4-2 Interfacing with the Network Processor or Forwarding Engine



3.2.1 Data Path

Transfer of complete packets or shorter bursts is controlled by the programmed MaxBurst1 or MaxBurst2 in conjunction with the FIFO status bus. The maximum configured payload data transfer size must be a multiple of 16 bytes. Control words are inserted between burst transfers only. Once a transfer begins, data words are sent uninterrupted until an end-of-packet, or until a multiple of 16 bytes is reached as programmed in MaxBurst1 and MaxBurst2. The interval between the end of a given transfer and the next payload control word (marking the start of another transfer) consists of zero or more idle control words and/or training patterns.

Note: The system designer should be aware that the MAC Transfer Threshold Register must be set to a value which exceeds MaxBurst1 number of bytes. Otherwise, a TX FIFO under-run may result.

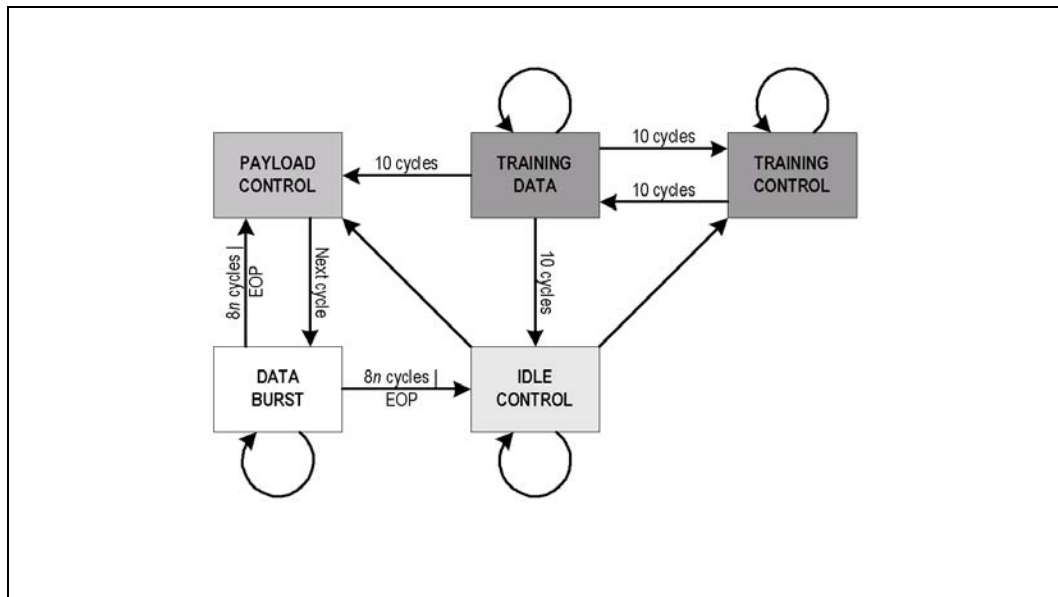
The minimum and maximum supported packet lengths are determined by the application. Because the IXF1010 is targeted at the Ethernet environment, the minimum frame size is 64 bytes and the maximum frame size is 1522 bytes for VLAN packets (1518 bytes for non-VLAN packets). For larger frames, adjust the Max Frame Size Register value, seen in Table 51 on page 94. For ease of implementation, successive start-of-packets must occur not less than eight cycles apart, where a cycle is one control or data word. The gap between shorter packets is filled with idle control words.

Note: Data packets with frame lengths less than 64 bytes should not be transferred to the IXF1010 unless packet padding is enabled. If this rule is disregarded, unwanted fragments may be generated on the network at the RGMII interface.

Figure 8 on page 35 shows cycle-by-cycle behavior of the data path for valid state transitions. The states correspond to the type of words transferred on the data path. Transitions from the “Data Burst” state (to “Payload Control” or “Idle Control”) are possible only on the integer multiples of eight cycles (corresponding to multiples of 16-byte segmentations) or upon end-of-packet. A data burst must immediately follow a payload control word on the next cycle. Arcs not annotated correspond to single cycles.

In the IXF1010, the RX FIFO Status channel operates in a “pessimistic mode.” It is termed as pessimistic because it has the longest latency and largest impact on usable bandwidth. However, as a DIP-2 check error is a rare event, there will be no ‘real world’ effect on bandwidth utilization and no possibility of data loss. For example, if there is a DIP-2 check error found, all previously granted credits are cancelled and the internal status for each channel is set to SATISFIED. Any current data burst in transmission is completed. No new credits are granted until a complete FIFO status cycle has been received and validated by a correct DIP-2 check. This is the only method of operation that can eliminate the possibility of an overrun in the link partner device.

Figure 8. Data Path State Diagram



3.2.1.1 Control Words

A common control word format is used in both the transmit and receive interfaces. Table 9 describes the fields in the control word. When inserted in the data path, the control word is aligned such that its MSB is sent on the MSB of the transmit or receive data lines. A payload control word that separates two adjacent burst transfers contains status information pertaining to the previous transfer and the following transfer. Table 10 provides a list of control-word definitions.

Table 9. Control Word Format

Bit Position	Label	Description
15	Type	Control Word Type. Set to either of the following values: 1: payload control word (payload transfer will immediately follow the control word). 0: idle or training control word.
14:13	EOPS	End-of-Packet (EOP) Status. Set to the following values according to the status of the immediately preceding payload transfer. 0 0: Not an EOP. 0 1: EOP Abort (application-specific error condition). 1 0: EOP Normal termination, 2 bytes valid. 1 1: EOP Normal termination, 1 byte valid. EOPS is valid in the first control word following a burst transfer. It is ignored and set to "0 0" otherwise.
12	SOP	Start-of-Packet. Set to 1 if the payload transfer immediately following the control word corresponds to the start of a packet. Set to 0 otherwise. Set to 0 in all idle and training control words.
11:4	ADR	Port Address. 8-bit port address of the payload data transfer immediately following the control word. None of the addresses are reserved (all are available for payload transfer). Set to all zeroes in all idle control words. Set to all ones in all training control words.
3:0	DIP-4	4-bit Diagonal Interleaved Parity. 4-bit odd parity computed over the current control word and the immediately preceding data words (if any) following the last control word.

Table 10. Control Word Definitions

	Bit [15:12]	Next Word Status	Prior Word Status	Meaning
0	0000	Idle	Continued	Idle, not EOP, training control word
1	0001	Reserved	Reserved	Reserved
2	0010	Idle	EOP w/abort	Idle, Abort last packet
3	0011	Reserved	Reserved	Reserved
4	0100	Idle	EOP w/ 2 bytes	Idle, EOP with 2 bytes valid
5	0101	Reserved	Reserved	Reserved
6	0110	Idle	EOP w/ 1 byte	Idle, EOP with 1byte valid
7	0111	Reserved	Reserved	Reserved
8	1000	Valid	None	Valid, no SOP, no EOP
9	1001	Valid/SOP	None	Valid, SOP, no EOP
A	1010	Valid	EOP w/abort	Valid, no SOP, abort
B	1011	Valid/SOP	EOP w/abort	Valid, SOP, abort
C	1100	Valid	EOP w/ 2 bytes	Valid, no SOP, EOP with 2 bytes valid

Table 10. Control Word Definitions (Continued)

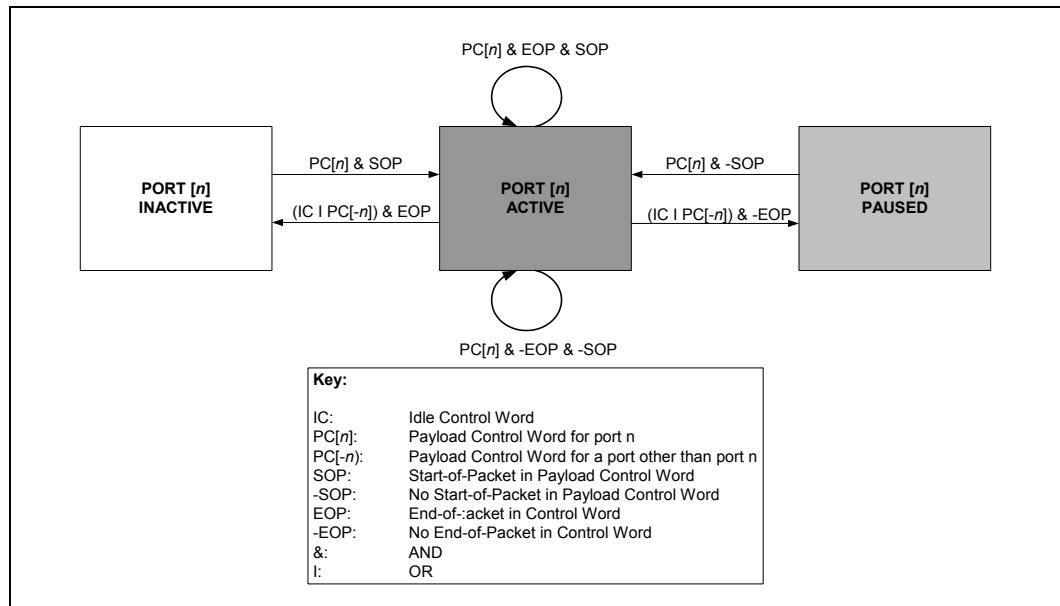
	Bit [15:12]	Next Word Status	Prior Word Status	Meaning
D	1101	Valid	EOP w/ 2 bytes	Valid, SOP, EOP with 2 bytes valid
E	1110	Valid	EOP w/ 1 byte	Valid, no SOP, EOP with 1byte valid
F	1111	Valid	EOP w/ 1 byte	Valid, SOP, EOP with 1byte valid

The SPI4-2 specification details all available Payload Control Words and should be used to reference the specific meaning of each. The IXF1010 supports all required functions per this specification. However, there are various specifics in the way certain Control Words affect the balance of the IXF1010 operation, such as how the device deals with EOP Aborts.

The SPI4-2 specification allows the EOP Abort Payload Control word, which signals that the data associated with a particular frame is errored and should be dropped, or errored and dropped by the far-end link partner. In the IXF1010, all TX SPI4-2 transfers that end with an EOP Abort code have the TX RGMII CRC corrupted. This is true regardless of the MAC configuration.

Figure 9 shows per-port state transitions at control-word boundaries. At any given time, a port may be active (sending data), paused (not sending data but pending the completion of an outstanding packet), or inactive (not sending data, no outstanding packet).

Figure 9. Per-Port State Diagram with Transitions at Control Words



3.2.1.2 DIP4

Figure 10 shows the range over which the Diagonal Interleaved Parity (DIP-4) parity bits are computed. A functional description of calculating the DIP-4 code is given as follows. Assume that the stream of 16-bit data words are arranged as shown in Figure 11, MSB at the left most column, time moving downward. (The first word received is at the top of the figure; the last word is at the bottom of the figure.) The parity bits are generated by summing diagonally (in the control word, the space occupied by the DIP-4 code (bits a, b, c, d) is set to all 1s during encoding). The first 16-bit result is split into two bytes, which are added to each other modulo-2 to produce an 8-bit result.

The 8-bit result is then divided into two 4-bit nibbles, which are added to each other modulo-2 to produce the final DIP-4 code. The procedure described applies to either parity generation on the Rx path or to check parity on the Tx path.

Figure 10. DIP-4 Calculation Boundaries

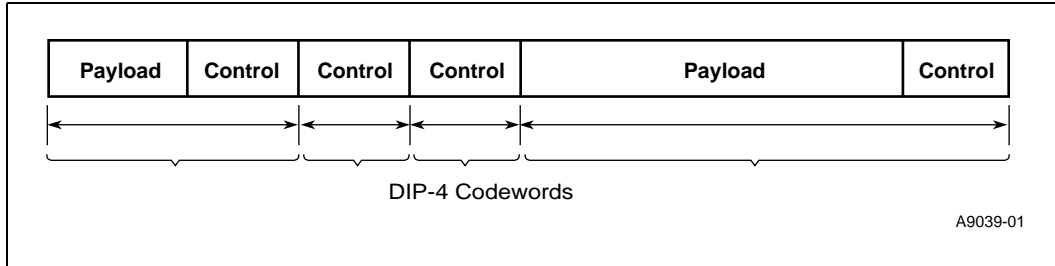
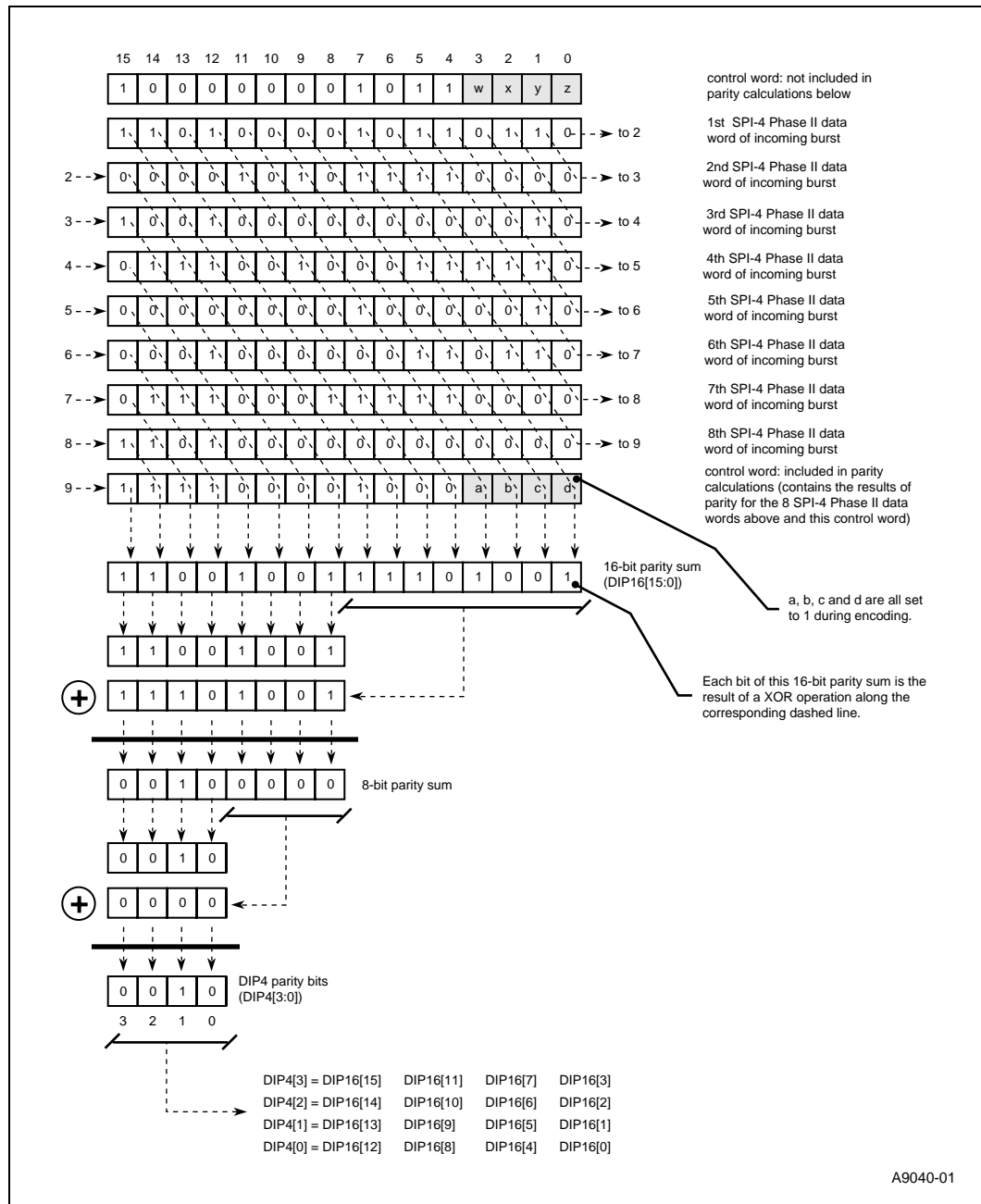


Figure 11. DIP-4 Calculation Algorithm



3.2.2 Start-Up Parameters

3.2.2.1 CALENDAR_LEN

CALENDAR_LEN specifies the length of each calendar sequence. As the IXF1010 is a 10-port device, CALENDAR_LEN is fixed at 10 for both TX and RX data paths.

3.2.2.2 CALENDAR_M

CALENDAR_M specifies the number of times the calendar port status sequence is repeated between the framing and DIP2 cycle of the calendar sequence.

In the IXF1010, the TX path CALENDAR_M is fixed at 1; thus, the port status for ports 0 - 9 will be transmitted only once between the framing and DIP2 cycle of the calendar sequence.

In the IXF1010, the RX path CALENDAR_M is configurable. The default value of expected RX CALENDAR_M is 1 as per the TX path. In [Table 95, “SPI4-2 RX Calendar Register \(Addr: 0x702\)” on page 137](#), bits 3 to 0 specify CAL_M, which is the number of times the calendar sequence will be repeated over the default value of 1.

The default value for CAL_M is 0, thus the default value of both Tx and RX CALENDAR_M parameters is 1.

3.2.2.3 DIP2_Thr

DIP2_Thr is a parameter specifying the number of consecutive correct DIP2s required by the RX SPI4-2 to validate a calendar sequence and therefore terminate sending training sequences. In [Table 95, “SPI4-2 RX Calendar Register \(Addr: 0x702\)” on page 137](#), bits 19 to 16 specify this parameter. The default value for DIP2_Thr is 1.

3.2.2.4 Loss_Of_Sync

Loss_of_Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and therefore restart training sequences. [Table 95, “SPI4-2 RX Calendar Register \(Addr: 0x702\)” on page 137](#), bits 11 to 8 specify this parameter. The default value for Loss_Of_Sync is three.

3.2.2.5 DATA_MAX_T

DATA_MAX_T is an RX SPI4-2 parameter specifying the interval between transmission of periodic training sequences. In [Table 94, “SPI4-2 RX Training Register \(Addr: 0x701\)” on page 136](#), bits 15 to 0 specify this parameter. The default value for DATA_MAX_T is 0x0000, which disables periodic training sequence transmission.

3.2.2.6 REP_T

REP_T is an RX SPI4-2 parameter specifying the number of repetitions of the training sequence to be scheduled every DATA_MAX_T interval. In [Table 94, “SPI4-2 RX Training Register \(Addr: 0x701\)” on page 136](#), bits 23 to 16 specify this parameter. The default value for REP_T is 0x00.

3.2.2.7 DIP4_UnLock

DIP4_UnLock is a TX SPI4-2 parameter specifying the number of consecutive incorrect DIP4 fields to be detected in order to declare loss of synchronization and drive TSTAT[1:0] bus with framing. In [Table 96, “SPI4-2 TX Synchronization Register \(Addr: 0x703\)” on page 138](#), bits 15 to 8 specify this parameter. The default value for DIP4_UnLock is 0x4.

3.2.2.8 DIP4_Lock

DIP4_Lock is a TX SPI4-2 parameter specifying the number of consecutive correct DIP4 fields to be detected in order to declare synchronization achieved and enable the calendar sequence. In [Table 96, “SPI4-2 TX Synchronization Register \(Addr: 0x703\)” on page 138](#), bits 7 to 0 specify this parameter. The default value for DIP4_Lock is 0x20.

3.2.2.9 MaxBurst1

MaxBurst1 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates “starving”. Bits 24 to 16 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst1 is 0x006, indicating a MaxBurst1 of 96 bytes [see [Section 93, “SPI4-2 RX Burst Size Register \(Addr: 0x700\)” on page 136](#)].

3.2.2.10 MaxBurst2

MaxBurst2 is an RX SPI4-2 parameter specifying the maximum number of 16 byte blocks that may be transmitted when the associated FIFO status indicates “hungry”. Bits 8 to 0 of the SPI4-2 RX Burst Size Register specify this parameter. The default value for MaxBurst2 is 0x002, indicating a MaxBurst2 of 32 bytes (see [Section 93, “SPI4-2 RX Burst Size Register \(Addr: 0x700\)” on page 136](#)).

3.2.3 Training Sequence for Dynamic Phase Alignment (Data Path De-skew)

3.2.3.1 Training at Start-up

The SPI4-2 Specification states that on power-up or after a reset, the training sequence (as defined in the SPI4-2 Specification) is sent indefinitely by the source side until it receives valid FIFO status on the FIFO bus. The specification also states that it is possible for the bus de-skew to be completed after one training sequence takes place. It is unlikely that the bus can be de-skewed in a single training sequence because of the presence of both random and deterministic jitter. The only way to account for the random element is to determine an average over repeated training sequences. Since the required number of repeats is dependent on several characteristics of the system in which the IXF1010 is being used, power on training (or training following loss of synchronization) will continue until synchronization is achieved and the calendar is provisioned. The length of power on training will not be a fixed number of repeats.

The number of training sequence repeats could be fairly large (16, 32, or 64). If this is necessary every time training is required, a significant use of interface bandwidth is needed just to train and de-skew the data path. This is only done at power-up or reset for an optimal starting point interface. After this, periodic training provides a better adjustment and a substantially lower bandwidth overhead.

3.2.3.2 Periodic Training

A scheduled training sequence is sent at least once every pre-configured bounded interval (DATA_MAX_T) on both the transmit and receive paths. These training sequences are used by the receiving end of each interface for de-skewing bit arrival times on the data and control lines. The sequence allows the receiving end to correct for relative skew difference of up to +/- 1 bit time. The

training sequence consists of one (1) idle control word followed by one or more repetitions of a 20-word training pattern consisting of 10 (repeated) training-control words followed by 10 (repeated) training-data words.

The initial idle control word removes dependencies of the DIP-4 in the training control words from preceding data words. Assuming a maximum of +/- bit time alignment jitter on each line, and a maximum of +/- bit time relative skew between lines, there are at least eight bit times when a receiver can detect a training control word prior to de-skew. The training data word is chosen to be orthogonal to the training control word. In the absence of bit errors in the training pattern, a receiver should be able successfully to de-skew the data and control lines with one training pattern. The sending side of the data path on both the transmit and receive interfaces must schedule the training sequence at least once every DATA_MAX_T cycles.

Note: DATA_MAX_T may be set to zero, disabling periodic training on the interface (refer to [Table 94, “SPI4-2 RX Training Register \(Addr: 0x701\)” on page 136](#)). This is done when a system shows very little drift during normal operation, and no fine-grain correction on an on-going basis is needed. This allows the maximum possible bandwidth for data transfer. The transmit and receive interface training sequences are scheduled independently.

3.2.3.3 Training in a Practical Implementation

The OIF Standard states that it should be possible to train and de-skew the data input in a single training cycle. However, from the research carried out and the variances in jitter and skew due to board layout and clock tolerance issues, some sort of averaging over several repeated training patterns is required to reliably determine the optimal point at which to capture the incoming data. This is true for both static alignment and dynamic phase alignment. Therefore, several training patterns are required for an average. The more training patterns, the more accurate the average.

The de-skew circuit in the IXF1010 uses dynamic phase alignment with a typical averaging requirement of 32 training patterns required to deliver a reliable result. During power-on training, an unlimited number of training cycles is sent by the data sourcing device. (The standard states that training must be sourced until a calendar has been provisioned.) In the IXF1010, the de-skew circuit waits until completion of its programmed average over the training patterns, ensuring that the required number of good DIP-4s is seen. Only then is a calendar provisioned.

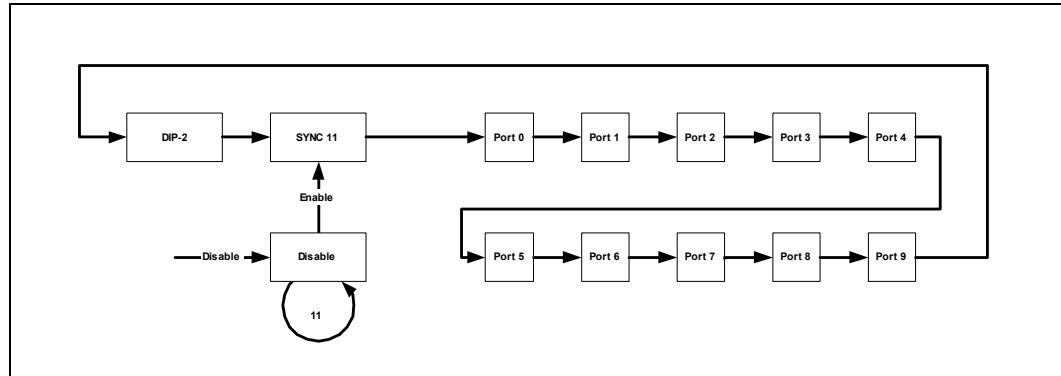
During periodic training, it is important to ensure that the training result is no less accurate than that already used for the initial decision during power-on training. Thus, a similar number of training cycles must be averaged over (32). This could make the overhead associated with periodic training large if it is required to be carried out too often. We therefore recommend that periodic training be scheduled infrequently (DATA_MAX_T = a large number) and that the number of repetitions of training be = $32(\alpha)$.

3.2.4 FIFO Status Channel

FIFO status information is sent periodically over the TSTAT link from the IXF1010 to the upper layer processor device, and over the RSTAT link from the upper layer processor to the IXF1010. The status channels operate independently.

[Figure 12](#) shows the operation of the FIFO status channel. The sending side of the FIFO status channel is initially in the DISABLE state and sends the “1 1” pattern repeatedly. When FIFO status transmission is enabled, there is a transition to the SYNC state and the “1 1” framing pattern is sent. FIFO status words are then sent according to the calendar sequence, repeating the sequence CALENDAR_M times, followed by the DIP-2 code.

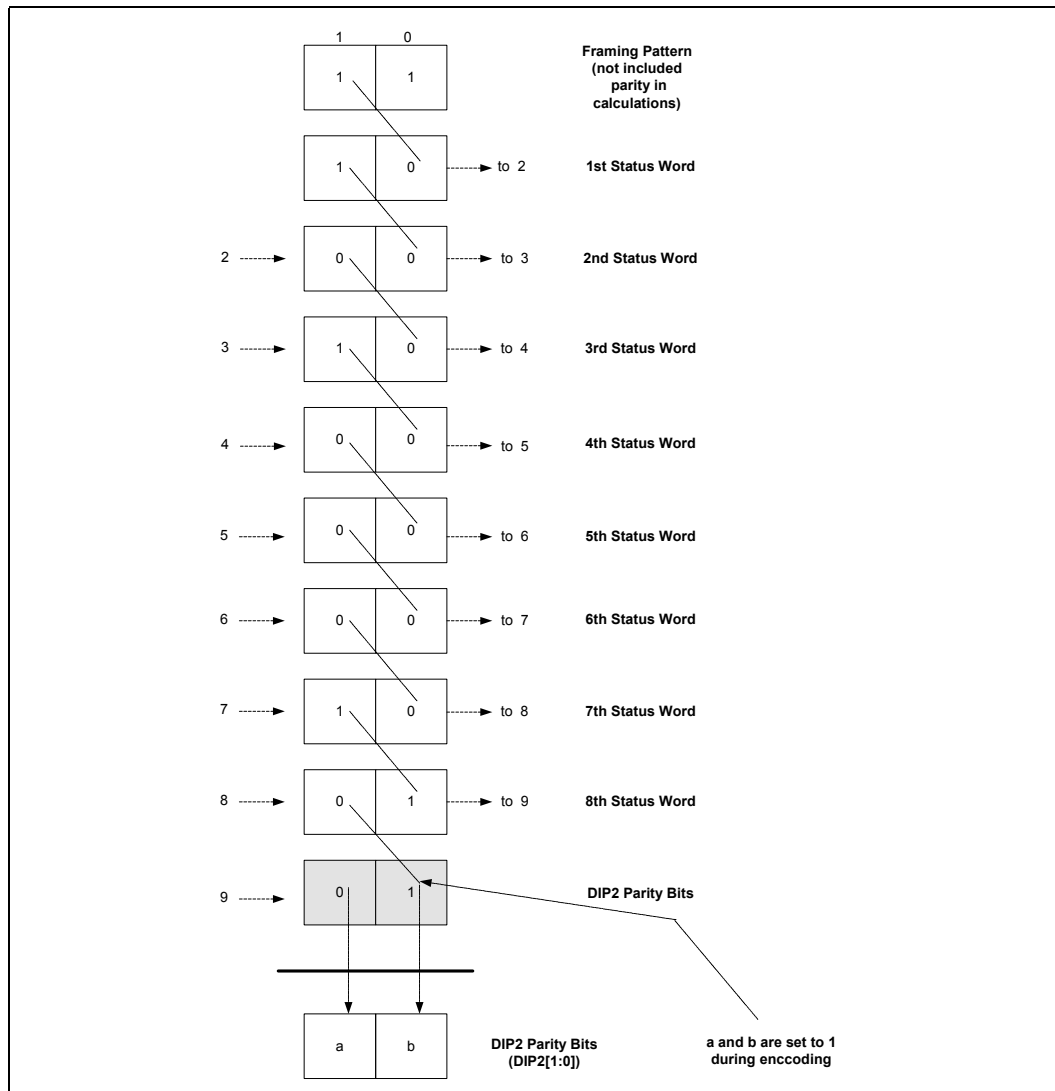
Figure 12. FIFO Status State Diagram



The FIFO status of each port is encoded in a 2-bit data structure, which is defined in [Table 11](#), “FIFO Status Format” on page 45. The most significant bit of each port status is sent over TSTAT[1]/RSTAT[1] and the least significant bit is sent over TSTAT[0]/RSTAT[0]. The “1 1” pattern is reserved for In-band framing, which must be sent once prior to the start of the FIFO status sequence.

Immediately before the “1 1” framing pattern, a DIP-2 odd parity checksum is sent at the end of each complete sequence. The DIP-2 code is computed diagonally over TSTAT[1]/RSTAT[1] and TSTAT[0]/RSTAT[0] for all preceding FIFO status indications sent after the last “1 1” framing pattern, as shown in [Figure 13](#) on page 44. The first word is at the top of the figure and the last word is at the bottom. The parity bits are computed by summing diagonally. Bits a and b in line 9 correspond to the space occupied by the DIP-2 parity bits and are set to 1 during encoding. The “1 1” framing pattern is not included in the parity calculation. The procedure described applies to either parity generation on the egress path or to check parity on the ingress path.

Figure 13. Example of DIP-2 Encoding



When the parity bits mimic the “1 1” pattern, the receiving end still frames successfully by syncing onto the last cycle in a repeated “1 1” pattern, and by making use of the configured sequence length when searching for the framing pattern.

To permit more efficient FIFO utilization, the MaxBurst1 and MaxBurst2 credits are granted and consumed in increments of 16-byte blocks. For any given port, these credits correspond to the most recently received FIFO status. They are not cumulative and supersede previously granted credits for the given port. A burst transfer shorter than 16 bytes (for example, an end-of-packet fragment) consumes an entire 16-byte credit.

A continuous stream of repeated “1 1” framing patterns indicates a disabled status link. For example, it may be sent to indicate that the data path de-skew is not yet completed or confirmed. When a repeated “1 1” pattern is detected, all outstanding credits are cancelled and set to zero.

Table 11. FIFO Status Format

MSB	LSB	Description
1	1	Reserved for framing or to indicate a disabled status link.
1	0	SATISFIED: Indicates that the corresponding port's FIFO is almost full. When SATISFIED is received, only transfers using the remaining previously granted 16-byte blocks (if any) may be sent to the corresponding port until the next status update. No additional transfers to that port are permitted while SATISFIED is indicated.
0	1	HUNGRY: When HUNGRY is received, transfers for up to MaxBurst2 16-byte blocks, or the remainder of what was previously granted (whatever is greater), may be sent to the corresponding port until the next status update.
0	0	STARVING: Indicates that buffer underflow is imminent in the corresponding PHY port. When STARVING is received, transfers for up to MaxBurst1 16-byte blocks may be sent to the corresponding port until the next status update

The indicated FIFO status is based on the latest available information. A STARVING indication provides additional feedback information, so that transfers are scheduled accordingly. Applications that do not distinguish between HUNGRY and STARVING may only examine the most significant FIFO status bit.

Note: If a port is disabled on the IXF1010, FIFO status for the port is set to SATISFIED to avoid the possibility of any data being sent to it by the controlling device. This applies to the IXF1010 transmit path.

Upon reset, the FIFOs in the data path receiver are emptied, and any outstanding credits are cleared in the data path transmitter. After reset, and before active traffic is generated, the data transmitter sends continuous training patterns. Transmission of the training patterns continues until valid information is received on the FIFO Status Channel. The receiver ignores all incoming data until it has observed the training pattern and acquired synchronization with the data. Synchronization may be declared after a provisional number of consecutive correct DIP-4 code words is seen. Loss of synchronization may be reported after a provisional number of consecutive DIP-4 code words is detected. [For details, see [Table 96, “SPI4-2 TX Synchronization Register \(Addr: 0x703\)” on page 138.](#)]

As stated above, the DIP-4 thresholds are programmable. However, there is a potential issue where it is possible that a given link showing DIP-4 errors may never lose synchronization and re-train to fix the issue. This would mean an on-going and potentially significant loss of data on the link affecting all ports transferring data at that time.

This issue may be seen in two instances:

- During training (most likely periodic training)
- During data transfers where each of the data transfers (MaxBurst1 or MaxBurst2) are separated by more than one idle control word

The mechanism for both issues is the same because data will not change during a repeated period of the same control word being transmitted on the link. If there have been some consecutive DIP-4 errors, they will be incremented towards the Loss-of-Sync threshold. This is most likely to occur from a path requiring de-skew. If either a stream of idles or training control words follow the burst and the DIP-4 associated with each of the words is checked, only the first one and the last one will be seen as invalid. Any other control words in the middle will be seen as having a valid DIP-4 and will reset the Loss-of-Sync threshold counter back to zero.

In order to avoid this, the IXF1010 has altered the way in which the check is done for idle control words and training control words. We now only validate the first occurrence of the DIP-4 in both training control words and idle control words for correctness. We do still check each of the words but only use the first occurrence to clear the DIP-4 error counter. Any DIP-4 error in any of these words is still counted towards the Loss-of-Sync threshold counter. It is now impossible to mask the DIP-4 error on our interface.

3.2.5 DC Parameters

For DC parameters on the SPI4-2 interface, please refer to [Figure 21, “2.5 V LVTTTL and CMOS I/O Electrical Characteristics”](#) on page 67 and [Figure 22, “LVDS I/O Electrical Characteristics”](#) on page 67.

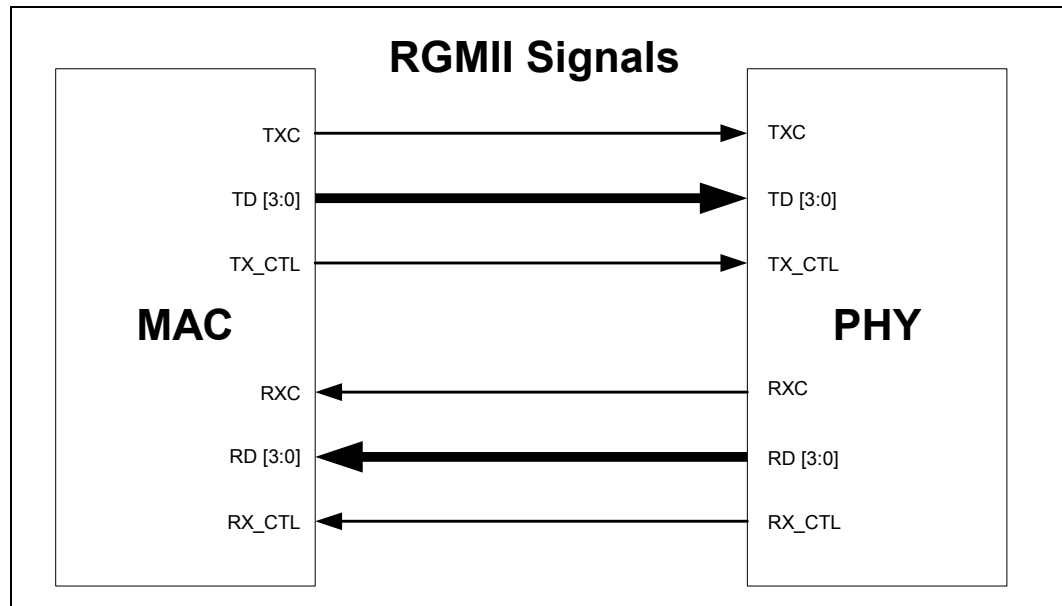
3.3 Reduced Gigabit Media Independent Interface (RGMI)

IXF1010 supports Reduced Gigabit Media Independent Interface (RGMI) standards as defined in the Hewlett-Packard RGMI Version 1.2a specification. The RGMI is an alternative to the IEEE 802.3u MII, the IEEE 802.3z GMII, and the Ten-Bit Interface (TBI).

3.3.1 Purpose

The RGMI reduces the number of pins required to interconnect the MAC and the PHY, from a maximum of 28 pins (TBI) to 12 pins, in a cost-effective and technology-independent manner. The data paths and all associated control signals are reduced, control signals are multiplexed together, and both edges of the clock are used. For Gigabit operation, the clocks operate at 125 MHz, and for 100 Mbps operation, the clocks operate at 25 MHz. For 100 Mbps operation, the RGMI interface data path reverts to standard MII operational mode, as defined in IEEE 802.3, Clause 22. The multiplexed control signals operate as defined in RGMI Specification 1.2a.

Figure 14. IXF1010 System Diagram



3.3.2 1000 Mbps Operation

3.3.2.1 Multiplexing of Data and Control

Multiplexing of data and control information is achieved by utilizing both edges of the reference clocks and sending the lower 4 bits on the rising edge and the upper 4 bits on the falling edge. Control signals are multiplexed into a single clock cycle using the same technique (see Figure 25, “RGMII 1000 Mbps Multiplexing and Timing Diagram” on page 69).

3.3.2.2 Timing Specifics

This interface requires that the clock and data are generated simultaneously by the source of the signals, thus skew between the clock and data is critical for proper operation. This approach is used to provide tighter control of skew. Table 23, “RGMII 1000 Mbps Timing Specifics” on page 69 provides these timing specifics.

3.3.3 100 Mbps Operation

3.3.3.1 Multiplexing of Data and Control

The control signals are multiplexed, as in the 1000 Mbps operation, by using both edges of the clock. The data signals, however, do not need to be multiplexed. The data signals are driven off the rising edge of the clock. The clock rate is reduced to 25 MHz for 100 Mbps operation. The MAC generates the Transmit Reference Clock (TXC) and the Receive Reference Clock (RXC) is generated by the PHY. During packet reception, the RXC is stretched on either the positive or negative pulse to accommodate transition from the free-running clock to a data-synchronous clock domain (see Figure 26, “RGMII 100 Mbps Multiplexing and Timing Diagram” on page 71). When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitching of the clocks is allowed during speed transitions.

3.3.3.2 Timing Specifics

Skew between the clock and data is critical to proper operation, so timing for this interface allows simultaneous generation of the clock and data by the source. This approach is used to provide tighter control of skew. Table 25, “RGMII 100 Mbps Timing Specifics” on page 71 provides these timing specifics.

3.3.4 TXERR and RXERR Coding

To reduce interface power, the transmit error condition (TXERR) and the receive error condition (RXERR) are encoded on the RGMII interface to minimize transitions during normal network operation (refer to Table 13 on page 48 for the encoding method). Table 12 provides signal definitions for RGMII. Figure 15 shows the transitions for frames with and without errors.

Table 12. RGMII Signal Definitions

IXF1010 Symbol	RGMII Standard Symbol	Source	Description
TXC	TXC	MAC	Depending on speed, the transmit reference clock is 125 MHz or 25 MHz +/- 100 ppm
TD[3:0] _n	TD<3:0>	MAC	Contains Register bits 3:0 on the rising edge of TXC and may contain Register bits 7:4 on the falling edge of TXC, depending on speed
TX_CTL	TX_CTL	MAC	TXEN on the rising edge of TXC TXEN xor TXERR on the falling edge of TXC
RXC	RXC	PHY	Continuous reference clock is 125 MHz or 25 MHz +/- 100 ppm
RD[3:0] _n	RD<3:0>	PHY	Contains Register bits 3:0 on the rising edge of RXC and may contain Register bits 7:4 on the falling edge of RXC, depending on speed
RX_CTL	RX_CTL	PHY	RX_CTL is on the rising edge of RXC RX_CTL xor RXERR is the falling edge of RXC

Note: The value of RGMII_TXER and RGMII_TXEN are valid at the rising edge of the clock while TXERR is presented on the falling edge of the clock. RXERR coding behaves in the same way.

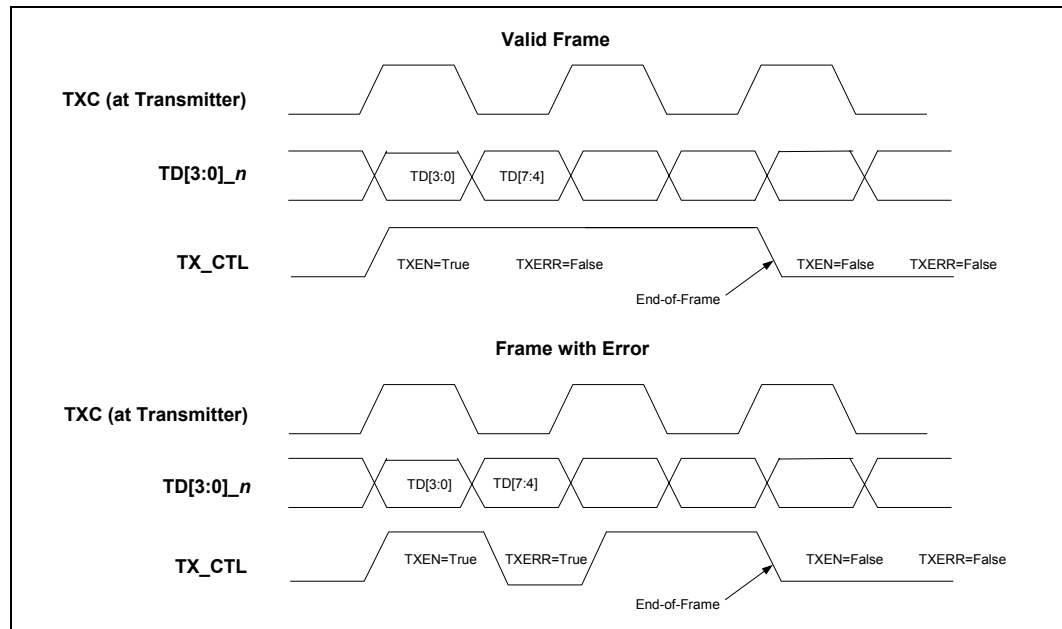
$TXERR \leq RGMII_TXER (XOR) RGMII_TXEN$

$RXERR \leq RGMII_RXER (XOR) RGMII_RXDV$

Table 13. TXERR and RXERR Coding Example

Condition	Description	
Receiving valid frame, no errors	RX_CTL = true Logic High on rising edge of RXC	RXERR = false Logic High on the falling edge of RXC
Receiving valid frame, with errors	RX_CTL = true Logic High on rising edge of RXC	RXERR = true Logic Low on the falling edge of RXC
Receiving invalid frame (or no frame)	RX_CTL = false Logic Low on rising edge of RXC	RXERR = false Logic Low on the falling edge of RXC
NOTE: Refer to Figure 15 for TX_CTL Behavior.		

Figure 15. TX_CTL Behavior Diagram



3.3.4.1 In-Band Status

Carrier Sense (CRS) is generated by the PHY when a packet is received from the network interface. CRS is indicated when:

- RX_CTL is true
- RX_CTL is false, RXERR is true, and a value of 0xFF exists on the RD[7:0] bits simultaneously
- RX_CTL is false, RXERR is true, and a value of 0x0F exists on RD[7:0] bits simultaneously
- RX_CTL is false, RXERR is true, and a value of 0x1F exists on RD[7:0] bits simultaneously
- RX_CTL is false, RXERR is true, and a value of 0x0E exists on RD[7:0] bits simultaneously

3.3.5 Electrical Characteristics

The RGMII signals (including MDIO/MDC) are based on 2.5V CMOS interface voltages, as defined by JEDEC EIA/JESD8-5 (see Table 24).

3.4 MDIO Control and Interface

3.4.1 MDIO Interface

IXF1010 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows the IXF1010 to monitor and control each of the PHY devices that are connected to the device's 10 ports.

3.4.2 General Description

The MDIO Master Interface block is implemented once in the IXF1010. The MDIO Interface block contains the logic through which the user accesses the registers in PHY devices connected to the MDIO/MDC interface, controlled by each port.

The MDIO Master Interface block supports the management frame format, specified by IEEE 802.3, Clause 22, Section 2.4.5. This block also supports single MDI access via the CPU interface and an autoscan mode. Autoscan allows the MDIO master to read all 32 registers of the per-port PHYs and store the contents in the IXF1010. This ability provides an external CPU-ready access to the PHY register contents via a single CPU Read without the latency of waiting on the low-speed serial MDIO data bus for each register access.

3.4.3 MDIO Register Descriptions

Table 41, “MDIO Block Register Map” on page 90 provides an overview of the MDIO Register set and Table 89, “MDI Single Command Register (Addr: 0x680)” on page 134 through Table 92, “MDI Control Register (Addr: 0x683)” on page 135 provide a register-by-register bit definition of the MDIO Register set.

3.4.4 Clear When Done

The MDI Command Register bit, in the MDI Single Command and Address Register, clears upon command completion and is set by the user to start the requested single MDIO Read or Write operation. This bit is cleared automatically upon operation completion.

3.4.5 MDC Generation

The MDC clock is used for the MDIO/MDC interface. The frequency of the MDC clock is selectable by setting the MDC speed bit in the MDI Control Register (see Table 92, “MDI Control Register (Addr: 0x683)” on page 135).

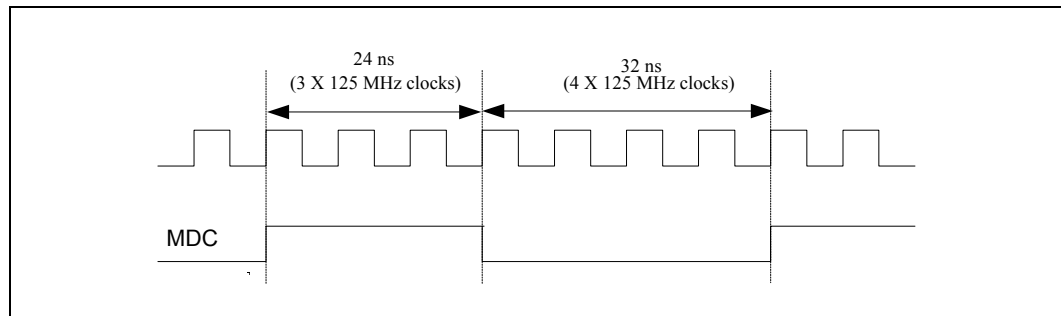
3.4.5.1 MDC High-Frequency Operation

The high-frequency MDC is 18 MHz, derived from the 125 MHz system clock by dividing the frequency by 7.

The clock duty cycle is as follows:

- MDC High duration: $3 \times (1/125 \text{ MHz}) = 3 \times 8 \text{ ns} = 24 \text{ ns}$
- MDC Low duration: $4 \times (1/125 \text{ MHz}) = 4 \times 8 \text{ ns} = 32 \text{ ns}$
- MDC runs continuously after reset

Figure 16. High-Frequency MDC Timing Diagram



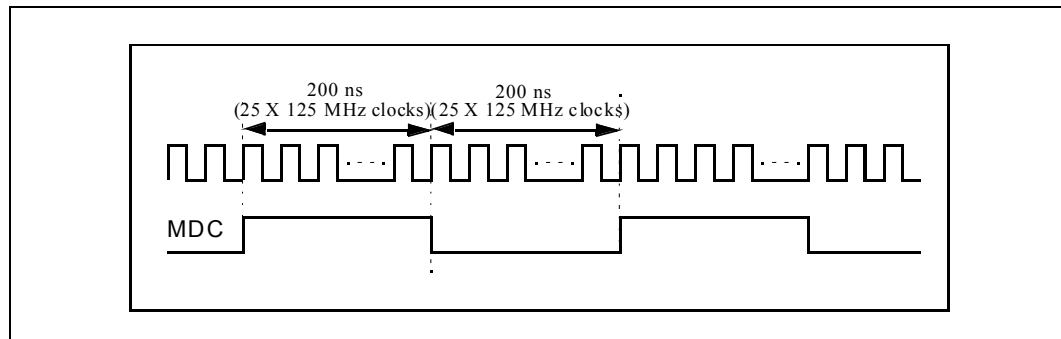
3.4.5.2 MDC Low-Frequency Operation

The low-frequency MDC is 2.5 MHz, which is derived from the 125 MHz system clock by dividing the frequency by 50.

The duty cycle is as follows:

- MDC High duration: $25 \times (1/125 \text{ MHz}) = 25 \times 8 \text{ ns} = 200 \text{ ns}$
- MDC Low duration: $25 \times (1/125 \text{ MHz}) = 25 \times 8 \text{ ns} = 200 \text{ ns}$
- MDC runs continuously after reset

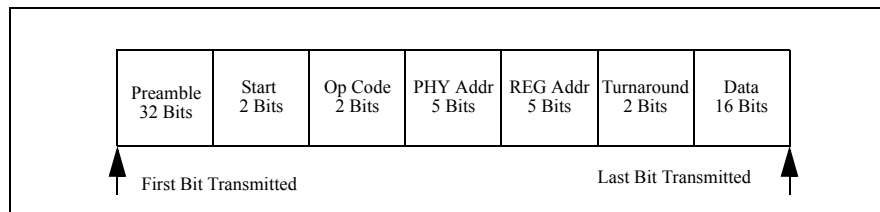
Figure 17. Low-Frequency MDC Timing Diagram



3.4.6 MDIO Management Frames

The MDIO Management interface serializes the external register access information into the format specified by IEEE 802.3, Clause 22, Section 2.4.5.

Figure 18. MDIO Management Frame Structure



3.4.7 Single MDI Command Operation

The Management Data interface is accessed through the MDI Single Command and Address Register and the MDI Single Read and Write Data Register. A single management frame is sent by setting bit 20 to Logic 1 in the MDI Single Command and Address Register, and is automatically cleared when the frame is completed.

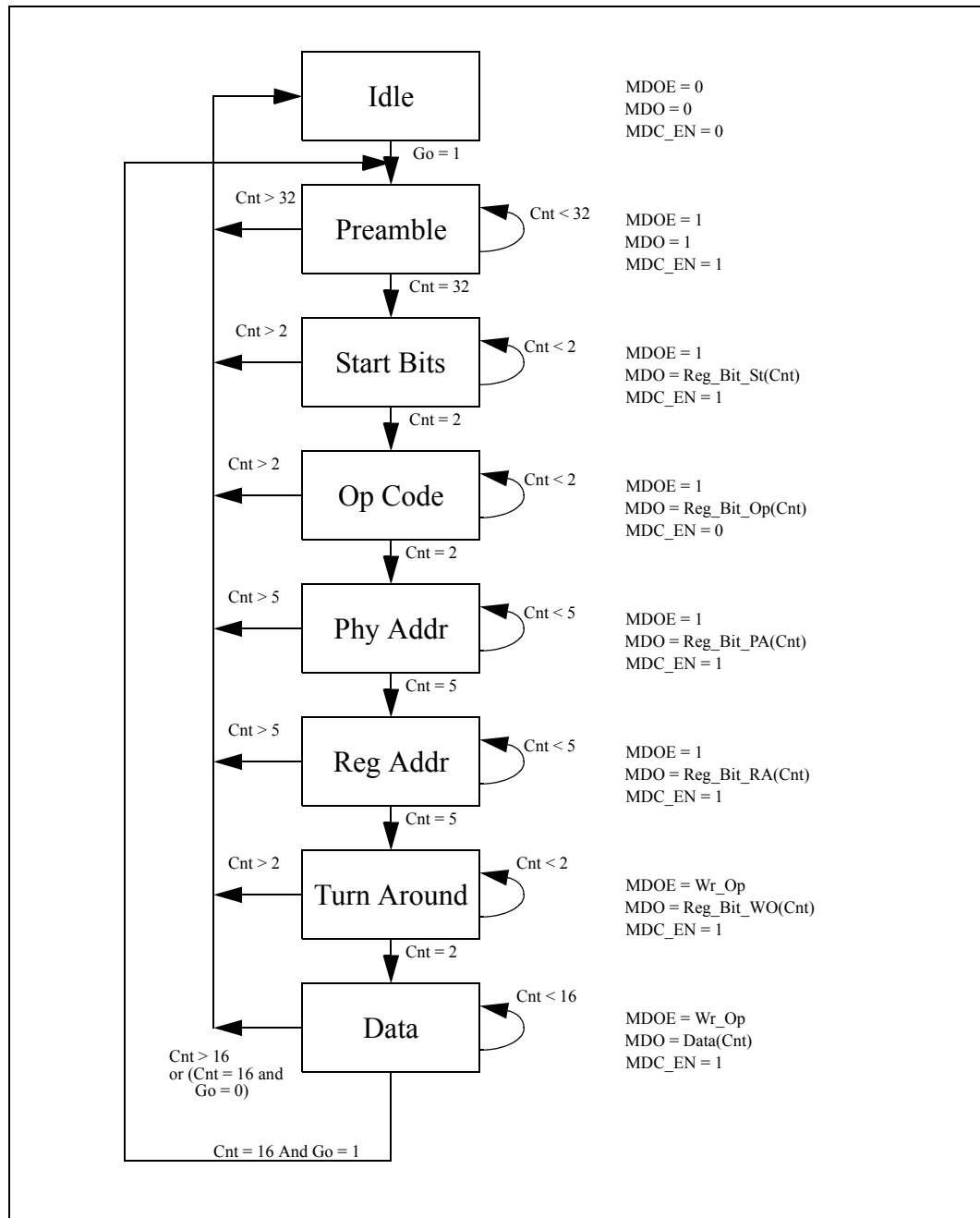
Write data is first set up in MDI Single Read and Write Data Register bits 15:0 for Write operation. The MDI Single Command and Address Register is initialized with the appropriate control information (start, op code, etc.) and MDI Single Command and Address Register bit 20 is set to Logic 1. Bit 20 is reset to Logic 0 when the frame is complete.

Read operation steps are identical except in MDI Single Read and Write Data Register bits 15:0, where the data is ignored. Data received from the MDIO is read by the CPU interface from bits 31:16.

3.4.8 MDI State Machine

The MDI State Machine sequences the information sent to it by the MDIO control registers and keeps track of the current sequence bit count, enabling or disabling the MDIO driver output (see [Figure 19, “MDI State Diagram” on page 53](#)).

Figure 19. MDI State Diagram



3.4.9 Autoscan Operation

The Autoscan PHY Address Enable Register (Table 91, “Autoscan PHY Address Enable Register (Addr: 0x682)” on page 134) is used to determine which PHY addresses are used for each of the ten IXF1010 ports. The Autoscan PHY Address Enable Register is 32 bits wide, which allows for PHY addresses 0 - 31 to be used. The bits set in this register correspond to consecutive MAC ports. The Least Significant Bit (LSB) set in the Address Enable Register is port 0 for the IXF1010; the next significant bit set is assumed to be port 1, and this continues on to port 9. If more than 10 bits are set, the bits beyond the tenth bit are ignored. If less than 10 bits are set, the round-robin process reads only the PHY registers for the reduced MAC port count.

The autoscan function stores the 32 registers in each external PHY (up to 10) internally in the IXF1010. Autoscan is enabled by setting bit 1 of the MDI Control Register (Table 92, “MDI Control Register (Addr: 0x683)” on page 135). When enabled, autoscan runs continuously, reading each PHY register. When a PHY register access is instigated through the MDIO interface, the current autoscan register Read is completed before the MDIO register access starts. Upon completion of the MDIO access, the autoscan functionality restarts from the last autoscan register access prior to the MDIO register access.

For example, the IXF1010 is connected to PHYs addressed 20-29, with the IXF1010 port 0 connected to PHY address 20, and Port 1 connected to PHY address 21. This is continued to port 9, which is connected to PHY address 29. To enable autoscan for all 10 ports on the IXF1010, bits 29:20 in the Autoscan PHY Address Enable Register must be set to 1 and all other bits set to a 0. This enables the autoscan to read PHY addresses 20-29, which allows all 32 registers of each PHY to be stored in the connected IXF1010 ports (refer to Table 37, “PHY Autoscan Register Map” on page 86).

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3.5 LED Interface

3.5.1 Introduction

The IXF1010 uses a serial interface consisting of three signals to provide LED data to some form of external driver. This interface provides the data for 30 separate direct drive LEDs and allows three LEDs per MAC port.

There are two modes of operation, each with its own separate LED decode mapping. Modes of operation and LEDs are detailed in “Modes of Operation”.

3.5.2 Modes of Operation

Mode selection is accomplished by using the LED_SEL_MODE bit. This bit is globally selected and controls the operation of all ports (see Table 74, “LED Control Register (Addr: 0x509)” on page 114).

There are two modes of operation:

Mode 0: (LED_SEL_MODE = 0 [Default]): This mode selects operations compatible with the SGS Thompson M5450 Led Display Driver Device. This device converts the serial data stream, output by the IXF1010, into 30 direct-drive LED outputs.

Mode 1: (LED_SEL_MODE = 1): This mode is used with standard TTL (74LS595) or HCMOS (74HC595) octal shift registers with latches, providing the most general and cost-effective implementation of the serial data stream conversion.

In addition to these physical modes of operation, there are two types of specific LED data decodes available. This option is a global selection and controls the operation of all ports (see [Table 74](#), “LED Control Register (Addr: 0x509)” on page 114).

3.5.3 LED Interface Signal Description

The IXF1010 LED interface consists of three output signal pins that are 2.5 V CMOS level pads. [Table 14](#) provides LED signal names, pin numbers and descriptions.

Table 14. LED Pin Descriptions

Pin Name	Pin #	Pin Description
LED_CLK	A20	LED_CLK: This signal is an output that provides a continuous clock synchronous to the serial data stream output on the LED_DATA pin. This clock has a maximum speed of 0.5 MHz. The behavior of this signal remains constant in all modes of operation.
LED_DATA	A19	LED_DATA: This signal provides the data, in various formats, as a serial bit stream. The data must be valid on the rising edge of the LED_CLK signal. In Mode 0, the data presented on this pin is TRUE (Logic 1 = High). In Mode 1, the data presented on this pin is INVERTED (Logic 1 = Low).
LED_LATCH	K18	LED_LATCH: This is an output pin and the signal is used only in Mode 1 as the Latch enable for the shift register chain. This signal is not used in Mode 0, and should be left unconnected.

3.5.4 Mode 0: Detailed Operation

Note: Please refer to the SGS Thompson M5450 datasheet for device-operation information.

The operation of the LED Interface in Mode 0 is based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. [Figure 20 on page 55](#) shows the basic timing relationship and relative positioning in the data stream of each bit.

[Figure 20](#) shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the M5450 device. The actual data shown in [Figure 20](#) consists of a chain of 36 bits only, 30 of which are valid LED DATA. The 36-bit data chain is built up as follows:

Figure 20. Mode 0 Timing Diagram

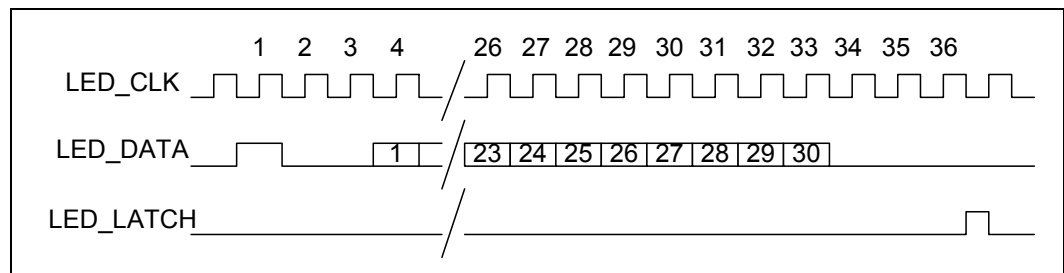


Table 15. Mode 0 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit is used to synchronize the M5450 device to expect 35 bits of data to follow.
2:3	PAD BITS	These bits are used only as fillers in the data stream to extend the length from the actual 30 bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.
4:33	LED DATA 1-30	These bits are the actual data transmitted to the M5450 device. The decode for each individual bit in each mode is defined in Table 14 on page 55 . The data is TRUE. Logic 1(LED ON) = High
34:36	PAD BITS	These bits are used as fillers in the data stream to extend the length from the actual 30-bit LED DATA to the required 36-bit frame length. These bits should always be a Logic 0.

When implemented on a board with the M5450 device, the LED DATA bit 1 appears on output bit 3 of the M5450 and the LED DATA bit 2 appears on output bit 4, etc. This means that output bits 1, 2, 3, 34, and 35 will never have valid data and should not be used.

3.5.5 Mode 1: Detailed Operation

Note: Please refer to manufacturers' 74LS/HC595 datasheet for information on device operation.

The operation of the LED Interface in Mode 1 is again based on a 36-bit counter loop. The data for each LED is placed in turn on the serial data line and clocked out by the LED_CLK. [Figure 21 on page 57](#) shows the basic timing relationship and relative positioning in the data stream of each bit.

[Figure 21](#) shows the 36 clocks that are output on the LED_CLK pin. The data changes on the falling edge of the clock and is valid for almost the entire clock cycle. This ensures that the data is valid during the rising edge of the LED_CLK, which is used to clock the data into the Shift Register chain devices.

The LED_LATCH signal is required in Mode 1, and is used to latch the data shifted into the shift register chain into the output latches of the 74HC595 device. As seen in [Figure 21](#), the LED_LATCH signal is active High during the Low period on the 36th LED_CLK cycle. This avoids any possibility of trying to latch data as it is shifting through the register.

When this operation mode is implemented on a board with a shift register chain containing three 74HC595 devices, the LED DATA bit 1 is output on Shift Register bit 1, and so on up the chain. Only Shift Register bits 31 and 32 do not contain valid data. The actual data shown in [Figure 21](#) consists of a 36-bit chain, of which 30 bits are valid LED DATA. The 36-bit data chain is built up as follows:

Note: The LED_DATA signal is now inverted from the state in Mode 0.

Figure 21. Mode 1 Timing Diagram

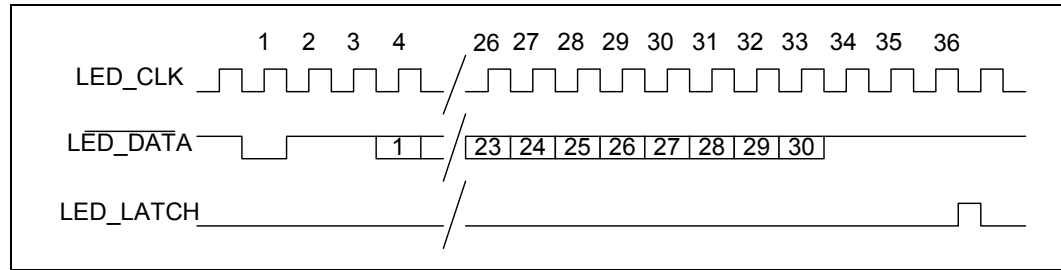


Table 16. Mode 1 Clock Cycle to Data Bit Relationship

LED_CLK CYCLE	LED_DATA NAME	LED_DATA DESCRIPTION
1	START BIT	This bit has no meaning in Mode 1 operation and is shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
2:3	PAD BITS	These bits have no meaning in Mode 1 operation and are shifted out of the 32-stage shift register chain before the LED_LATCH signal is asserted.
4:33	LED DATA 1-30	These bits are the actual data to be transmitted to the 32-stage shift register chain. The decode for each bit in each mode is defined in Table 16 on page 57 . The data is INVERTED. Logic 1 (LED ON) = Low.
34:36	PAD BITS	These bits have no meaning in Mode 1 operation and are latched into positions 31 and 32 in the shift register chain. These bits are not considered as valid data and should be ignored. They should always be a Logic 0 = High.

3.5.6 Power-On, Reset, and Initialization

The LED interface is disabled at power-on or reset. The system software controller must enable the LED interface. The internal state machines and output pins are held in reset until the full IXF1010 device configuration is completed. This is done by setting the LED_ENABLE bit to a logic 1 (see [Table 74, “LED Control Register \(Addr: 0x509\)” on page 114](#)). The power-on default for this bit is Logic 0.

3.5.7 LED Data Decodes

[Table 17](#) shows the data decode of the data for the IXF1010.

Table 17. LED DATA Decodes

LED_DATA#	MACPORT #	IXF1010 Designation
1	0	Link LED - Amber
2		Link LED - Green
3		Activity LED - Green
4	1	Link LED - Amber
5		Link LED - Green
6		Activity LED - Green
7	2	Link LED - Amber
8		Link LED - Green
9		Activity LED - Green
10	3	Link LED - Amber
11		Link LED - Green
12		Activity LED - Green
13	4	Link LED - Amber
14		Link LED - Green
15		Activity LED - Green
16	5	Link LED - Amber
17		Link LED - Green
18		Activity LED - Green
19	6	Link LED - Amber
20		Link LED - Green
21		Activity LED - Green
22	7	Link LED - Amber
23		Link LED - Green
24		Activity LED - Green
25	8	Link LED - Amber
26		Link LED - Green
27		Activity LED - Green
28	9	Link LED - Amber
29		Link LED - Green
30		Activity LED - Green

3.5.7.1 LED Signaling Behavior

Operation in each mode for the decoded LED data in [Table 17](#) is detailed in [Table 18](#).

3.5.7.1.1 IXF1010 LED Behavior

Table 18. IXF1010 LED Behavior

Type	Status	Description
Link LED - Amber	Off	Port does not have an RGMII RXERR or remote fault
	On	Port does have an RGMII RXERR condition detected
	Blinking	Port has a remote fault
Link LED - Green	Off	Port does not have link
	On	Port is enabled and has link
Activity LED - Green	Off	Port is not transmitting and receiving
	Blinking	Port is transmitting and receiving

3.6 CPU Interface

3.6.1 General Description

The CPU Interface block provides access to registers and statistics in the IXF1010. The interface is asynchronous externally and operates within the 125 MHz clock domain internally. The interface provides access to the following registers:

- MAC Control
- MAC RX Statistics
- MAC TX Statistics
- PHY Auto Scan
- Global Status and Configuration
- RX Block
- TX Block
- MDIO Block
- SPI4-2 Block

3.6.2 Functional Description

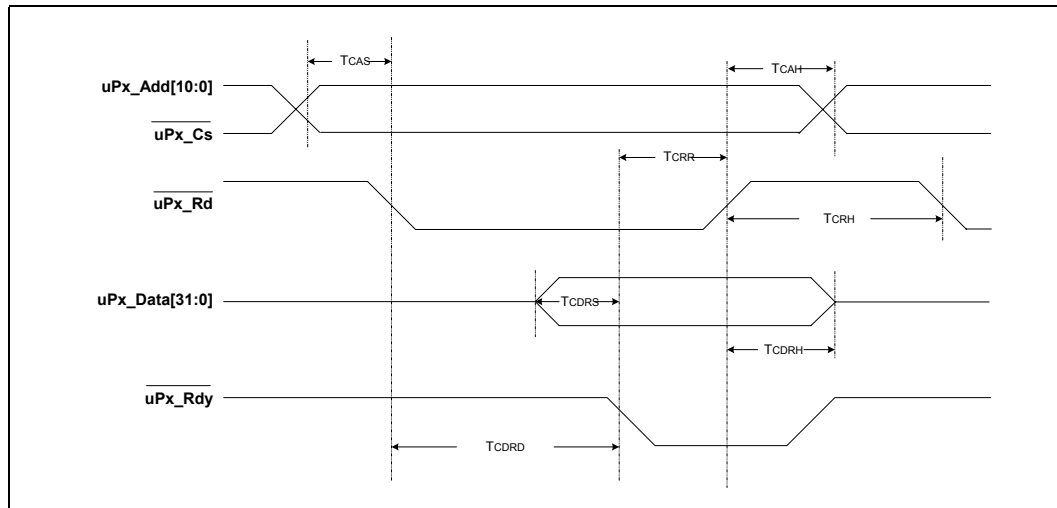
3.6.2.1 Read Access

Read access involves the following:

- Detect assertion of asynchronous Read control signal and latch address
- Generate internal Read strobe
- Drive valid data onto processor bus
- Assert asynchronous-ready signal for required length of time

Figure 22 provides the timing of the asynchronous interface for Read access.

Figure 22. Read Timing Diagram - Asynchronous Interface



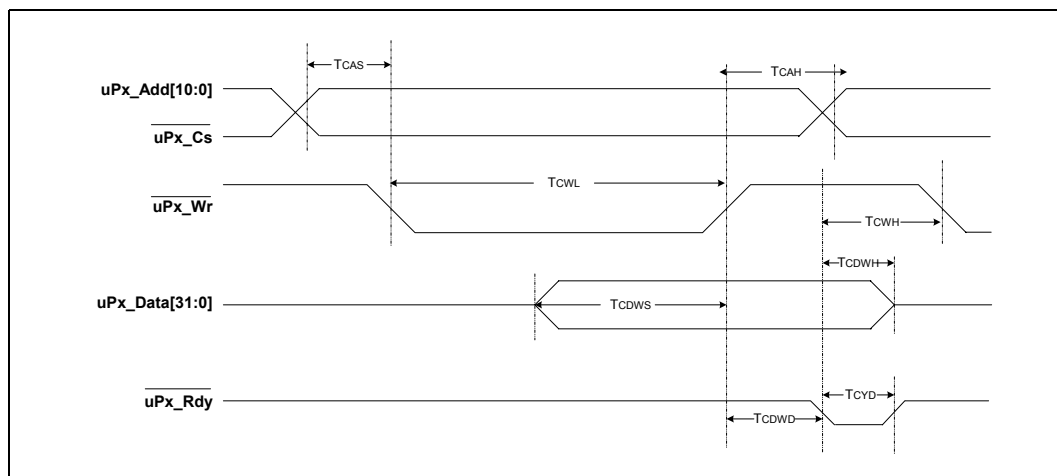
3.6.2.2 Write Access

The Write process involves the following:

- Detect assertion of asynchronous Write control signal and latch address
- Detect de-assertion of asynchronous Write control signal and latch data
- Generate internal Write strobe
- Assert asynchronous Ready signal for required length of time

Figure 23 illustrates the timing of the asynchronous interface for Write access.

Figure 23. Write Timing Diagram - Asynchronous Interface



3.6.3 Endian

The Endian of the CPU interface may be changed to allow connection of various CPUs to the IXF1010. The Endian selection is determined by setting the Endian bit in the CPU Interface Register (see [Table 73 on page 114](#)).

3.7 Clocks

The IXF1010 device has system interface reference clocks, SPI4-2 data path input and output clocks, RGMII input and output clocks, MDIO output clock, a JTAG input clock, and an LED output clock. This section details the unique clock source requirements.

3.7.1 System Interface Reference Clocks

There are two system interface clocks required by the IXF1010:

3.7.1.1 CLK125

The system interface clock, which supplies the clock to the majority of the internal circuitry, is the 125 MHz clock. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- +/- 50 ppm
- Maximum duty cycle distortion 40/60

3.7.1.2 CLK50

The other system interface clock supplies the clock source to the SPI4-2 receive circuitry. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- 1/8 frequency of the SPI4-2 data path clock (RDCLK+/-)
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Range = 40 Mhz to 50 MHz

3.7.2 SPI4-2 Receive and Transmit Data Path Clocks

The SPI4-2 data path clocks are compliant with the OIF 2000.88.4 Specification.

The IXF1010 has the following requirements on the transmit data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable (frequency and level) when reset is removed or when sourced, whichever happens last

- TSCLK frequency is one-quarter TDCLK frequency

The IXF1010 meets the following specifications on the receive data path:

- 2.5 V LVDS drive
- Maximum duty cycle distortion 45/55
- Maximum peak-to-peak jitter (low and high frequency) of 125 pS
- Stable when sourced

3.7.3 RGMII Clocks

The RGMII interface is governed by the HP 1.2a specification. The IXF1010 is fully specification compliant as follows:

- 2.5 V CMOS drive
- Maximum duty cycle distortion 40/60
- +/- 100 ppm
- 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps

3.7.4 MDC Clock

The IXF1010 device supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. The IXF1010 meets the following specification for this clock:

- 2.5 V CMOS drive
- 2.5/18 MHz operation (selectable by the MDC speed bit in the MDI Control Register)
- 50/50 duty cycle for 2.5 MHz operation
- 43/57 duty cycle for 18 MHz operation

3.7.5 JTAG Clock

The IXF1010 supports JTAG. The source of this clock must meet the following specifications:

- 2.5 V CMOS drive
- Maximum clock frequency 11 MHz
- Maximum duty cycle distortion 40/60

3.7.6 LED Clock

The IXF1010 supports a serial LED data stream. This interface implements a 2.5 V CMOS output clock with a maximum frequency of 720 kHz.

The IXF1010 supports a serial LED data stream. The IXF1010 meets the following specifications for this clock:

- 2.5 V CMOS drive



Intel® IXF1010 10-Port 100/1000 Mbps Ethernet Media Access Controller

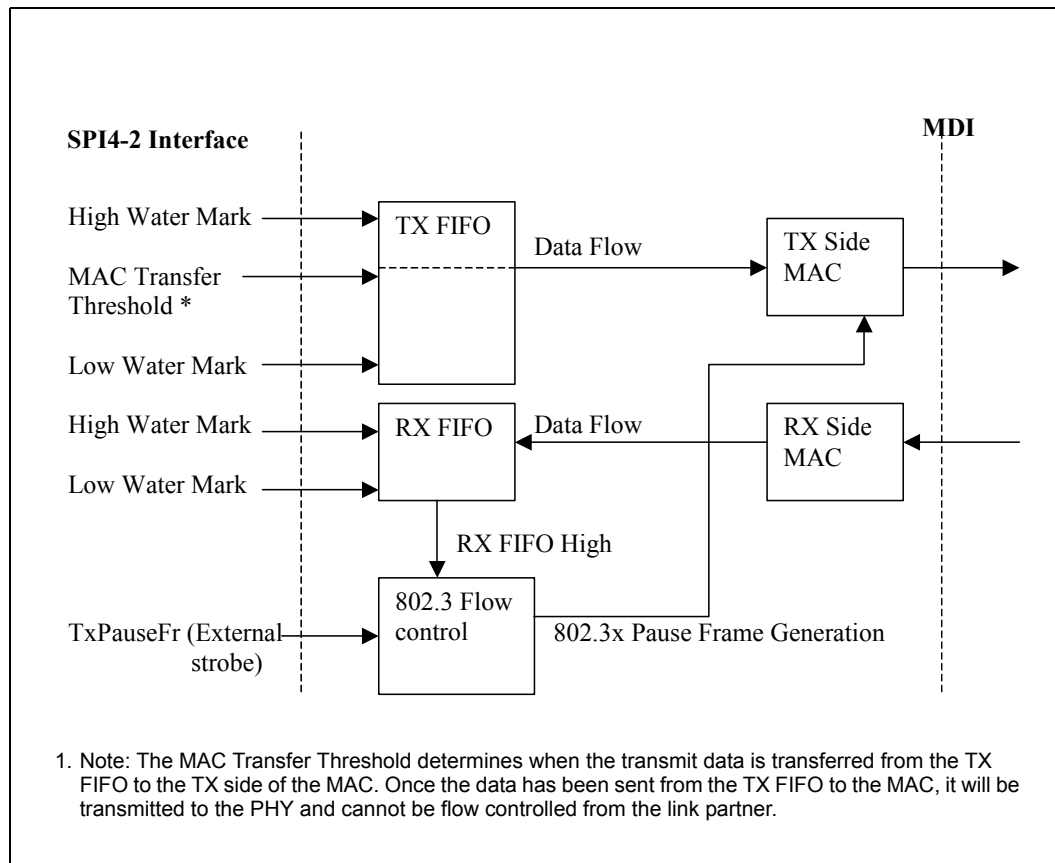
- Maximum frequency of 720 kHz
- Maximum duty cycle distortion: 50/50

4.0 Applications

4.1 TX and RX FIFO Operation

The Intel® IXF1010 packet buffering is comprised of individual port FIFOs and system-interface FIFOs. Figure 24 illustrates the interaction of these FIFOs.

Figure 24. Packet Buffering FIFO



4.1.1 TX FIFO

The IXF1010 TX FIFOs are implemented with 4.5 KB for each channel. This provides enough space for at least one maximum size packet per-port storage and ensures that no under-run conditions occur, assuming that the sending device can supply data at the required data rate.

The MAC threshold parameter, which is user programmable, determines when data is transmitted out of the MAC. This parameter is configurable for specific block sizes and the user must ensure that an under-run does not occur. The threshold must be set to a value that exceeds the programmed MaxBurst1 parameter. This method of operation eliminates the possibility of under-run, except when the controlling switch device fails.

4.1.2 RX FIFO

The IXF1010 RX FIFOs are provisioned so that each port has its own 17.0 KB memory space. This is enough memory to ensure against an over-run on any channel while transferring normal Ethernet frame-size data.

The FIFOs can be configured to automatically generate Pause control frames to initiate the following:

- Halt the link partner when the High watermark is reached
- Restart the link partner when the data stored in the FIFO falls below the low watermark

4.2 Reset and Initialization

When powering up the IXF1010, the hardware reset signal ($\overline{\text{Sys_Res}}$) should be held active Low for a minimum of 100 ns after all of the power rails have fully stabilized to their nominal values and the input clocks have reached their nominal frequency (TDCLK = 400 MHz, CLK125 = 125 MHz, and CLK50 = 50 MHz).

Note: In systems where the $\overline{\text{Sys_Res}}$ pin is driven from a single board-wide reset signal, the switch or network processor only comes out of reset at the same time as the IXF1010, or possibly later. This means the TDCLK will not be stable when the $\overline{\text{Sys_Res}}$ pin is released. A built-in feature in the IXF1010 reactivates the internal reset once TDCLK is applied. Ensure that the switch or network processor does not output TDCLK until it is stable and has reached its nominal operating frequency.

The IXF1010 extends this hardware reset internally to ensure synchronization of all internal blocks within the system. The internal reset is extended for a minimum of 4.11 ms after all clocks are stable.

The device is correctly initialized at this point and ready for use. Clocks start to appear at the relevant device ports and the SPI4-2 interface begins to source a training pattern on the receive side while waiting for a training pattern on the transmit side. The SPI4-2 interface synchronizes with the connected switch or network processor per the SPI4-2 Specification.

The CPU accesses can begin to configure the device for any existing user preferences desired. By default, all ports on the IXF1010 are enabled after power-up. The device is ready for use at this time if the default settings are to be used. Otherwise, access the required registers via the CPU interface and configure the control registers to the required settings.

5.0 Test Specifications

Table 19 through Table 33 on page 80 and Figure 29 on page 73 through Figure 36 on page 80 represent the target specifications of the following IXF1010 interfaces:

- RGMII
- MDIO
- CPU
- JTAG
- Transmit Pause Control
- Hardware Reset
- LED
- SPI4-2

Note: These specifications are not guaranteed and are subject to change without notice. Minimum and maximum values listed in Table 21 through Table 33 on page 80 apply over the recommended operating conditions specified in Table 19.

Table 19. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply Voltage		VDD	-0.3	2.4	Volts
		AVDD	-0.3	2.4	Volts
		VDD2	-0.3	3.0	Volts
		AVDD2	-0.3	3.0	Volts
Operating Temperature	Ambient	TOPA	-15	+85	°C
	Case	TOPC	–	+130	°C
Storage Temperature		TST	-65	+150	°C
<p>Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.</p>					

Table 20. Operating Conditions

Parameter		Symbol	Min	Typ ¹	Max	Units
Recommended Supply Voltage		VDD, AVDD	1.71	1.80	1.89	Volts
		VDD2, AVDD2	2.375	2.50	2.625	Volts
Operating Current	1000BASE-T	IDD, AIDD	–	2.062	–	Amps
		IDD2, AIDD2	–	0.432	–	Amps
Recommended Operating Temperature	Ambient	TOPA	0	–	70	°C
	Case with Heat Sink	TOPC-HS	0	–	118	°C
	Case without Heat Sink	TOPC-NHS	0	–	119	°C
Power Consumption	1000BASE-T full-duplex TX and RX at 25 °C	P	–	4.8	–	Watts
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Table 21. 2.5 V LVTTTL and CMOS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
Input Low Voltage	V _{IL}	–	–	0.70	V	VCC = MIN
Input High Voltage	V _{IH}	1.7	–	3.3	V	VCC = MIN
Output Low Voltage RGMII	VOLRG	–	–	0.40	V	VCC=MIN, IOL=6.9mA
Output Low Voltage All Others	V _{OL}	–	–	0.40	V	VCC = Min, IOL = 3.9 mA
Output High Voltage RGMII	VOHRG	2.0	–	–	V	VCC=MIN, IOH=-5.2mA
Output High Voltage All Others	V _{OH}	2.0	–	–	V	VCC = MIN, IOH = -2.9 mA
Output Leakage Current	I _{oZ}	–	–	10	μA	VCC = MAX
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						
2. 3.3 V CMOS tolerant.						

Table 22. LVDS I/O Electrical Characteristics

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
Input Voltage Range	V _I	-0.20	–	V _{ddMax} +0.20	V	–
Differential Input Voltage	V _{ID}	100	–	–	mV	@ 400 MHz
Input Common-Mode Current	ICM	–	–	–	μA	LVDS Input VOS = 1.2 V
Threshold Hysteresis	TH	25	–	–	mV	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Table 22. LVDS I/O Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
Differential Input Impedance	R _{IN}	85	–	115	Ω	Typical 100 Ω
Output Low Voltage	V _{OL}	0.95	–	–	V	–
Output High Voltage	V _{OH}	–	–	1.51	V	–
Differential Output Voltage	V _{OD}	330	–	446	mV	–
Delta Differential Output Voltage (Complementary States)	Δ V _{OD}	–	–	25	mV	–
Offset (Common-Mode) Voltage	V _{OS}	1.12	–	1.3	V	–
Output Leakage Current	I _{OZ}	–	–	10	μA	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 25. RGMII 1000 Mbps Multiplexing and Timing Diagram

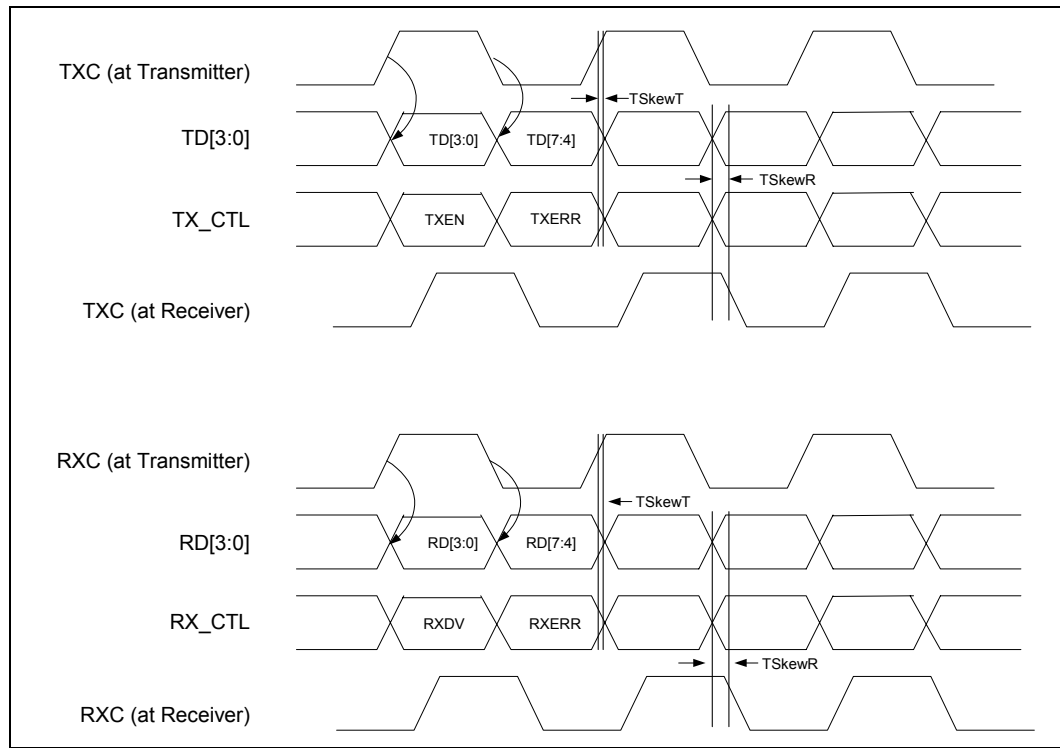


Table 23. RGMII 1000 Mbps Timing Specifics

Parameter	Symbol	Min	Typ ⁴	Max	Units	Test Conditions
Data-to-Clock Output Skew (at Transmitter)	TskewT	-500	0	500	ps	–
Data-to-Clock Input Skew (at Receiver) ¹	TskewR	1	1.5	2.8	ns	–
Clock Cycle Duration ²	Tcyc	7.2	8	8.8	ns	–
Duty Cycle for Gigabit ³	Duty_T	45	50	55	%	–
Rise/Fall Time (20-80%)	Tr/Tf	–	–	.75	ns	–

1. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
 2. For 100 Mbps, Tcyc scales to 40 ns +/- 4 ns.
 3. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain, as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.
 4. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 24. RGMII I/O Electrical Characteristics

Parameter	Symbol	Min	Max	Units	Test Conditions
Output High Voltage	V _{OH}	2.0	VDD +.3	V	I _{OH} = -1.0 mA; V _{CC} = MIN
Output Low Voltage	V _{OL}	GND -.3	0.40	V	I _{OL} = 1.0 mA; V _{CC} = MIN
Input High Voltage	V _{IH}	–	–	V	V _{IH} > V _{IH_MIN} ; V _{CC} = MIN
Input Low Voltage	V _{IL}	–	.70	V	V _{IH} > V _{IL_MAX} ; V _{CC} = MIN
Input High Current	I _{IH}	–	15	μA	V _{CC} = MAX; V _{IN} = 2.5V
Input Low Current	I _{IL}	-15	–	μA	V _{CC} = MAX; V _{IN} = 0.4V
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.					

Figure 26. RGMII 100 Mbps Multiplexing and Timing Diagram

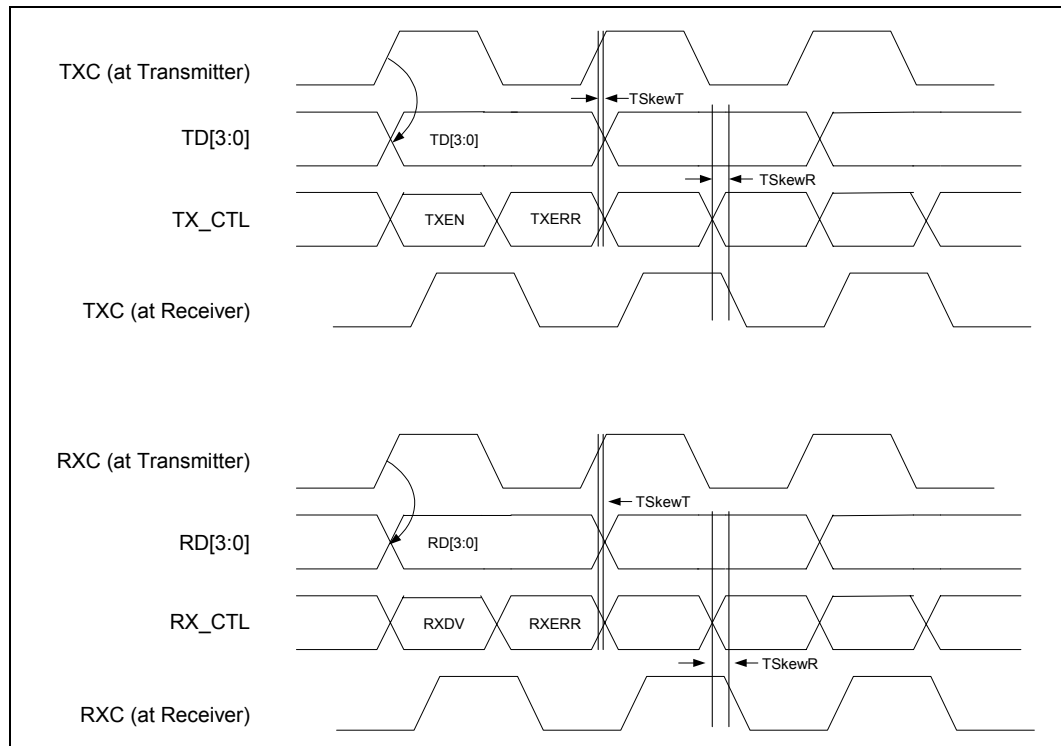


Table 25. RGMII 100 Mbps Timing Specifics

Parameter	Symbol	Min	Typ ⁴	Max	Units	Test Conditions
Data-to-Clock Output Skew (at Transmitter)	TskewT	-500	0	500	ps	–
Data-to-Clock Input Skew (at Receiver) ¹	TskewR	1	1.5	2.8	ns	–
Clock Cycle Duration ²	Tcyc	36	40	44	ns	–
Duty Cycle for 100T ³	Duty_G	40	50	60	%	–
Rise/Fall Time (20-80%)	Tr/Tf	–	–	.75	ns	–

1. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
 2. For 100 Mbps, Tcyc scales to 40 ns +/- 4 ns.
 3. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain, as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.
 4. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 27. MDIO Write Timing Diagram

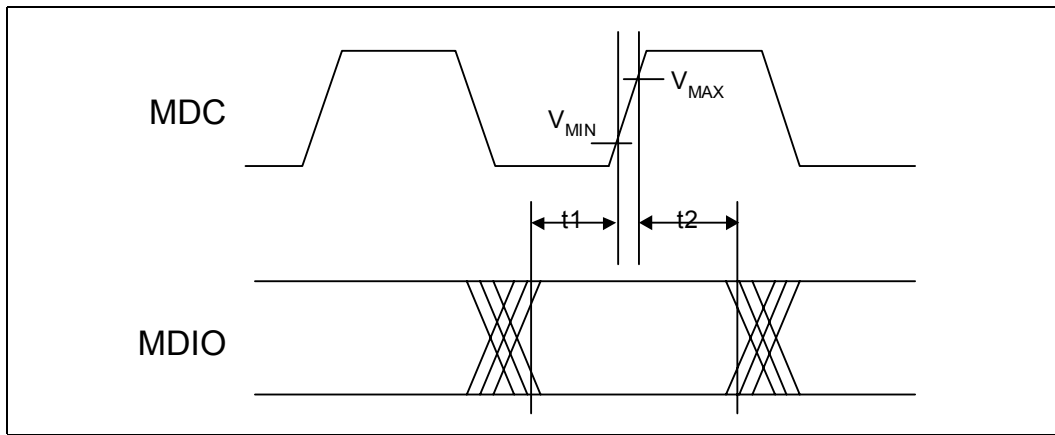


Figure 28. MDIO Read Timing Diagram

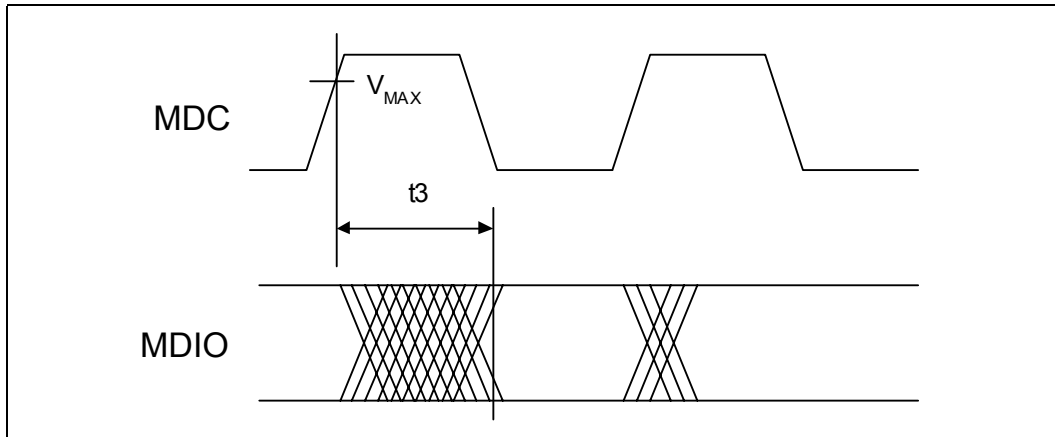


Table 26. MDIO Timing Parameters

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
MDIO Setup before MDC.	t1	10	–	–	ns	MDC = 17.8 MHz
		10	–	–	ns	MDC = 2.5 MHz
MDIO Hold after MDC.	t2	10	–	–	ns	MDC = 17.8 MHz
		10	–	–	ns	MDC = 2.5 MHz
MDC to MDIO Output delay	t3	0	–	30	ns	MDC = 17.8 MHz
		0	–	200	ns	MDC = 2.5 MHz

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 29. CPU Port Read Timing Diagram

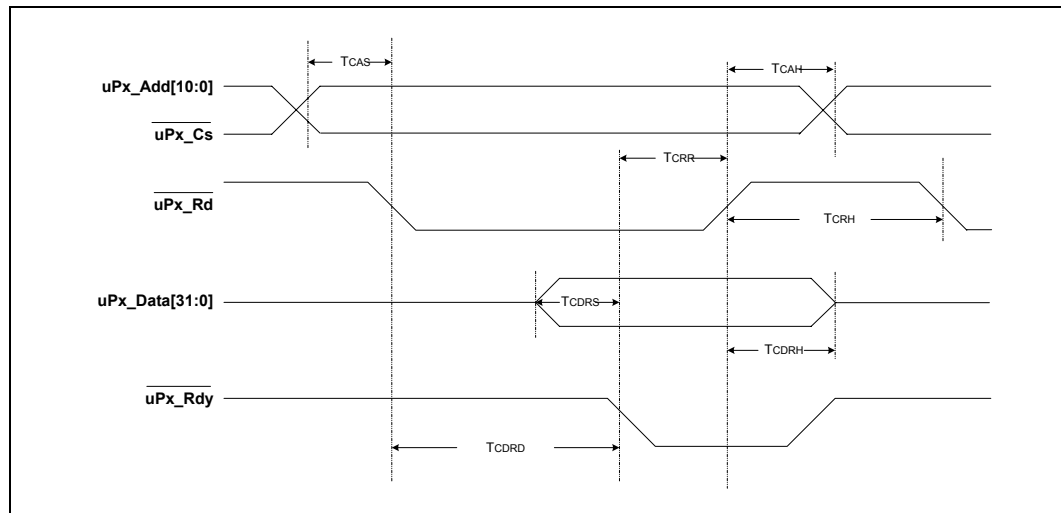


Figure 30. CPU Port Write Timing Diagram

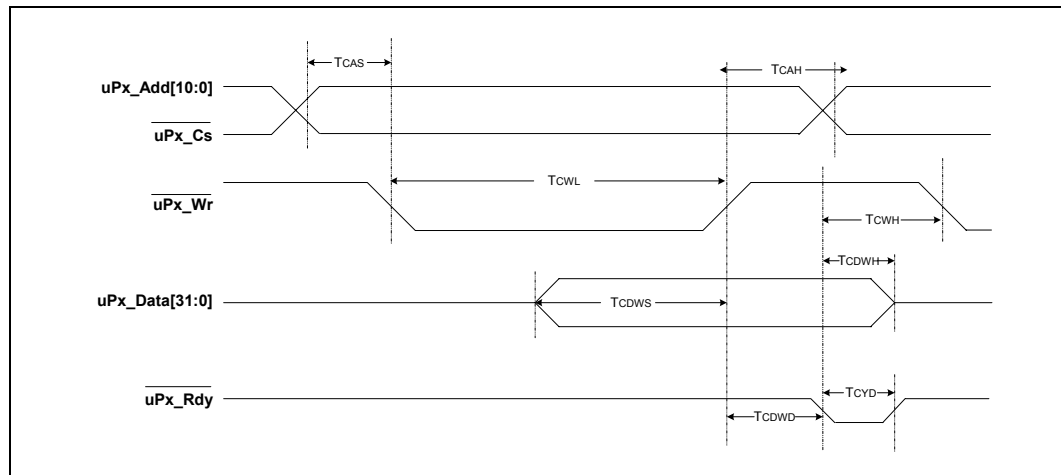


Table 27. CPU Timing Parameters

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
uPx_Add[12:0], uPx_Cs Setup Time	TCAS	10	–	–	ns	–
uPx_Add[12:0], uPx_Cs Hold Time	TCAH	10	–	–	ns	–
uPx_Rdy Assertion to uPx_Rd De-assertion	TCRR	10	–	–	ns	–
uPx_Rd High Width	TCRH	24 (3x cycle)	–	–	ns	–
uPx_Data[31:0] to uPx_Rdy Setup Time	TCDRS	10	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 27. CPU Timing Parameters (Continued)

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
$\overline{\text{uPx_Data}}[31:0]$ to $\overline{\text{uPx_Rd}}$ Hold Time	TCDRH	8	–	32	ns	–
Read $\overline{\text{uPx_Data}}[31:0]$ Driving Delay	TCDRD	24	–	120	ns	–
$\overline{\text{uPx_Wr}}$ Width	TCWL	40	–	–	ns	–
$\overline{\text{uPx_Rdy}}$ to $\overline{\text{uPx_Wr}}$ Hold Time	TCWH	16	–	–	ns	–
$\overline{\text{uPx_Data}}[31:0]$ to $\overline{\text{uPx_Wr}}$ Setup Time	TCDWS	10	–	–	ns	–
$\overline{\text{uPx_Rdy}}$ to $\overline{\text{uPx_Data}}[31:0]$ Hold Time	TCDWH	10	–	–	ns	–
$\overline{\text{uPx_Data}}[31:0]$ Latching Delay	TCDWD	8	–	32	ns	–
$\overline{\text{uPx_Rdy}}$ Width in Write Cycle	TCYD	24	–	40	ns	–
Read $\overline{\text{uPx_Rdy}}$ de-assertion to $\overline{\text{uPx_Wr}}$ Assertion	TRTW	32	–	–	ns	–
Write $\overline{\text{uPx_Rdy}}$ de-assertion to $\overline{\text{uPx_Rd}}$ Assertion	TWTR	32	–	–	ns	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 31. JTAG Timing Diagram

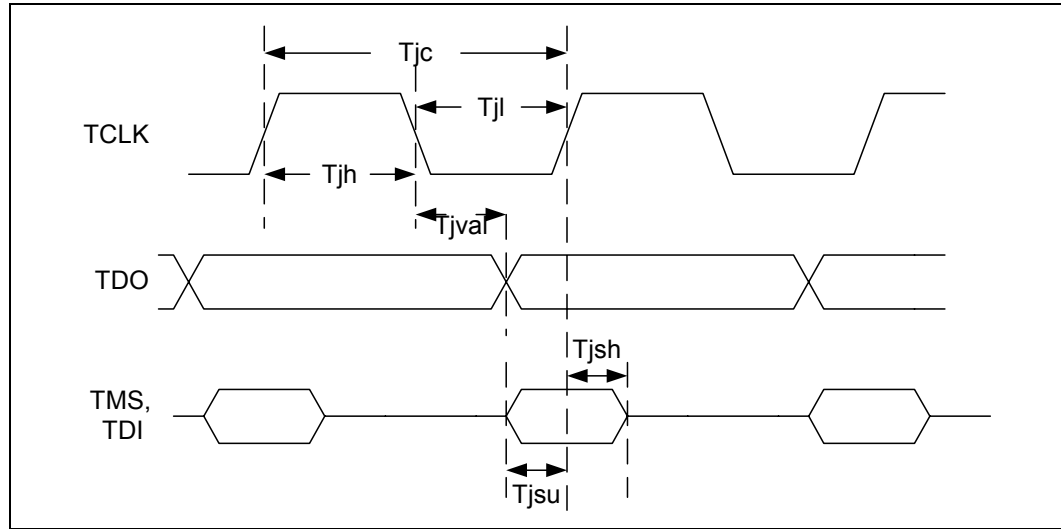


Table 28. JTAG Timing Parameters

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
TCLK Cycle Time	T_{JC}	90	–	–	ns	–
TCLK High Time	T_{JH}	$0.4 \times T_{JC}$	–	$0.6 \times T_{JC}$	ns	–
TCLK Low Time	T_{JL}	$0.4 \times T_{JC}$	–	$0.6 \times T_{JC}$	ns	–
TCLK Falling Edge to TDO Valid	T_{JVAL}	–	–	25	ns	–
TMS/TDI Setup to TCLK	T_{JSU}	20	–	–	ns	–
TMS/TDI Hold from TCLK	T_{JSH}	5	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 32. Transmit Pause Control Interface Diagram

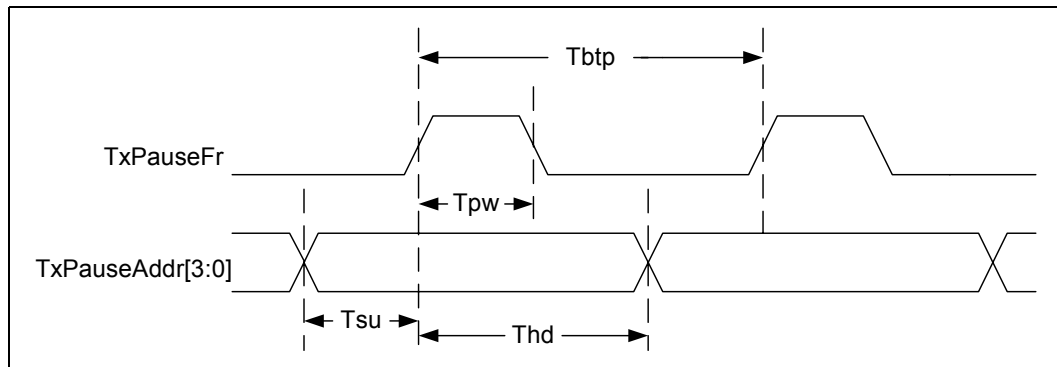


Table 29. Transmit Pause Control Interface Parameters

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
TxPauseFr Width	TPW	16	–	–	ns	–
TxPauseAddr[3:0] Setup to TxPauseFr	TSU	16	–	–	ns	–
TxPauseAddr[3:0] Hold from TxPauseFr	THD	32	–	–	ns	–
TxPauseFr Pulse to Pulse	TBTP	48	–	–	ns	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 33. Hardware Reset Timing Diagram

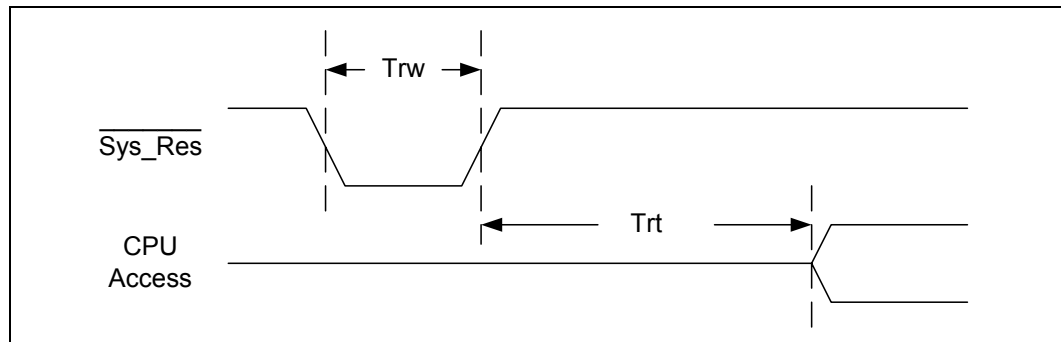


Table 30. Hardware Reset Timing Parameters

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
Reset Pulse Width	TRW	100	–	–	ns	–
Reset Recovery Time	TRT	4.11	–	–	μs	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 34. LED Timing Diagram

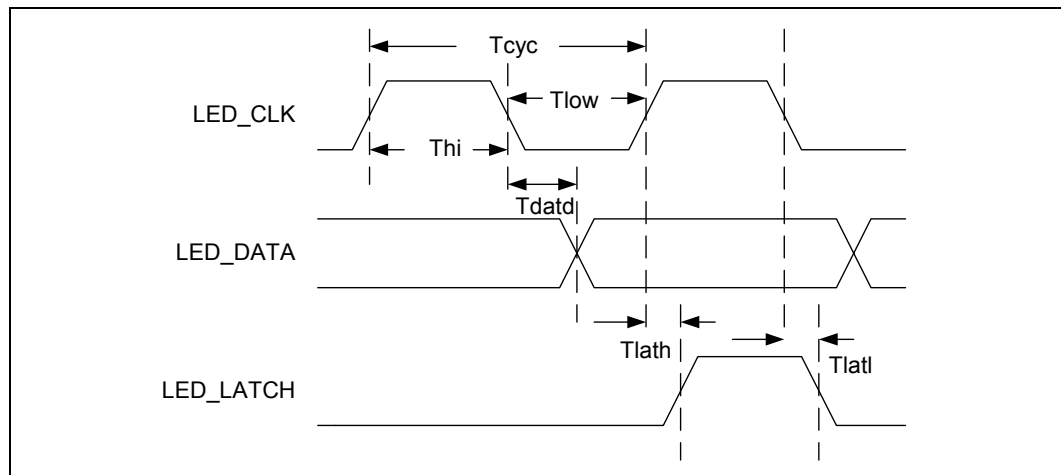


Table 31. LED Timing Parameters

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions ²
LED_CLK Cycle Time	Tcyc	1.36	–	1.40	ms	–
LED_CLK High Time	THI	680	–	700	μs	50% duty cycle
LED_CLK Low Time	TLOW	680	–	700	μs	50% duty cycle

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Flash Rate = 100 ms, LED Mode 1.

Table 31. LED Timing Parameters (Continued)

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions ²
LED_CLK Falling Edge to LED_DATA Valid	TDATD	2	–	5	ns	–
LED_CLK Rising Edge to LED_LATCH Rising Edge	TLATH	690	–	700	μs	–
LED_CLK Falling Edge to LED_LATCH Falling Edge	TLATL	690	–	700	μs	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing. 2. Flash Rate = 100 ms, LED Model.						

Figure 35. SPI4-2 Transmit FIFO Status Bus Timing Diagram

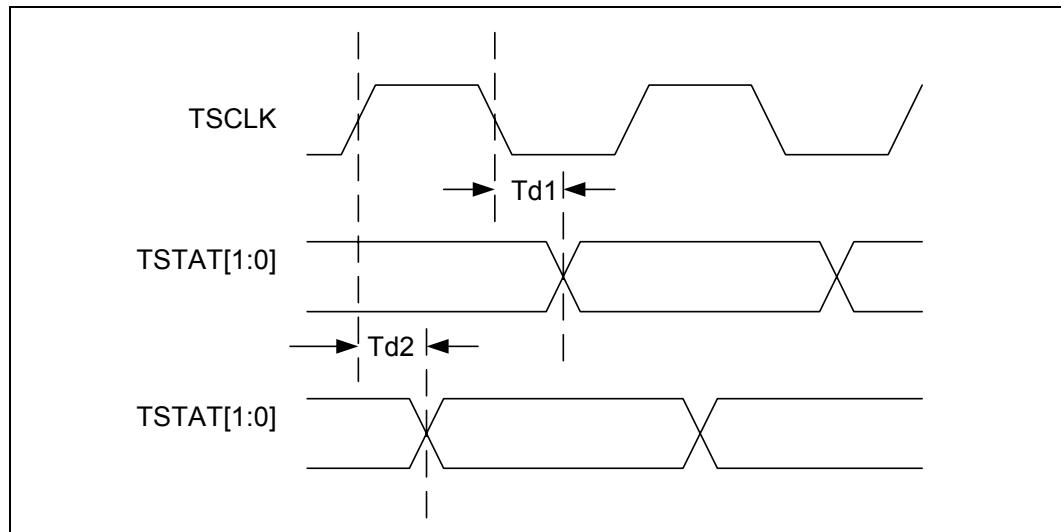


Table 32. SPI4-2 Transmit FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
TSClk Falling Edge to TSTAT[1:0] Valid (Active edge flipped to falling)	Td1	–	–	280	pS	–
TSClk Rising Edge to TSTAT[1:0] Valid (Default operation)	Td2	–	–	280	pS	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 36. SPI4-2 Receive FIFO Status Bus Timing Diagram

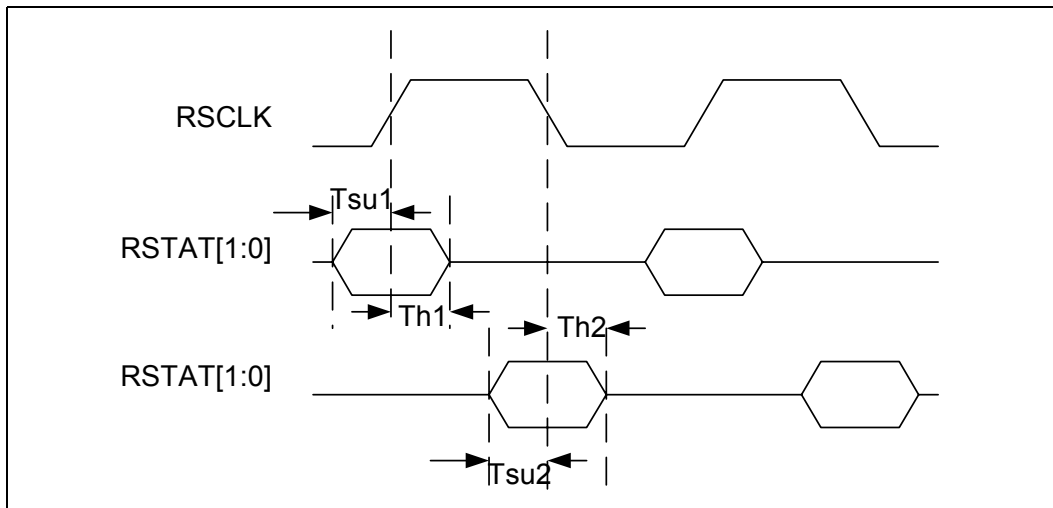


Table 33. SPI4-2 Receive FIFO Status Bus Timing Parameters

Parameter	Symbol	Min	Typ ¹	Max	Units	Test Conditions
RSTAT[1:0] Setup to RSCLK Rising Edge (Default operation)	Tsu1	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Rising Edge (Default operation)	Th1	0.5	–	–	ns	–
RSTAT[1:0] Setup to RSCLK Falling Edge (When active edge flipped to falling)	Tsu2	2	–	–	ns	–
RSTAT[1:0] Hold From RSCLK Falling Edge (When active edge flipped to falling)	Th2	0.5	–	–	ns	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

6.0 Register Definitions

6.1 Introduction

This section provides information on the location and functionality of the control and status registers contained in the Intel® IXF1010.

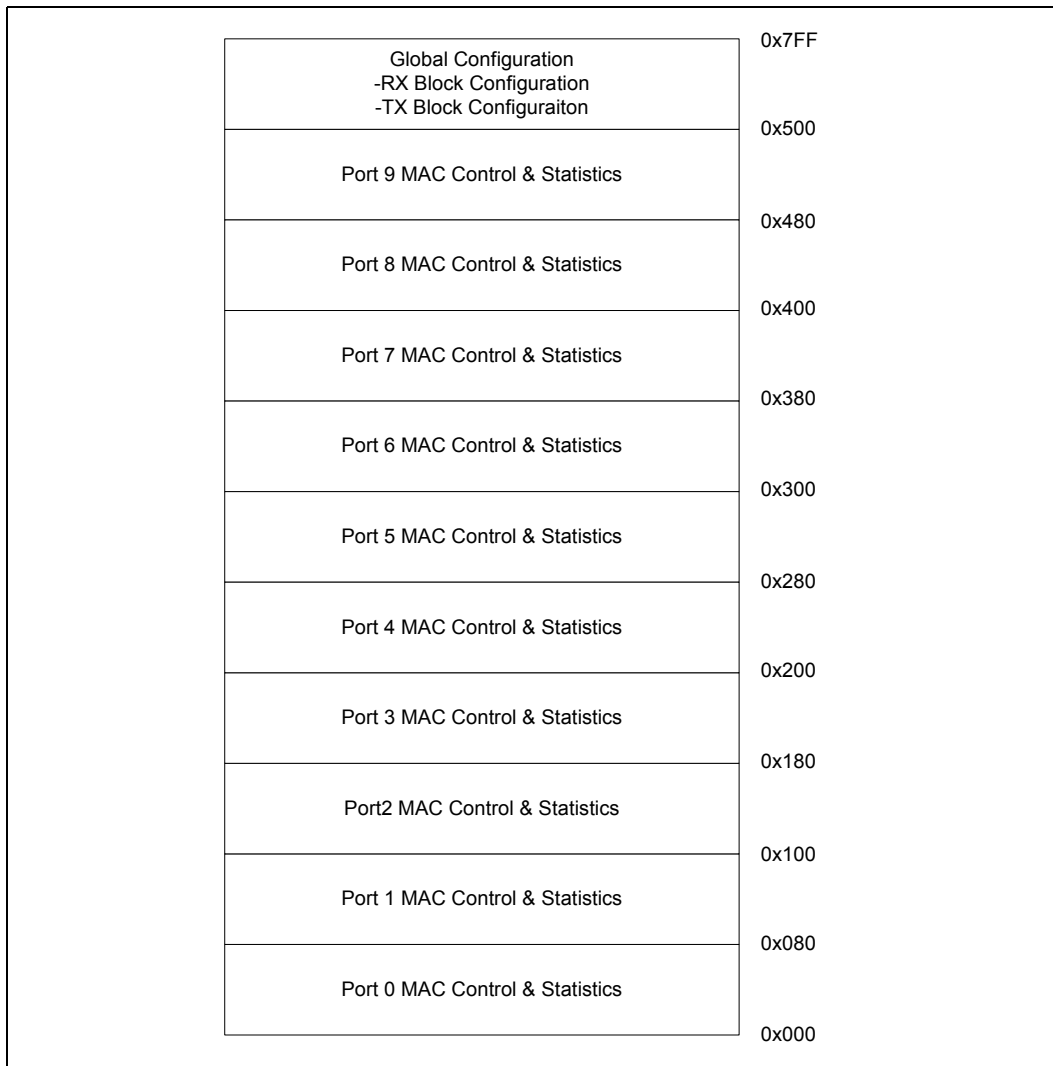
6.2 Document Structure

This document is structured to give a general overview of the register map and an in-depth description of each bit of a register in later sections.

6.3 Graphical Representation

[Figure 37](#) represents an overview of the IXF1010 global control status registers that are used to configure or report on all ports.

Figure 37. Memory Overview Diagram

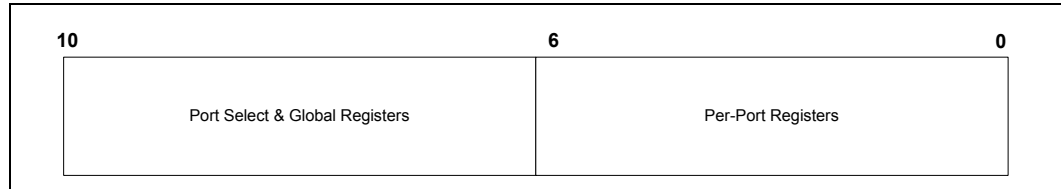


6.4 Per Port Registers

The following section covers all of the registers that are replicated in each of the 10 ports in the IXF1010. These registers perform an identical function in each port.

The address vector for the IXF1010 is 11 bits wide. This allows for 7 bits of port-specific access and a 4-bit vector to address each port and all global registers. The address format is shown in Figure 38.

Figure 38. Register Overview Diagram



6.5 Memory Map

Table 34 through Table 42 on page 91 provide the IXF1010 memory maps. A number of global control and status registers are used to configure or report on all ports, and some registers are replicated on a per-port basis.

Note: All registers in the IXF1010 are 32 bits.

Table 34. MAC Control Register Map

Register	Bit Size	Mode ¹	Ref Page	Offset
MAC Control Registers (Port Index + Offset)				
Station Address Low	32	R/W	92	0x00
Station Address High	32	R/W	92	0x01
Reserved	32	RO	–	0x02
FDFC Type	32	R/W	92	0x03
Reserved	32	RO	–	0x04
Reserved	32	RO	–	0x05
Reserved	32	RO	–	0x06
FC TX Timer Value	32	R/W	92	0x07
FDFC Address Low	32	R/W	93	0x08
FDFC Address High	32	R/W	93	0x09
Reserved	32	RO	–	0x0A
Reserved	32	RO	–	0x0B
IPG Transmit Time	32	R/W	93	0x0C
Reserved	32	R/W	--	0x0D
Pause Threshold	32	R/W	93	0x0E
Max Frame Size	32	R/W	94	0x0F
RGMII Speed	32	R/W	94	0x10
Reserved	32	RO	–	0x11
FC Enable	32	R/W	94	0x12
Reserved	32	RO	–	0x13
Short Runt Threshold	32	R/W	94	0x14
Discard Unknown Control Frame	32	R/W	95	0x15
Reserved	32	RO	–	0x16
Reserved	32	RO	–	0x17
Diverse Config	32	R/W	95	0x18
RX Packet Filter Control	32	R/W	95	0x19
Port Multicast Address Low	32	R/W	97	0x1A
Port Multicast Address High	32	R/W	97	0x1B
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 35. MAC RX Statistics Register Map

Register	Bit Size	Mode ¹	Ref Page	Offset
MAC RX Statistics Registers (Port Index + Offset)				
RXOctetsTotalOK	32	RR	98	0x20
RXOctetsBAD	32	RR	98	0x21
RXUCPkts	32	RR	98	0x22
RXMCPkts	32	RR	98	0x23
RXBCPkts	32	RR	98	0x24
RXPkts64Octets	32	RR	98	0x25
RXPkts65to127Octets	32	RR	98	0x26
RXPkts128to255Octets	32	RR	98	0x27
RXPkts256to511Octets	32	RR	98	0x28
RXPkts512to1023Octets	32	RR	98	0x29
RXPkts1024to1518Octets	32	RR	98	0x2A
RXPkts1519toMaxOctets	32	RR	98	0x2B
RXFCSErrors	32	RR	98	0x2C
RXTagged	32	RR	98	0x2D
RXDataError	32	RR	98	0x2E
RXAlignErrors	32	RR	98	0x2F
RXLongErrors	32	RR	98	0x30
RXJabberErrors	32	RR	98	0x31
RXPauseMacControlCounter	32	RR	98	0x32
RXUnknownMacControlFrameCounter	32	RR	98	0x33
RXVeryLongErrors	32	RR	98	0x34
RXRuntErrors	32	RR	98	0x35
RXShortErrors	32	RR	98	0x36
RXCarrierExtendError	32	RR	98	0x37
RXSequenceErrors	32	RR	98	0x38
RXSymbolErrors	32	RR	98	0x39
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 36. MAC TX Statistics Register Map

Register	Bit Size	Mode ¹	Ref Page	Offset
MAX TX Statistics Registers (Port Index + Offset)				
TXOctetsTotalOK	32	RR	102	0x40
TXOctetsBad	32	RR	102	0x41
TXUCPkts	32	RR	102	0x42
TXMCPkts	32	RR	102	0x43
TXBCPkts	32	RR	102	0x44
TXPkts64Octets	32	RR	102	0x45
TXPkts65to127Octets	32	RR	102	0x46
TXPkts128to255Octets	32	RR	102	0x47
TXPkts256to511Octets	32	RR	102	0x48
TXPkts512to1023Octets	32	RR	102	0x49
TXPkts1024to1518Octets	32	RR	102	0x4A
TXPkts1519toMaxOctets	32	RR	102	0x4B
TXDeferred	32	RR	102	0x4C
TXTotalCollisions	32	RR	102	0x4D
TXSingleCollisions	32	RR	102	0x4E
TXMultipleCollisions	32	RR	102	0x4F
TXLateCollisions	32	RR	102	0x50
TXExcessiveCollisionErrors	32	RR	102	0x51
TXExcessiveDeferralErrors	32	RR	102	0x52
TXExcessiveLengthDrop	32	RR	102	0x53
TXUnderrun	32	RR	102	0x54
TXTagged	32	RR	102	0x55
TXCRCError	32	RR	102	0x56
TXPauseFrames	32	RR	102	0x57
TXFlowControlCollisionsSend	32	RR	102	0x58
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 37. PHY Autoscan Register Map

Register	Bit Size	Mode ¹	Ref Page	Offset
PHY Autoscan Registers (Port Index + Offset)				
PHY Control	32	RO	106	0x60
PHY Status	32	RO	107	0x61
PHY ID 1	32	RO	108	0x62
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				



Table 37. PHY Autoscan Register Map (Continued)

Register	Bit Size	Mode ¹	Ref Page	Offset
PHY Autoscan Registers (Port Index + Offset)				
PHY ID 2	32	RO	108	0x63
Auto-Negotiation Advertisement	32	RO	108	0x64
Auto-Negotiation Link Partner Base Page Ability	32	RO	109	0x65
Auto-Negotiation Expansion	32	RO	110	0x66
Auto-Negotiation Next Page Transmit	32	RO	111	0x67
Reserved	32	RO	--	0x68
Reserved	32	RO	--	0x69
Reserved	32	RO	--	0x6A
Reserved	32	RO	--	0x6B
Reserved	32	RO	--	0x6C
Reserved	32	RO	--	0x6D
Reserved	32	RO	--	0x6E
Reserved	32	RO	--	0x6F
Vendor Specific	32	RO	--	0x70
Vendor Specific	32	RO	--	0x71
Vendor Specific	32	RO	--	0x72
Vendor Specific	32	RO	--	0x73
Vendor Specific	32	RO	--	0x74
Vendor Specific	32	RO	--	0x75
Vendor Specific	32	RO	--	0x76
Vendor Specific	32	RO	--	0x77
Vendor Specific	32	RO	--	0x78
Vendor Specific	32	RO	--	0x79
Vendor Specific	32	RO	--	0x7A
Vendor Specific	32	RO	--	0x7B
Vendor Specific	32	RO	--	0x7C
Vendor Specific	32	RO	--	0x7D
Vendor Specific	32	RO	--	0x7E
Vendor Specific	32	RO	--	0x7F
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 38. Global Status and Configuration Register Map

Register	Bit Size	Mode ¹	Ref Page	Address
Port Enable	32	R/W	112	0x500
Reserved	32	RO	–	0x501
Link LED Enable	32	R/W	113	0x502
Reserved	32	RO	–	0x503
Reserved	32	RO	–	0x504
Reserved	32	RO	–	0x505
MDIO Soft Reset	32	R/W	114	0x506
Reserved	32	RO	–	0x507
CPU Interface	32	R/W	114	0x508
LED Control	32	R/W	114	0x509
LED Flash Rate	32	R/W	114	0x50A
LED Fault Disable	32	R/W	115	0x50B
JTAG ID	32	R/W	116	0x50C
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 39. RX Block Register Map

Register	Bit Size	Mode ¹	Ref Page	Address
RX FIFO High Watermark Port 0	32	R/W	117	0x580
RX FIFO High Watermark Port 1	32	R/W	117	0x581
RX FIFO High Watermark Port 2	32	R/W	117	0x582
RX FIFO High Watermark Port 3	32	R/W	117	0x583
RX FIFO High Watermark Port 4	32	R/W	117	0x584
RX FIFO High Watermark Port 5	32	R/W	117	0x585
RX FIFO High Watermark Port 6	32	R/W	117	0x586
RX FIFO High Watermark Port 7	32	R/W	117	0x587
RX FIFO High Watermark Port 8	32	R/W	117	0x588
RX FIFO High Watermark Port 9	32	R/W	117	0x589
RX FIFO Low Watermark Port 0	32	R/W	118	0x58A
RX FIFO Low Watermark Port 1	32	R/W	118	0x58B
RX FIFO Low Watermark Port 2	32	R/W	118	0x58C
RX FIFO Low Watermark Port 3	32	R/W	118	0x58D
RX FIFO Low Watermark Port 4	32	R/W	118	0x58E
RX FIFO Low Watermark Port 5	32	R/W	118	0x58F
RX FIFO Low Watermark Port 6	32	R/W	118	0x590
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				



Table 39. RX Block Register Map (Continued)

Register	Bit Size	Mode ¹	Ref Page	Address
RX FIFO Low Watermark Port 7	32	R/W	118	0x591
RX FIFO Low Watermark Port 8	32	R/W	118	0x592
RX FIFO Low Watermark Port 9	32	R/W	118	0x593
RX FIFO Number of Frames Removed on Port 0	32	RR	120	0x594
RX FIFO Number of Frames Removed on Port 1	32	RR	120	0x595
RX FIFO Number of Frames Removed on Port 2	32	RR	120	0x596
RX FIFO Number of Frames Removed on Port 3	32	RR	120	0x597
RX FIFO Number of Frames Removed on Port 4	32	RR	120	0x598
RX FIFO Number of Frames Removed on Port 5	32	RR	120	0x599
RX FIFO Number of Frames Removed on Port 6	32	RR	120	0x59A
RXFIFO Number of Frames Removed on Port 7	32	RR	120	0x59B
RX FIFO Number of Frames Removed on Port 8	32	RR	120	0x59C
RX FIFO Number of Frames Removed on Port 9	32	RR	120	0x59D
Reserved	32	RO	–	0x59E
RX FIFO Errored Frames Drop Enable	32	R/W	122	0x59F
RX FIFO Overflow Event	32	RR	123	0x5A0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 40. TX Block Register Map

Register	Bit Size	Mode ¹	Ref Page	Address
TX FIFO High Watermark Port 0	32	R/W	125	0x600
TX FIFO High Watermark Port 1	32	R/W	125	0x601
TX FIFO High Watermark Port 2	32	R/W	125	0x602
TX FIFO High Watermark Port 3	32	R/W	125	0x603
TX FIFO High Watermark Port 4	32	R/W	125	0x604
TX FIFO High Watermark Port 5	32	R/W	125	0x605
TX FIFO High Watermark Port 6	32	R/W	125	0x606
TX FIFO High Watermark Port 7	32	R/W	125	0x607
TX FIFO High Watermark Port 8	32	R/W	125	0x608
TX FIFO High Watermark Port 9	32	R/W	125	0x609
TX FIFO Low Watermark Port 0	32	R/W	125	0x60A
TX FIFO Low Watermark Port 1	32	R/W	126	0x60B
TX FIFO Low Watermark Port 2	32	R/W	126	0x60C
TX FIFO Low Watermark Port 3	32	R/W	126	0x60D
TX FIFO Low Watermark Port 4	32	R/W	126	0x60E

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 40. TX Block Register Map (Continued)

Register	Bit Size	Mode ¹	Ref Page	Address
TX FIFO Low Watermark Port 5	32	R/W	126	0x60F
TX FIFO Low Watermark Port 6	32	R/W	126	0x610
TX FIFO Low Watermark Port 7	32	R/W	126	0x611
TX FIFO Low Watermark Port 8	32	R/W	126	0x612
TX FIFO Low Watermark Port 9	32	R/W	126	0x613
TX FIFO MAC Transfer Threshold Port 0	32	R/W	128	0x614
TX FIFO MAC Transfer Threshold Port 1	32	R/W	128	0x615
TX FIFO MAC Transfer Threshold Port 2	32	R/W	128	0x616
TX FIFO MAC Transfer Threshold Port 3	32	R/W	128	0x617
TX FIFO MAC Transfer Threshold Port 4	32	R/W	128	0x618
TX FIFO MAC Transfer Threshold Port 5	32	R/W	128	0x619
TX FIFO MAC Transfer Threshold Port 6	32	R/W	128	0x61A
TX FIFO MAC Transfer Threshold Port 7	32	R/W	128	0x61B
TX FIFO MAC Transfer Threshold Port 8	32	R/W	128	0x61C
TX FIFO MAC Transfer Threshold Port 9	32	R/W	128	0x61D
TX FIFO Overflow Event	32	RR	131	0x61E
Reserved	32	RO	–	0x61F
Reserved	32	RO	–	0x620
TX FIFO Info Out of Sequence	32	RR	132	0x621
TX FIFO Number of Frames Removed on Port 0	32	RR	132	0x622
TX FIFO Number of Frames Removed on Port 1	32	RR	132	0x623
TX FIFO Number of Frames Removed on Port 2	32	RR	132	0x624
TX FIFO Number of Frames Removed on Port 3	32	RR	132	0x625
TX FIFO Number of Frames Removed on Port 4	32	RR	132	0x626
TX FIFO Number of Frames Removed on Port 5	32	RR	132	0x627
TX FIFO Number of Frames Removed on Port 6	32	RR	132	0x628
TX FIFO Number of Frames Removed on Port 7	32	RR	132	0x629
TX FIFO Number of Frames Removed on Port 8	32	RR	132	0x62A
TX FIFO Number of Frames Removed on Port 9	32	RR	132	0x62B

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write



Table 41. MDIO Block Register Map

Register	Bit Size	Mode ¹	Ref Page	Address
MDI Single Command	32	R/W	134	0x680
MDI Single Read and Write Data	32	R/W	134	0x681
Autoscan PHY Address Enable	32	R/W	134	0x682
MDI Control	32	R/W	135	0x683
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 42. SPI4-2 Block Register Map

Register	Bit Size	Mode ¹	Ref Page	Address
SPI4-2 Rx Burst Size	32	R/W	136	0x700
SPI4-2 Rx Training	32	R/W	136	0x701
SPI4-2 Calendar	32	R/W	137	0x702
SPI4-2 Tx Synchronization	32	R/W	138	0x703
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.1 MAC Control Registers

Table 43 through Table 59 on page 97 provide details on the control and status registers associated with each MAC port. The register address is ‘Port_index + 0x**’, where the port index is set at any value from 0x000 through 0x500. All registers are 32 bits.

Table 43. Station Address Register Low (Addr: Port_Index + 0x00)

Bit	Name	Description	Type ¹	Default
31:0	Station Address Low	Source MAC address bits 31-0. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 44. Station Address Register High (Addr: Port_Index + 0x01)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Station Address High	Source MAC address bits 47-32. This address is inserted in the source address field when transmitting Pause frames, and is also used to compare against unicast Pause frames at the receiving side.	R/W	
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 45. FDFC Type Register (Addr: Port_Index + 0x03)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FDFC Type	Contains the value of the type field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds its high watermark.	R/W	0x8808
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 46. FC TX Timer Value Register (Addr: Port_Index + 0x07)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FC TX Timer Value	The pause length sent to the receiving station in 512 bit times	R/W	0x005E
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 47. FDFC Address Low Register (Addr: Port_Index + 0x08)

Bit	Name	Description	Type ¹	Default
31:0	FDFC Address Low	Contains the value of the lowest 32 bits of the destination address field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds its high watermark.	R/W	0xC2000001
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 48. FDFC Address High Register (Addr: Port_Index + 0x09)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	FDFC Address High	Contains the value of the highest 16 bits of the destination address field transmitted in an internally generated flow control (pause) frame. Internally generated flow control frames are generated via the external pause interface or when the RX FIFO exceeds its high watermark.	R/W	0x0180
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 49. IPG Transmit Time Register (Addr: Port_Index + 0x0C)

Bit	Name	Description	Type ¹	Default
31:10	Reserved	Reserved	RO	0x0000
9:0	IPG Transmit Time	IPG time for back-to-back transmissions (specified in multiples of 512 bit times) Note: The value specified in this register should be four less than desired.	R/W	0x0008
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 50. Pause Threshold Register (Addr: Port_Index + 0x0E)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Pause Threshold	When a pause frame is sent, an internal timer checks when a new pause frame must be scheduled for transmission to keep the link partner in pause mode. The pause threshold value is the minimum time to send before the earlier pause frame is aged out (specified in multiples of 512 bit times).	R/W	0x002F
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 51. Max Frame Size Register (Addr: Port_Index + 0x0F)

Bit	Name	Description	Type ¹	Default
31:14	Reserved	Reserved	RO	0x0000
13:0	Max Frame Size	The maximum frame size the MAC can receive or transmit without activating any error counters, and without truncation. The maximum frame size is internally adjusted by +4 if VLAN is tagged.	R/W	0x05EE
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 52. RGMII Speed Register (Addr: Port_Index + 0x10)

Bit	Name	Description	Type ¹	Default
31:2	Reserved	Reserved	RO	0x00000000
1:0	RGMII Speed	These bits are used to define the speed of the IXF1010 operation. 01 = 100 Mbps - RGMII TX_CLK is 25 MHz 1x = 1 Gbps - RGMII TX_CLK is 125 MHz	R/W	11
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 53. FC Enable Register (Addr: Port_Index + 0x12)

Bit	Name	Description	Type ¹	Default
Register Description: Indicates flow control settings of the IXF1010.				0x00000007
31:2	Reserved	Reserved	RO	0x00000001
1	TX FD FC	1 = Enable TX FD Flow Control 0 = Disables	R/W	1
0	RX FD FC	1 = Enable RX FD Flow Control 0 = Disables	R/W	1
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 54. Short Runts Threshold Register (Addr: Port_Index + 0x14)

Bit	Name	Description	Type ¹	Default
31:5	Reserved	Reserved	RO	0x00000000
4:0	Short Runts Threshold	Holds the value in bytes, which applies to the threshold in determining between runts and short.	R/W	01000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 55. Discard Unknown Control Frame Register (Addr: Port_Index + 0x15)

Bit	Name	Description	Type ¹	Default
31:1	Reserved	Reserved	RO	0x00000000
0	Discard Unknown Control Frame	0 = Keep unknown control frames 1 = Discard unknown control frames.	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 56. Diverse Config Register (Addr: Port_Index + 0x18)

Bit	Name	Description	Type ¹	Default
Register Description: This register enables the padding of undersized frames on transmit and automatic CRC generation. For proper operation, if padding of undersized frames is enabled, the automatic CRC generation must be enabled.				0x0000110D
31:8	Reserved	Reserved	RO	0
7	pad_enable	Enable padding of undersized packets	R/W	0
6	crc_add	Enable automatic CRC appending	R/W	0
5:0	Reserved	Reserved	RO	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 57. RX Packet Filter Control Register (Addr: Port_Index + 0x19)

Bit	Name	Description	Type ¹	Default
Register Description: This register allows for specific packet types to be marked for filtering, and is used in conjunction with the RX FIFO Errored Frames Drop Enable Register				0x00000000
31:6	Reserved	Reserved	RO	0x00000000
5	CRC Error Pass ²	This bit enables a Global filter on frames with a CRC Error. When CRCErrorPASS = 0, all frames with a CRC Error are marked as bad. Note: When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 81 on page 122). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When CRCErrorPASS = 1, frames with a CRC Error are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write
2. Jumbo frames (1519 - 9600 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.
3. Frames are dropped only when the appropriate bits are set in the RX FIFO Errored Frame Drop Enable Register ([Table 81 on page 122](#)). When the appropriate bits are not set, the frames are sent across the SPI4-2 interface and marked as EOP abort frames.

Table 57. RX Packet Filter Control Register (Addr: Port_Index + 0x19) (Continued)

Bit	Name	Description	Type ¹	Default
4	Pause Frame Pass ²	This bit enables a Global filter on Pause frames. When PauseFramePass = 0, all Pause frames are marked as bad. Note: When used in conjunction with the RX FIFO ErroredFrameDropEnable[9:0] Register (see Table 81 on page 122). This allows the frame to be dropped in the RX FIFO. Otherwise, the frame is sent across the SPI4-2 interface but marked as an EOP Abort frame. When PauseFramePass = 1, all Pause frames are not marked as bad and are passed to the SPI4-2 interface for transfer as good frames, regardless of the state of the FrameDropEn[9:0] bits.	R/W	0
3	VLAN Drop En ²	This bit enables a Global filter on VLAN frames. When VLANDropEn = 0, all VLAN frames are passed to the SPI4-2 Interface. When VLANDropEn = 1, all VLAN frames are dropped. ³	R/W	0
2	B/Cast Drop En ²	This bit enables a Global filter on Broadcast frames. When B/CastDropEn = 0, all broadcast frames are passed to the SPI4-2 Interface. When B/CastDropEn = 1, all broadcast frames are dropped. ³	R/W	0
1	M/Cast Match En ²	This bit enables a filter on multicast frames. If this bit = 0, all multicast frames are good and are passed to the SPI4-2 Interface. If this bit = 1, only multicast frames with a destination address that matches the PortMulticastAddress is forwarded. All other multicast frames are dropped. ³	R/W	0
0	U/Cast Match En ²	This bit enables a filter on unicast frames. If this bit = 0, all unicast frames are good and are passed to the SPI4-2 interface. If this bit = 1, only unicast frames with a destination address that matches the Station Address is forwarded. All other unicast frames are dropped. ³	R/W	0
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write</p> <p>2. Jumbo frames (1519 - 9600 bytes), matching the filter conditions, which would cause the frame to be dropped by the RX FIFO, will not be dropped. Instead, jumbo frames that are marked to be dropped by the RX FIFO, based on the filter setting in this register, will still be sent across the SPI4-2 interface, but will be marked as an EOP abort frame. Thus, jumbo frames matching the filter conditions will not be counted in the RX FIFO Number of Frames Removed Register because they are not removed by the RX FIFO. Only standard packet sizes (64 - 1518 bytes) meeting the filter conditions set in this register will actually be dropped by the RX FIFO and counted in the RX FIFO Number of Frames Removed.</p> <p>3. Frames are dropped only when the appropriate bits are set in the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122). When the appropriate bits are not set, the frames are sent across the SPI4-2 interface and marked as EOP abort frames.</p>				



Table 58. Port Multicast Address Low Register (Addr: Port_Index + 0x1A)

Bit	Name	Description	Type ¹	Default
31:0	Port Multicast Address Low	This address is used to compare against multicast frames at the receiving side if multicast filtering is enabled. This register contains bits 31:0 of the address.	R/W	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 59. Port Multicast Address High Register (Addr: Port_Index + 0x1B)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0x0000
15:0	Port Multicast Address High	This address is used to compare against multicast frames at the receiving side if Multicast filtering is enabled. This register contains bits 47:32 of the address.	R/W	0x0000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.2 MAC RX Statistics Register Overview

The MAC RX Statistics Registers contain the MAC receiver statistic counters and are cleared when read. The software polls these registers and accumulates values to ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 60 covers the MAC RX Statistics Registers for all 10 MAC ports. The address is identical to the port number.

Table 60. MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)

Name	Description	Address	Type ¹	Default
RxOctetsTotalOK	Counts the bytes received in all legal frames, including all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x20	RR	0x00000000
RxOctetsBAD ²	Counts the bytes received in all bad frames of a size greater than or equal to 64 bytes. A bad frame is defined as a properly framed packet containing a CRC, alignment error, or code violation. The 64-byte value is measured from the destination address, up to and including CRC. The initial preamble and SFD are not included in this value. Note: This register does not increment the Bad Octet count on undersized receive packets.	Port_Index + 0x21	RR	0x00000000
RxUCPkts	The total number of unicast packets received (excluding bad packets) Note: This count includes non-pause control and VLAN packets, which are also counted in other counters. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x22	RR	0x00000000
RxMCPkts	The total number of multicast packets received (excluding bad packets) Note: This count includes pause control packets, which are also counted in the PauseMacControl-ReceivedCounter. These packet types are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x23	RR	0x00000000
RxBcPkts	The total number of Broadcast packets received (excluding bad packets)	Port_Index + 0x24	RR	0x00000000
RxPkts64Octets	The total number of packets received (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x25	RR	0x00000000
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write</p> <p>2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2¹⁴-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2¹⁴-1. MaxFrameSize is determined by the settings in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 94.</p>				

**Table 60. MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)
(Continued)**

Name	Description	Address	Type ¹	Default
RxPkts65to127 Octets	The total number of packets received (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x26	RR	0x00000000
RxPkts128to255 Octets	The total number of packets received (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128-255 bytes, including tag field	Port_Index + 0x27	RR	0x00000000
RxPkts256to511 Octets	The total number of packets received (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x28	RR	0x00000000
RxPkts512to1023 Octets	The total number of packets received (including bad packets) that were [512-1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x29	RR	0x00000000
RxPkts1024to1518 Octets	The total number of packets received (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x2A	RR	0x00000000
RxPkts1519toMax Octets	The total number of packets received (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max frame size, including the tag	Port_Index + 0x2B	RR	0x00000000
RxFCSErrors	Number of frames received with legal size, but with wrong CRC field (also called FCS field) Note: Legal size is 64 bytes through the value stored in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 94.	Port_Index + 0x2C	RR	0x00000000
RxTagged	Number of frames (including bad packets) with VLAN tag (Type field = 0x8100)	Port_Index + 0x2D	RR	0x00000000
RxDataError	Number of frames received with legal length, containing a code violation (signaled with RX_ERR on RGMII)	Port_Index + 0x2E	RR	0x00000000
RxAlignErrors	Frames with a legal frame size, but containing less than 8 additional bits. The CRC of the frame is wrong when the additional bits are stripped. If the CRC is OK, the frame is not counted, but treated as an OK frame.	Port_Index + 0x2F	RR	0x00000000
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2¹⁴-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2¹⁴-1. MaxFrameSize is determined by the settings in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 94.</p>				

**Table 60. MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)
(Continued)**

Name	Description	Address	Type ¹	Default
RxLongErrors ²	Frames bigger than the maximum allowed, with both OK CRC and the integral number of octets Default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x30	RR	0x00000000
RxJabberErrors	Frames bigger than the maximum allowed, with either a bad CRC or a non-integral number of octets. The default maximum allowed is 1518 bytes untagged and 1522 bytes tagged, but the value can be changed by a register. Frames bigger than the larger of 2*MaxFrameSize and 50000 bits are not counted here, but counted in the VeryLongError counter.	Port_Index + 0x31	RR	0x00000000
RxPauseMac ControlCounter	Number of Pause MAC control frames received	Port_Index + 0x32	RR	0x00000000
RxUnknownMac ControlFrame Counter	Number of MAC control frames received with an op code different from 0001 (Pause)	Port_Index + 0x33	RR	0x00000000
RxVeryLongErrors ²	Frames bigger than the larger of 2*MaxFrameSize and 50000 bits	Port_Index + 0x34	RR	0x00000000
RxRuntErrors	The total number of packets received that are less than 64 octets in length, but longer than or equal to 96 bit times. Note: The "ShortRunsThreshold" Register controls the byte count used to determine the difference between Runts and Shorts, and therefore controls which counter is incremented for a given frame size. This counter is only updated after receipt of two good frames.	Port_Index + 0x35	RR	0x00000000
RxShortErrors	The total number of packets received that are less than 96 bit times, which corresponds to a 4-byte frame with a well formed preamble and SFD. This counter indicates fragment sizes illegal in all modes, and is only fully updated after reception of a good frame following a fragment.	Port_Index + 0x36	RR	0x00000000
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2¹⁴-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2¹⁴-1. MaxFrameSize is determined by the settings in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 94.</p>				

**Table 60. MAC RX Statistics Registers (Addr: Port_Index + 0x20 - Port_Index + 0x39)
(Continued)**

Name	Description	Address	Type ¹	Default
RxCarrierExtend Error	Gigabit half-duplex event only Note: N/A - half-duplex only	Port_Index + 0x37	RR	0x00000000
RxSequenceErrors	Records the number of sequencing errors that occur. Note: The IXF1010 does not support fiber.	Port_Index + 0x38	RR	0x00000000
RxSymbolErrors	Records the number of symbol errors encountered. Note: The IXF1010 does not support fiber.	Port_Index + 0x39	RR	0x00000000
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write</p> <p>2. When sending in large frames, the counters can only deal with certain limits. The behavior of the LongErrors and VeryLongErrors counters is as follows: VeryLongErrors counts frames that are 2*MaxFrameSize, dependent on where the MaxFrameSize variable is set. If MaxFrameSize sets greater than half of the available count in RxOctetsBad (2¹⁴-1), VeryLongErrors is never incremented, but LongErrors is incremented. This is due to a limitation in the counter size, which means that an accurate count will not occur in the RxOctetsBAD counter if the frame is larger than 2¹⁴-1. MaxFrameSize is determined by the settings in the "Max Frame Size Register (Addr: Port_Index + 0x0F)" on page 94.</p>				

6.5.3 MAC TX Statistics Register Overview

The MAC TX Statistics Registers contain all the MAC transmit statistic counters and are cleared when read. The software must poll these registers to accumulate values and ensure that the counters do not wrap. The 32-bit counters wrap after approximately 30 seconds.

Table 61 covers the MAC TX Statistics Registers for all 10 MAC ports. The address is identical to the port number.

Table 61. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)

Name	Description	Address	Type ¹	Default
TXOctetsTotalOK	Counts the bytes transmitted in all legal frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted.	Port_Index + 0x40	RR	0x00000000
TXOctetsBad	Counts the bytes transmitted in all bad frames. The count includes all bytes from the destination MAC address to and including the CRC. The initial preamble and SFD bytes are not counted. TX underrun counted: The count is expected to match the number of bytes actually transmitted before the frame is discarded. TX CRC error counted: All bytes not sent with success are counted by this counter	Port_Index + 0x41	RR	0x00000000
TXUCPkts	The total number of unicast packets transmitted (excluding bad packets)	Port_Index + 0x42	RR	0x00000000
TXMCPkts	The total number of multicast packets transmitted (excluding bad packets) Note: This count includes pause control packets which are also counted in the TxPauseFrames Counter. Thus, these types of packets are counted twice. Take care when summing register counts for reporting MIB information.	Port_Index + 0x43	RR	0x00000000
TXBCPkts	The total number of broadcast packets transmitted (excluding bad packets)	Port_Index + 0x44	RR	0x00000000
TXPkts64Octets	The total number of packets transmitted (including bad packets) that were 64 octets in length. Incremented for tagged packets with a length of 64 bytes, including tag field	Port_Index + 0x45	RR	0x00000000
TXPkts65to127Octets	The total number of packets transmitted (including bad packets) that were [65-127] octets in length. Incremented for tagged packets with a length of 65 - 127 bytes, including tag field	Port_Index + 0x46	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

**Table 61. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)
(Continued)**

Name	Description	Address	Type ¹	Default
TXPkts128to255Octets	The total number of packets transmitted (including bad packets) that were [128-255] octets in length. Incremented for tagged packets with a length of 128 - 255 bytes, including tag field	Port_Index + 0x47	RR	0x00000000
TXPkts256to511Octets	The total number of packets transmitted (including bad packets) that were [256-511] octets in length. Incremented for tagged packets with a length of 256 - 511 bytes, including tag field	Port_Index + 0x48	RR	0x00000000
TXPkts512to1023Octets	The total number of packets transmitted (including bad packets) that were [512 - 1023] octets in length. Incremented for tagged packets with a length of 512 - 1023 bytes, including tag field	Port_Index + 0x49	RR	0x00000000
TXPkts1024to1518Octets	The total number of packets transmitted (including bad packets) that were [1024-1518] octets in length. Incremented for tagged packet with a length between 1024-1522, including the tag	Port_Index + 0x4A	RR	0x00000000
TXPkts1519toMaxOctets	The total number of packets transmitted (including bad packets) that were >1518 octets in length. Incremented for tagged packet with a length between 1523-max frame size, including the tag	Port_Index + 0x4B	RR	0x00000000
TXDeferred	Number of times the initial transmission attempt of a frame is postponed due to another frame already being transmitted on the Ethernet network. Note: N/A - half-duplex only	Port_Index + 0x4C	RR	0x00000000
TXTotalCollisions	Sum of all collision events Note: N/A - half-duplex only	Port_Index + 0x4D	RR	0x00000000
TXSingleCollisions	A count of successfully transmitted frames on a particular interface where the transmission is inhibited by exactly one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the MultipleCollisionFrames object. Note: N/A - half-duplex only	Port_Index + 0x4E	RR	0x00000000

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

**Table 61. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)
(Continued)**

Name	Description	Address	Type ¹	Default
TXMultipleCollisions	A count of successfully transmitted frames on a particular interface for which transmission is inhibited by more than one collision. A frame that is counted by an instance of this object is also counted by the corresponding instance of either the UnicastPkts, MulticastPkts, or BroadcastPkts, and is not counted by the corresponding instance of the SingleCollisionFrames object. Note: N/A - half-duplex only	Port_Index + 0x4F	RR	0x00000000
TXLateCollisions	The number of times a collision is detected on a particular interface later than 512 bit-times into the transmission of a packet. Such frame are terminated and discarded. Note: N/A - half-duplex only	Port_Index + 0x50	RR	0x00000000
TXExcessiveCollisionErrors	A count of frames, which collides 16 times and is then discarded by the MAC. Not effecting xMultipleCollisions Note: N/A - half-duplex only	Port_Index + 0x51	RR	0x00000000
TXExcessiveDeferralErrors	Number of times frame transmission is postponed more than 2*MaxFrameSize due to another frame already being transmitted on the Ethernet network. This causes the MAC to discard the frame. Note: N/A - half-duplex only	Port_Index + 0x52	RR	0x00000000
TXExcessiveLengthDrop	Frame transmissions aborted by the MAC because the frame is longer than maximum frame size. These frames are truncated by the MAC when the maximum frame size violation is detected by the MAC.	Port_Index + 0x53	RR	0x00000000
TXUnderrun	Internal TX error which causes the MAC to end the transmission before the end of the frame because the MAC did not get the needed data in time for transmission. The frames are lost and a fragment or a CRC error is transmitted.	Port_Index + 0x54	RR	0x00000000
TXTagged	Number of OK frames with VLAN tag. (Type field = 0x8100).	Port_Index + 0x55	RR	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

**Table 61. MAC TX Statistics Registers (Addr: Port_Index + 0x40 - Port_Index + 0x58)
(Continued)**

Name	Description	Address	Type ¹	Default
TXCRCError	Number of frames transmitted with a legal size, but with the wrong CRC field (also called FCS field)	Port_Index + 0x56	RR	0x00000000
TXPauseFrames	Number of pause MAC frames transmitted	Port_Index + 0x57	RR	0x00000000
TXFlowControlCollisions Send	Collisions generated on purpose on incoming frames, to avoid reception of traffic, while the port is in half-duplex and has flow control enabled, and do not have sufficient memory to receive more frames. Note: Due to the internal counting technique, a last frame might have to be transmitted after last flow control collision send to get the correct statistic. Note: N/A - half-duplex only	Port_Index + 0x58	RR	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.4 PHY Autoscans Registers

Table 62. PHY Control Register (Addr: Port_Index + 0x60)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0
15	Reset	PHY Soft Reset. Resets the PHY registers to their default value. This register bit self-clears after the reset is complete. 1 = PHY reset 0 = Normal Operation	RO	0
14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	RO	0
13	Speed Selection	0.6 (Speed<1> 0.13 (Speed<0>) 1 1 = Reserved 1 0 = 1000 Mbps (manual mode not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	RO	0 ²
12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process This register bit must be enabled for 1000BASE-T operation	RO	1
11	Power-Down	1 = Power-down 0 = Normal operation	RO	0
10	Isolate	1 = Electrically isolate PHY from GMII	RO	0
9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation	RO	0
8	Duplex Mode	1 = Full-duplex mode 0 = Half-duplex mode	RO	1 ²
7	Collision Test	1 = Enable COL signal test 0 = Disable COL signal test This register bit is ignored unless loopback is enabled (Register bit 0.14 = 1)	RO	0
6	Speed Selection 1000 Mbps	0.6 (Speed<1>) 0.13 (Speed<0>) 1 1 = Reserved 1 0 = 1000 Mbps (manual mode now allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	RO	0 ²
5:0	Reserved	Reserved	RO	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. This register is ignored if auto-negotiation is enabled.				

Table 63. PHY Status Register (Addr: Port_Index + 0x61)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0
15	100BASE-T4	1 = PHY able to operate in 100BASE-T4	RO	0
14	100BASE-X Full-Duplex	1 = PHY able to operate in 100BASE-X in full-duplex mode 0 = PHY not able to operate in 100BASE-X in full-duplex mode	RO	1
13	100BASE-X Half-Duplex	1 = PHY able to operate in 100BASE-X in half-duplex mode 0 = PHY not able to operate in 100BASE-X in half-duplex mode	RO	1
12	10 Mbps Full-Duplex	1 = PHY able to operate in 10 Mbps in full-duplex mode 0 = PHY not able to operate in 10 Mbps in full-duplex mode	RO	1
11	10 Mbps Half-Duplex	1 = PHY able to operate in 10 Mbps in half-duplex mode 0 = PHY not able to operate in 10 Mbps in half-duplex mode	RO	1
10	100BASE-T2 Full-Duplex	1 = PHY able to operate in 100BASE-T2 in full-duplex mode 0 = PHY not able to operate in 10BASE-T2 in full-duplex mode (not supported)	RO	0
9	100BASE-T2 Half-Duplex	1 = PHY able to operate in 100BASE-T2 in half-duplex mode 0 = PHY not able to operate in 100BASE-T2 in half-duplex mode	RO	0
8	Extended Status	1 = Extended status information in Register 15 0 = No extended status information in Register 15	RO	1
7	Reserved	Reserved	RO	0
6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	RO	0
5	Reserved	Reserved	RO	0
4	Remote Fault	1 = Remote fault condition detected	RO	0
3	Auto-Negotiation Ability	1 = PHY is able to perform auto-negotiation	RO	1
2	Link Status	1 = Link is up 0 = Link is down	RO	0
1	Jabber Detect	1 = Jabber condition detected 0 = Jabber condition not detected	RO	0
0	Extended Capability	1 = Extended register capabilities 0 = No extended register capabilities	RO	1

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 64. PHY ID 1 Register (Addr: Port_Index + 0x62)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0
15:0	PHY ID Number	The PHY identifier is composed of Register bits 18.3 of the OUI (Organizationally Unique Identifier)	RO	h0013
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 65. PHY ID 2 Register (Addr: Port_Index + 0x63)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0
15:10	PHY ID Number	The PHY identifier is composed of Register bits 24:19 of the OUI (Organizationally Unique Identifier)	RO	011110
9:4	Manufacturer's Model	Six bits containing the manufacturer's part number	RO	010000
3:0	Manufacturer's Revision Number	Four bits containing the manufacturer's revision number	RO	0000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 66. Auto-Negotiation Advertisement Register (Addr: Port_Index + 0x64)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0
15	Next Page	1 = Manual control of Next Page (software)	RO	0
14	Reserved	Reserved	RO	0
13	Remote Fault	1 = Remote fault 0 = No remote fault	RO	0
12	Reserved	Reserved	RO	0
11	ASM_DIR	Advertise Asymmetric Pause Direction Register bit. This register bit is used in conjunction with Pause (Register bit 4.10) 1 = Link partner is capable of asymmetric pause 0 = Link partner is not capable of asymmetric pause	RO	1
10	Pause	Advertise to link partner that Pause operation is desired (IEEE 802.3x Standard)	RO	0
9	100BASE-T4	1 = 100BASE-T4 capability is available 0 = 100BASE-T4 capability is not available	RO	0
8	100BASE-TX Full-Duplex	1 = DTE is 100BASE-TX, full-duplex mode capable 0 = DTE is not 100BASE-TX, full-duplex mode capable	RO	1
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 66. Auto-Negotiation Advertisement Register (Continued)(Addr: Port_Index + 0x64)

Bit	Name	Description	Type ¹	Default
7	100BASE-TX Half-Duplex	1 = DTE is 100BASE-TX, half-duplex mode capable 0 = DTE is not 100BASE-TX, half-duplex mode capable	RO	1
6	10BASE-T Full-Duplex	1 = DTE is 10BASE-T, full-duplex mode capable 0 = DTE is not 10BASE-T, full duplex mode capable	RO	1
5	10BASE-T Half-Duplex	1 = DTE is 10BASE-T, half-duplex mode capable 0 = DTE is not 10BASE-T, half-duplex mode capable	RO	1
4:0	Selector Field, S[4:0]	00001 = IEEE 802.3 00010 = IEEE 802.9 ISLAN-16T 00000 = Reserved for future auto-negotiation development 11111 = Reserved for future auto-negotiation development Unspecified or reserved combinations should not be transmitted Setting this field to a value other than 00001 will most likely cause auto-negotiation to fail	RO	00001
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 67. Auto-Negotiation Base Page Ability Register (Addr: Port_Index + 0x65)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0
15	Next Page	1 = Link partner has the ability to send multiple pages 0 = Link partner has no ability to send multiple pages	RO	N/A
14	Acknowledge	1 = Link partner has received Link Code Word from IXF1010 0 = Link partner has not received Link Code Word from IXF1010	RO	N/A
13	Remote Fault	1 = Remote fault 0 = No remote fault	RO	N/A
12	Reserved	Reserved	RO	0
11	ASM_DIR	Advertise Asymmetric Pause Direction Register bit. This register bit is used in conjunction with Pause (Register bit 4.10) 1 = Link partner is capable of asymmetric pause 0 = Link partner is not capable of asymmetric pause	RO	1
10	Link Partner Pause	Link partner wants to utilize Pause Operation as defined in IEEE 802.3x Standard	RO	0
9	1000BASE-T4	1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable	RO	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 67. Auto-Negotiation Base Page Ability Register (Addr: Port_Index + 0x65) (Continued)

Bit	Name	Description	Type ¹	Default
8	100BASE-TX Full-Duplex	1 = Link partner is 100BASE-TX, full-duplex mode capable 0 = Link partner is not 100BASE-TX, full-duplex mode capable	RO	1
7	100BASE-TX Half-Duplex	1 = Link partner is 100BASE-TX, half-duplex mode capable 0 = Link partner is not 100BASE-TX, half-duplex mode capable	RO	1
6	10BASE-T Full-Duplex	1 = Link partner is 10BASE-T, full-duplex mode capable 0 = Link partner is not 10BASE-T, full duplex mode capable	RO	1
5	10BASE-T Half-Duplex	1 = Link partner is 10BASE-T, half-duplex mode capable 0 = Link partner is not 10BASE-T, half-duplex mode capable	RO	1
4:0	Selector Field, S[4:0]	00001 = IEEE 802.3 00010 = IEEE 802.9 ISLAN-16T 00000 = Reserved for future auto-negotiation development 11111 = Reserved for future auto-negotiation development Unspecified or reserved combinations should not be transmitted Setting this field to a value other than 00001 will most likely cause auto-negotiation to fail	RO	00001
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 68. Auto-Negotiation Expansion Register (Addr: Port_Index + 0x66)

Bit	Name	Description	Type ¹	Default
31:6	Reserved	Reserved	RO	0
5	Base Page	This register bit indicates the status of the auto-negotiation variable, base page. It flags synchronization with the auto-negotiation state diagram allowing detection of interrupted links. This register bit is only used if Register bit 16.1 (alternate Next Page feature) is set. 1 = base_page = true 0 = base_page = false	RO	0
4	Parallel Detection Fault	1 = Parallel detection fault has occurred 0 = Parallel detection fault has not occurred	RO	0
3	Link Partner Next Page Able	1 = Link partner is Next Page able 0 = Link partner is not Next Page able	RO	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 68. Auto-Negotiation Expansion Register (Continued) (Addr: Port_Index + 0x66)

Bit	Name	Description	Type ¹	Default
2	Next Page Able	1 = Local device is Next Page able 0 = Local device is not Next Page able	RO	0
1	Page Received	Indicates that a new page has been received and the received code word has been loaded into Register 5 (base pages) or Register 8 (next pages) as specified in the IEEE 802.3 Standard. This bit clears on Read.	RO	0
0	Link Partner Auto-Negotiation Able	1 = Link partner is auto-negotiation able 0 = Link partner is not auto-negotiation able	RO	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 69. Auto-Negotiation Next Page Transmit Register (Addr: Port_Index + 0x67)

Bit	Name	Description	Type ¹	Default
31:16	Reserved	Reserved	RO	0
15	Next Page (NP)	1 = Additional Next Pages follow 0 = Last page	RO	0
14	Reserved	Reserved	RO	0
13	Message Page (MP)	1 = Message page 0 = Unformatted page	RO	0
12	Acknowledge 2	1 = Complies with message 0 = Cannot comply with message	RO	0
11	Toggle (T)	1 = Previous value of the transmitted Link Code Word was logic zero 0 = Previous value of the transmitted Link Code Word was logic one	RO	0
10:0	Message/ Unformatted Code Field	11-bit message code field See IEEE 802.3 Annex 28C	RO	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.5 Global Status and Configuration Register Overview

Table 70 through Table 76 on page 115 provide an overview of the Global Control and Status Registers.

Table 70. Port Enable Register (Addr: 0x500)

Bit	Name	Description	Type ¹	Default
Register Description: A control register for each port in the IXF1010. Port ID = bit position in the register. To make a port active, the bit must be set High (for example, port 4 active implies register value = 0001.0000). Setting the bit to 0 disables the port. The default state for this register is for all 10 ports to be active.				0x000003FF
31:10	Reserved	Reserved	RO	0x00000
9	Port 9 Enable	Port 9 0 = Disable 1 = Enable	R/W	1
8	Port 8 Enable	Port 8 0 = Disable 1 = Enable	R/W	1
7	Port 7 Enable	Port 7 0 = Disable 1 = Enable	R/W	1
6	Port 6 Enable	Port 6 0 = Disable 1 = Enable	R/W	1
5	Port 5 Enable	Port 5 0 = Disable 1 = Enable	R/W	1
4	Port 4 Enable	Port 4 0 = Disable 1 = Enable	R/W	1
3	Port 3 Enable	Port 3 0 = Disable 1 = Enable	R/W	1
2	Port 2 Enable	Port 2 0 = Disable 1 = Enable	R/W	1
1	Port 1 Enable	Port 1 0 = Disable 1 = Enable	R/W	1
0	Port 0 Enable	Port 0 0 = Disable 1 = Enable	R/W	1
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2.				

Table 71. Link LED Enable Register (Addr: 0x502)

Bit	Name	Description	Type ¹	Default
Register Description: Per-port bit should be set upon detection of link to enable proper operation of the link LEDs.				0x00000000
31:10	Reserved	Reserved	RO	0x000000
9	Link LED Enable Port 9	Port 9 link 0 = No link 1 = Link	R/W	0
8	Link LED Enable Port 8	Port 8 link 0 = No link 1 = Link	R/W	0
7	Link LED Enable Port 7	Port 7 link 0 = No link 1 = Link	R/W	0
6	Link LED Enable Port 6	Port 6 link 0 = No link 1 = Link	R/W	0
5	Link LED Enable Port 5	Port 5 link 0 = No link 1 = Link	R/W	0
4	Link LED Enable Port 4	Port 4 link 0 = No link 1 = Link	R/W	0
3	Link LED Enable Port 3	Port 3 link 0 = No link 1 = Link	R/W	0
2	Link LED Enable Port 2	Port 2 link 0 = No link 1 = Link	R/W	0
1	Link LED Enable Port 1	Port 1 link 0 = No link 1 = Link	R/W	0
0	Link LED Enable Port 0	Port 0 link 0 = No link 1 = Link	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 72. MDIO Soft Reset Register (Addr: 0x506)

Bit	Name	Description	Type ¹	Default
Register Description: Software activated reset of the MDIO module.				0x00000000
31:1	Reserved	Reserved	RO	0x00000000
0	MDIO Soft Reset	0 = Reset inactive 1 = Reset active	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 73. CPU Interface Register (Addr: 0x508)

Bit	Name	Description	Type ¹	Default
Register Description: CPU interface Endian select. This register allows the user to select the Endian of the CPU interface to allow various different CPUs to be connected to the IXF1010.				0x00000000
31:1	Reserved	Reserved	RO	0x00000000
0	Endian	0 = Little Endian 1 = Big Endian	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 74. LED Control Register (Addr: 0x509)

Bit	Name	Description	Type ¹	Default
Register Description: Globally selects and enables the LED mode.				0x00000000
31-2	Reserved	Reserved	RO	0x00000000
1	LED Enable	0 = Disable LEDs 1 = Enable LEDs	R/W	0
0	LED_SEL_MODE	0 = Enable LED Mode 0 for use with SGS Thompson M5450 LED driver 1 = (Default) LED Mode 1 for use with Standard Octal Shift Register	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 75. LED Flash Rate Register (Addr: 0x50A)

Bit	Name	Description	Type ¹	Default
Register Description: Globally selects and enables the flash rate.				0x00000000
31:3	Reserved	Reserved	RO	0x00000000
2:0	LED Flash Rate	000 = 100 ms flash rate 001 = 200 ms flash rate 010 = 300 ms flash rate 011 = 400 ms flash rate 100 = 500 ms flash rate 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				



Table 76. LED Fault Disable Register (Addr: 0x50B)

Bit	Name	Description	Type ¹	Default
Register Description: Per-port fault disable: Disables the LED flashing for local or remote faults				0x00000000
31:10	Reserved	Reserved	RO	0x00000000
9	LED Fault Disable Port 9	Port 9 0 = Fault enabled 1 = Fault disabled	R/W	0
8	LED Fault Disable Port 8	Port 8 0 = Fault enabled 1 = Fault disabled	R/W	0
7	LED Fault Disable Port 7	Port 7 0 = Fault enabled 1 = Fault disabled	R/W	0
6	LED Fault Disable Port 6	Port 6 0 = Fault enabled 1 = Fault disabled	R/W	0
5	LED Fault Disable Port 5	Port 5 0 = Fault enabled 1 = Fault disabled	R/W	0
4	LED Fault Disable Port 4	Port 4 0 = Fault enabled 1 = Fault disabled	R/W	0
3	LED Fault Disable Port 3	Port 3 0 = Fault enabled 1 = Fault disabled	R/W	0
2	LED Fault Disable Port 2	Port 2 0 = Fault enabled 1 = Fault disabled	R/W	0
1	LED Fault Disable Port 1	Port 1 0 = Fault enabled 1 = Fault disabled	R/W	0
0	LED Fault Disable Port 0	Port 0 0 = Fault enabled 1 = Fault disabled	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 77. JTAG ID Revision Register (Addr: 0x50C)

Bit	Name	Description	Type	Default
Register Description: The value of this register follows the same scheme as the device identification register found in the IEEE 1149.1 specification. The upper 4 bits correspond to silicon stepping. The next 16 bits store a Part ID Number. The next 11 bits contain a JEDEC Manufacturer ID. Bit zero = 1 if the chip is the first in a stack. The encoding scheme used for the Product ID field is implementation dependent.				0x203F2013
31:28	Version	Version	RO	0010
27:12	Part ID	Part ID	RO	0000001111110010
11:8	JEDEC Cont.	JEDEC Cont.	RO	0000
7:1	JEDEC ID	JEDEC ID	RO	0001001
0	Reserved	Reserved	RO	1
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.6 Global RX Block Register Overview

Table 78 through Table 82 on page 123 provide an overview of the RX Block Registers, which include the RX FIFO High and Low watermarks.

Table 78. RX FIFO High Watermark Ports 0 to 9 Registers (Addr: 0x580 - 0x589)

Name ²	Description	Address	Type ¹	Default
RX FIFO High Watermark Port 0	High watermark for RX FIFO port 0. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x580	R/W	0x00000740
RX FIFO High Watermark Port 1	High watermark for RX FIFO port 1. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x581	R/W	0x00000740
RX FIFO High Watermark Port 2	High watermark for RX FIFO port 2. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x582	R/W	0x00000740
RX FIFO High Watermark Port 3	High watermark for RX FIFO port 3. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x583	R/W	0x00000740
RX FIFO High Watermark Port 4	High watermark for RX FIFO port 4. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x584	R/W	0x00000740
RX FIFO High Watermark Port 5	High watermark for RX FIFO port 5. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x585	R/W	0x00000740
RX FIFO High Watermark Port 6	High watermark for RX FIFO port 6. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x586	R/W	0x00000740
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9): Bits 31:15 - Reserved and RO. Bits 14:0 - Described above.				

Table 78. RX FIFO High Watermark Ports 0 to 9 Registers (Addr: 0x580 - 0x589) (Continued)

Name ²	Description	Address	Type ¹	Default
RX FIFO High Watermark Port 7	High watermark for RX FIFO port 7. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x587	R/W	0x00000740
RX FIFO High Watermark Port 8	High watermark for RX FIFO port 8. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x588	R/W	0x00000740
RX FIFO High Watermark Port 9	High watermark for RX FIFO port 9. The default value is 1856 bytes. When the amount of data stored in the FIFO exceeds this value, a flow control command is sent to the corresponding TX MAC.	0x589	R/W	0x00000740
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. For all RX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9): Bits 31:15 - Reserved and RO. Bits 14:0 - Described above.				

Table 79. RX FIFO Low Watermark Ports 0 to 9 Registers (Addr: 0x58A - 0x593)

Name ²	Description	Address	Type ¹	Default
RX FIFO Low Watermark Port 0	Low watermark for RX FIFO port 0. The default value is 1840 bytes. When the port is in flow control, and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58A	R/W	0x00000730
RX FIFO Low Watermark Port 1	Low watermark for RX FIFO port 1. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58B	R/W	0x00000730
RX FIFO Low Watermark Port 2	Low watermark for RX FIFO port 2. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58C	R/W	0x00000730
RX FIFO Low Watermark Port 3	Low watermark for RX FIFO port 3. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58D	R/W	0x00000730
RX FIFO Low Watermark Port 4	Low watermark for RX FIFO port 4. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58E	R/W	0x00000730
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9): Bits 31:15 - Reserved and RO. Bits 14:0 - Described above.				

Table 79. RX FIFO Low Watermark Ports 0 to 9 Registers (Addr: 0x58A - 0x593) (Continued)

Name ²	Description	Address	Type ¹	Default
RX FIFO Low Watermark Port 5	Low watermark for RX FIFO port 5. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x58F	R/W	0x00000730
RX FIFO Low Watermark Port 6	Low watermark for RX FIFO port 6. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x590	R/W	0x00000730
RX FIFO Low Watermark Port 7	Low watermark for RX FIFO port 7. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x591	R/W	0x00000730
RX FIFO Low Watermark Port 8	Low watermark for RX FIFO port 8. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x592	R/W	0x00000730
RX FIFO Low Watermark Port 9	Low watermark for RX FIFO port 9. The default value is 1840 bytes. When the port is in flow control and the amount of data stored in the FIFO goes below this value, the flow control command is terminated in the corresponding TX MAC.	0x593	R/W	0x00000730
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. For all RX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9): Bits 31:15 - Reserved and RO. Bits 14:0 - Described above.</p>				

Table 80. RX FIFO Number of Frames Removed Ports 0 to 9 Registers (Addr: 0x594 - 0x59D)

Name ²	Description	Address	Type ¹	Default
RX FIFO Number of Frames Removed on Port 0	<p>This register counts all frames removed from the RX FIFO for port 0 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> The RX FIFO on this port becomes full Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x594	RR	0x00000000
RX FIFO Number of Frames Removed on Port 1	<p>This register counts all frames removed from the RX FIFO for port 1 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> The RX FIFO on this port becomes full Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x595	RR	0x00000000
RX FIFO Number of Frames Removed on Port 2	<p>This register counts all frames removed from the RX FIFO for port 2 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> The RX FIFO on this port becomes full Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x596	RR	0x00000000
RX FIFO Number of Frames Removed on Port 3	<p>This register counts all frames removed from the RX FIFO for port 3 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> The RX FIFO on this port becomes full Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x597	RR	0x00000000
RX FIFO Number of Frames Removed on Port 4	<p>This register counts all frames removed from the RX FIFO for port 4 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> The RX FIFO on this port becomes full Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x598	RR	0x00000000
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write. 2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9): Bits 31:22 - Reserved and RO. Bits 21:0 - Described above.</p>				

Table 80. RX FIFO Number of Frames Removed Ports 0 to 9 Registers (Addr: 0x594 - 0x59D)

Name ²	Description	Address	Type ¹	Default
RX FIFO Number of Frames Removed on Port 5	<p>This register counts all frames removed from the RX FIFO for port 5 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) • Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x599	RR	0x00000000
RX FIFO Number of Frames Removed on Port 6	<p>This register counts all frames removed from the RX FIFO for port 6 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) • Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x59A	RR	0x00000000
RX FIFO Number of Frames Removed on Port 7	<p>This register counts all frames removed from the RX FIFO for port 7 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) • Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x59B	RR	0x00000000
RX FIFO Number of Frames Removed on Port 8	<p>This register counts all frames removed from the RX FIFO for port 8 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) • Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x59C	RR	0x00000000
RX FIFO Number of Frames Removed on Port 9	<p>This register counts all frames removed from the RX FIFO for port 9 by meeting one of the following conditions:</p> <ul style="list-style-type: none"> • The RX FIFO on this port becomes full • Frames are removed in conjunction with the RX FIFO Errored Frame Drop Enable Register (Table 81 on page 122) • Frames are greater than the MaxFrameSize (Table 51 on page 94) 	0x59D	RR	0x00000000
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write. 2. For all Number of Frames Removed Registers, the following bit definitions apply to all ports (0:9): Bits 31:22 - Reserved and RO. Bits 21:0 - Described above.</p>				

Table 81. RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F)

Bit	Name	Description	Type ¹	Default
Register Description: This register is used in conjunction with the RX Packet Filter Control Register bits to select whether errored or filtered frames are to be dropped.				0x00000000
31:10	Reserved	Reserved	RO	0x00000000
9	RX FIFO Errored Frame Drop Enable Port 9	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 9: 0 = Do not drop frames 1 = Drop frames	R/W	0
8	RX FIFO Errored Frame Drop Enable Port 8	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 8: 0 = Do not drop frames 1 = Drop frames	R/W	0
7	RX FIFO Errored Frame Drop Enable Port 7	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 7: 0 = Do not drop frames 1 = Drop frames	R/W	0
6	RX FIFO Errored Frame Drop Enable Port 6	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 6: 0 = Do not drop frames 1 = Drop frames	R/W	0
5	RX FIFO Errored Frame Drop Enable Port 5	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 5: 0 = Do not drop frames 1 = Drop frames	R/W	0
4	RX FIFO Errored Frame Drop Enable Port 4	These bits are used in conjunction with the "RX Packet Filter Control Register (Addr: Port_Index + 0x19)" bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 4: 0 = Do not drop frames 1 = Drop frames	R/W	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 81. RX FIFO Errored Frame Drop Enable Register (Addr: 0x59F) (Continued)

Bit	Name	Description	Type ¹	Default
3	RX FIFO Errored Frame Drop Enable Port 3	These bits are used in conjunction with the “RX Packet Filter Control Register (Addr: Port_Index + 0x19)” bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 3: 0 = Do not drop frames 1 = Drop frames	R/W	0
2	RX FIFO Errored Frame Drop Enable Port 2	These bits are used in conjunction with the “RX Packet Filter Control Register (Addr: Port_Index + 0x19)” bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 2: 0 = Do not drop frames 1 = Drop frames	R/W	0
1	RX FIFO Errored Frame Drop Enable Port 1	These bits are used in conjunction with the “RX Packet Filter Control Register (Addr: Port_Index + 0x19)” bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 1: 0 = Do not drop frames 1 = Drop frames	R/W	0
0	RX FIFO Errored Frame Drop Enable Port 0	These bits are used in conjunction with the “RX Packet Filter Control Register (Addr: Port_Index + 0x19)” bits, allowing the user to select whether errored or filtered frames are to be dropped or not. Port 0: 0 = Do not drop frames 1 = Drop frames	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 82. RX FIFO Overflow Event Register (Addr: 0x5A0)

Bit	Name	Description	Type ¹	Default
Register Description: This register provides a status if a FIFO-full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x00000000
9	RX FIFO Overflow Event Port 9	Port 9 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
8	RX FIFO Overflow Event Port 8	Port 8 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
7	RX FIFO Overflow Event Port 7	Port 7 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

Table 82. RX FIFO Overflow Event Register (Addr: 0x5A0) (Continued)

Bit	Name	Description	Type ¹	Default
6	RX FIFO Overflow Event Port 6	Port 6 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
5	RX FIFO Overflow Event Port 5	Port 5 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
4	RX FIFO Overflow Event Port 4	Port 4 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
3	RX FIFO Overflow Event Port 3	Port 3 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
2	RX FIFO Overflow Event Port 2	Port 2 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1	RX FIFO Overflow Event Port 1	Port 1 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
0	RX FIFO Overflow Event Port 0	Port 0 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.7 TX Block Register Overview

Table 83 through Table 88 on page 132 provide an overview of the TX Block Registers, which include the TX FIFO High and Low Watermark.

Table 83. TX FIFO High Watermark Ports 0 to 9 (Addr: 0x600 - 0x609)

Name ²	Description	Address	Type ¹	Default
TX FIFO High Watermark Port 0	High watermark for TX FIFO port 0. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x600	R/W	0x00000630
TX FIFO High Watermark Port 1	High watermark for TX FIFO port 1. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x601	R/W	0x00000630
TX FIFO High Watermark Port 2	High watermark for TX FIFO port 2. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x602	R/W	0x00000630
TX FIFO High Watermark Port 3	High watermark for TX FIFO port 3. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x603	R/W	0x00000630
TX FIFO High Watermark Port 4	High watermark for TX FIFO port 4. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x604	R/W	0x00000630
TX FIFO High Watermark Port 5	High watermark for TX FIFO port 5. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x605	R/W	0x00000630
TX FIFO High Watermark Port 6	High watermark for TX FIFO port 6. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x606	R/W	0x00000630
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9): Bits 31:13 - Reserved and RO. Bits 12:0 - Described above.				

Table 83. TX FIFO High Watermark Ports 0 to 9 (Addr: 0x600 - 0x609) (Continued)

Name ²	Description	Address	Type ¹	Default
TX FIFO High Watermark Port 7	High watermark for TX FIFO port 7. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x607	R/W	0x00000630
TX FIFO High Watermark Port 8	High watermark for TX FIFO port 8. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x608	R/W	0x00000630
TX FIFO High Watermark Port 9	High watermark for TX FIFO port 9. The default value is 1584 bytes. When the amount of data stored in the FIFO exceeds this value, the TX FIFO indicates "SATISFIED." This implies further up in the system that no more data must be sent to this port.	0x609	R/W	0x00000630
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. For all TX FIFO High Watermark Registers, the following bit definitions apply to all ports (0:9): Bits 31:13 - Reserved and RO. Bits 12:0 - Described above.				

Table 84. TX FIFO Low Watermark Ports 0 to 9 (Addr: 0x60A - 0x613)

Name ²	Description	Address	Type ¹	Default
TX FIFO Low Watermark Port 0	Low watermark for TX FIFO port 0. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60A	R/W	0x000001D0
TX FIFO Low Watermark Port 1	Low watermark for TX FIFO port 1. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60B	R/W	0x000001D0
TX FIFO Low Watermark Port 2	Low watermark for TX FIFO port 2. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60C	R/W	0x000001D0
TX FIFO Low Watermark Port 3	Low watermark for TX FIFO port 3. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60D	R/W	0x000001D0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9): Bits 31:13 - Reserved and RO. Bits 12:0 - Described above.				

Table 84. TX FIFO Low Watermark Ports 0 to 9 (Addr: 0x60A - 0x613) (Continued)

Name ²	Description	Address	Type ¹	Default
TX FIFO Low Watermark Port 4	Low watermark for TX FIFO port 4. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60E	R/W	0x000001D0
TX FIFO Low Watermark Port 5	Low watermark for TX FIFO port 5. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x60F	R/W	0x000001D0
TX FIFO Low Watermark Port 6	Low watermark for TX FIFO port 6. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x610	R/W	0x000001D0
TX FIFO Low Watermark Port 7	Low watermark for TX FIFO port 7. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x611	R/W	0x000001D0
TX FIFO Low Watermark Port 8	Low watermark for TX FIFO port 8. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x612	R/W	0x000001D0
TX FIFO Low Watermark Port 9	Low watermark for TX FIFO port 9. The default value is 464 bytes. When the amount of data falls below this value, the TX FIFO status indicates "STARVING". This implies further up in the system that more data must be sent to this port to prevent an underrun.	0x613	R/W	0x000001D0
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. For all TX FIFO Low Watermark Registers, the following bit definitions apply to all ports (0:9): Bits 31:13 - Reserved and RO. Bits 12:0 - Described above.</p>				

Table 85. TX FIFO MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D)

Name ²	Description ³	Address	Type ¹	Default
TX FIFO MAC Transfer Threshold Port 0	<p>Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x614	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 1	<p>Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, and the threshold is set in increments of 8-byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x615	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 2	<p>Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x616	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 3	<p>Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x617	R/W	0x00000100
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write</p> <p>2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9): Bits 31:13 - Reserved and RO. Bits 12:0 - Described above.</p> <p>3. For proper operation of the IXF1010, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.</p>				

Table 85. TX FIFO MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D) (Continued)

Name ²	Description ³	Address	Type ¹	Default
TX FIFO MAC Transfer Threshold Port 4	<p>Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x618	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 5	<p>Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x619	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 6	<p>Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x61A	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 7	<p>Sets the value at which the FIFO begins to transfer data to MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x61B	R/W	0x00000100
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write</p> <p>2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9): Bits 31:13 - Reserved and RO. Bits 12:0 - Described above.</p> <p>3. For proper operation of the IXF1010, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.</p>				

Table 85. TX FIFO MAC Transfer Threshold Ports 0 to 9 (Addr: 0x614 - 0x61D) (Continued)

Name ²	Description ³	Address	Type ¹	Default
TX FIFO MAC Transfer Threshold Port 8	<p>Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x61C	R/W	0x00000100
TX FIFO MAC Transfer Threshold Port 9	<p>Sets the value at which the FIFO begins to transfer data to the MAC. The bottom 3 bits of this register are ignored, thus the threshold is set in increments of 8 byte steps.</p> <p>If this register is set above the standard packet size (including the 8-byte round-up), full packet transfers from the FIFO only are allowed.</p> <p>Transfer begins when either the count value in this register is exceeded or an End-of-Frame is received.</p>	0x61D	R/W	0x00000100
<p>1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write</p> <p>2. For all MAC Transfer Threshold Registers, the following bit definitions apply to all ports (0:9): Bits 31:13 - Reserved and RO. Bits 12:0 - Described above.</p> <p>3. For proper operation of the IXF1010, the MAC transfer threshold must be set to greater than the MaxBurst1 on the SPI4-2.</p>				

Table 86. TX FIFO Overflow Event Register (Addr: 0x61E)

Bit	Name	Description	Type ¹	Default
Register Description: This register provides status that a FIFO- full situation has occurred (for example, a FIFO overflow). The bit position equals the port number. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x00000000
9	TX FIFO Overflow Event Port 9	Port 9 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
8	TX FIFO Overflow Event Port 8	Port 8 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
7	TX FIFO Overflow Event Port 7	Port 7 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
6	TX FIFO Overflow Event Port 6	Port 6 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
5	TX FIFO Overflow Event Port 5	Port 5 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
4	TX FIFO Overflow Event Port 4	Port 4 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
3	TX FIFO Overflow Event Port 3	Port 3 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
2	TX FIFO Overflow Event Port 2	Port 2 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1	TX FIFO Overflow Event Port 1	Port 1 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
0	TX FIFO Overflow Event Port 0	Port 0 1 = FIFO overflow event occurred 0 = FIFO overflow event did not occur	RR	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 87. TX FIFO Info Out-of-Sequence Register (Addr: 0x621)

Bit	Name	Description	Type ¹	Default
Register Description: This register signals when out-of-sequence data is detected in the TX FIFO. Events such as SOP followed by another SOP cause this bit to be set and remain so until read. This register is cleared on Read.				0x00000000
31:10	Reserved	Reserved	RO	0x00000000
9	TX FIFO Info Out-of-Sequence Port 9	Port 9 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
8	TX FIFO Info Out-of-Sequence Port 8	Port 8 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
7	TX FIFO Info Out-of-Sequence Port 7	Port 7 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
6	TX FIFO Info Out-of-Sequence Port 6	Port 6 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
5	TX FIFO Info Out-of-Sequence Port 5	Port 5 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
4	TX FIFO Info Out-of-Sequence Port 4	Port 4 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
3	TX FIFO Info Out-of-Sequence Port 3	Port 3 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
2	TX FIFO Info Out-of-Sequence Port 2	Port 2 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
1	TX FIFO Info Out-of-Sequence Port 1	Port 1 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
0	TX FIFO Info Out-of-Sequence Port 0	Port 0 1 = FIFO out-of-sequence event occurred 0 = FIFO out-of-sequence event did not occur	RR	0
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 88. TX FIFO Number of Frames Removed Ports 0-9 (Addr: 0x622 - 0x62B)

Name	Description	Address	Type ¹	Default
TX FIFO Number of Frames Removed on Port 0	This register counts the number of frames removed on port 0 due to a TX FIFO overflow.	0x622	RR	0x00000000
TX FIFO Number of Frames Removed on Port 1	This register counts the number of frames removed on port 1 due to a TX FIFO overflow.	0x623	RR	0x00000000
TX FIFO Number of Frames Removed on Port 2	This register counts the number of frames removed on port 2 due to a TX FIFO overflow.	0x624	RR	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 88. TX FIFO Number of Frames Removed Ports 0-9 (Addr: 0x622 - 0x62B) (Continued)

Name	Description	Address	Type ¹	Default
TX FIFO Number of Frames Removed on Port 3	This register counts the number of frames removed on port 3 due to a TX FIFO overflow.	0x625	RR	0x00000000
TX FIFO Number of Frames Removed on Port 4	This register counts the number of frames removed on port 4 due to a TX FIFO overflow.	0x626	RR	0x00000000
TX FIFO Number of Frames Removed on Port 5	This register counts the number of frames removed on port 5 due to a TX FIFO overflow.	0x627	RR	0x00000000
TX FIFO Number of Frames Removed on Port 6	This register counts the number of frames removed on port 6 due to a TX FIFO overflow.	0x628	RR	0x00000000
TX FIFO Number of Frames Removed on Port 7	This register counts the number of frames removed on port 7 due to a TX FIFO overflow.	0x629	RR	0x00000000
TX FIFO Number of Frames Removed on Port 8	This register counts the number of frames removed on port 8 due to a TX FIFO overflow.	0x62A	RR	0x00000000
TX FIFO Number of Frames Removed on Port 9	This register counts the number of frames removed on port 9 due to a TX FIFO overflow.	0x62B	RR	0x00000000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

6.5.8 MDIO Block Register Overview

Table 89 through Table 92 on page 135 provide an overview of the MDIO Block Registers

Table 89. MDI Single Command Register (Addr: 0x680)

Bit	Name	Description	Type ¹	Default
Register Description: Provides the CPU with the ability to perform single MDIO Read and Write access				0x00000000
31:21	Reserved	Reserved	RO	000000000 0
20	MDI Command	Performs an MDIO access. When set, this bit self clears upon completion of the access. 1 = Performs an MDIO access 0 = MDIO access completed	R/W	0
19:18	Reserved	Reserved	RO	00
17:16	OP Code	MDIO Op Code 00 = Reserved 01 = Write Access 10 = Read Access 11 = Reserved	R/W	01
15:13	Reserved	Reserved	RO	000
12:8	PHY Address	Address of external PHY device	R/W	00000
7:5	Reserved	Reserved	RO	000
4:0	REG Address	Address of register within external PHY	R/W	00000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 90. MDI Single Read and Write Data Register (Addr: 0x681)

Bit	Name	Description	Type ¹	Default
Register Description: Allows for MDIO Read/Write capability.				0x00000000
31:16	MDI Read Data	Read Data from external device	RO	0x0000
15: 0	MDI Write Data	Write data for MDI Writes to the external device.	R/W	0x0000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 91. Autoscan PHY Address Enable Register (Addr: 0x682)

Bit	Name	Description	Address	Type ¹	Default
31:0	Autoscan PHY Address Enable	Defines valid PHY addresses Each bit enables the corresponding PHY address for autoscan operation: 1 = Enable this PHY Address 0 = Disable this PHY Address	0x682	R/W	0x000003FF
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write					



Table 92. MDI Control Register (Addr: 0x683)

Bit	Name	Description	Type ¹	Default
Register Description: MDI Control Register				0x00000000
31:4	Reserved	Reserved	RO	0x00000000
3	MDIO in Prog	Status of MDIO single transaction 1 = MDIO single command in progress 0 = MDIO single command not in progress (Default)	R/W	0
2	MDIO in Prog Enable	Enable the MDIO IN PROG Register bit 1 = MDIO IN PROG Register bit enabled 0 = MDIO IN PROG Register bit disabled (Default)	R/W	0
1	Autoscan Enable	Enable continuous Autoscan operation 1 = Autoscan enabled 0 = Autoscan disabled (default)	R/W	0
0	MDC Speed	Selects speed of MDC clock 1 = MDC runs at 17.8 MHz 0 = MDC runs at 2.5 MHz	R/W	0

1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write

6.5.9 SPI4-2 Block Register Overview

Table 93 through Table 96 on page 138 provide an overview of the SPI4-2 Block Registers.

Table 93. SPI4-2 RX Burst Size Register (Addr: 0x700)

Bit	Name	Description	Type ¹	Default
Register Description: SPI4-2 RX interface start-up parameters for burst size.				0x00060002
31	idles	1 = Inserts four idle control words between each burst. (This occurs not only on an EOP, but also at the end of every MaxBurst1 or MaxBurst2.) 0 = Zero idle insertion between transfer bursts.	R/W	0x0
30:25	Reserved	Reserved	RO	0x00
24:16	MaxBurst1	Maximum number of 16-byte blocks that the FIFO in the receive path, external to IXF1010, can accept when the FIFO Status channel indicates STARVING.	R/W	0x006
15:9	Reserved	Reserved	RO	0x00
8:0	MaxBurst2	Maximum number of 16-byte blocks that the FIFO in the receive path, external to the IXF1010, can accept when the FIFO Status channel indicates HUNGRY.	R/W	0x002
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write				

Table 94. SPI4-2 RX Training Register (Addr: 0x701)

Bit	Name	Description	Type ¹	Default
Register Description: SPI4-2 RX interface start-up parameters for training sequences				0x00000000
31:24	Reserved	Reserved	RO	0x00
23:16	REP_T	Number of repetitions of the data training sequence that must be scheduled every DATA_MAX_T cycles	R/W	0x00
15:0	DATA_MAX_T ²	Maximum interval (in number of cycles) between scheduling of training sequences on receive data path interface An all zero value disables periodic training sequences.	R/W	0x0000
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. The value of DATA_MAX_T is the Most Significant 16 bits of a 24-bit counter value. The Least Significant 8 bits are always 0x00. This allows for a much larger DATA_MAX_T time-out period and provides a more than adequate granularity of selection.				

Table 95. SPI4-2 RX Calendar Register (Addr: 0x702)

Bit	Name	Description	Type ¹	Default Value
Register Description: SPI4-2 RX interface start-up parameters for FIFO status calendar operation.				0x00010300
31:30	RX Train Test Modes	00 = Normal mode. 01 = Do not enter training based on a repeating "11" pattern on RSTAT[1:0] 1x = Train continuously	R/W	0x0
29	RSCLK_invert	1 = The FIFO status is captured on the falling edge of RSCLK 0 = The FIFO status is captured on the rising edge of the RSCLK as per the SPI4-2 specification.	R/W	0
28	TSCLK_invert	1 = The FIFO status is launched on the falling edge of TSCLK 0 = The FIFO status is launched on the rising edge of the TSCLK as per the SPI4-2 specification.	R/W	0
27:21	Reserved	Reserved	RO	0x000
20	DIP2_Error	Set based on an incorrect RX DIP2 result. This bit is cleared upon a read	RR	0x0
19:16	DIP-2_Thr	Defines how many consecutive correct DIP-2s are required to disable sending of training sequences on the RX SPI4-2.	R/W	0x1
15:14	Reserved	Reserved	RO	0x0
13	RX SPI4 Sync	1 = RX SPI4 Out Of Training (RDAT = idles). 0 = RX SPI4 In Training (RDAT = training).	RO	0
12	TX SPI4 Sync	1 = The TX SPI4-2 has received the valid training patterns on TDAT and is now sending a 10 port Calendar on TSAT with valid FIFO information. 0 = TX SPI4-2 Calendar is in constant Framing.	RO	0
11:8	Loss_of_Sync	Loss-of-Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and restart training sequences.	R/W	0x3
7:4	Reserved	Reserved	RO	0x0
3:0	CAL_M	Number of times FIFO status for ports 0 through 9 repeat between framing and DIP-2 cycles over the default value of 1.	R/W	0x0
1. R0 = Read Only; RR = Clear on Read; W = Write only; R/W = Read/Write				

Table 96. SPI4-2 TX Synchronization Register (Addr: 0x703)

Bit	Name	Description	Type ¹	Default
Register Description: SPI4-2 synchronization DIP-4 counters.				0x00000420
31:16	DIP4_Errors	DIP4_Errors is the total number of DIP4 errors detected since this register was last read.	RR	0x0000
15:8	DIP4_UnLock ²	DIP-4_Unlock is a SPI4-2 parameter specifying the number of incorrect DIP4 fields to be detected to declare loss of synchronization and drive the TSTAT[1:0] bus with framing.	R/W	0x04
7:0	DIP4_Lock	Number of consecutive correct DIP4 results to achieve synchronization and end training	R/W	0x20
1. RO = Read Only; RR = Clear on Read; W = Write; R/W = Read/Write 2. When Periodic Training is enabled, the actual count of DIP4 errors required to lose synchronization is 1 less than the programmed value in this register. Therefore, this value should always be programmed to be 1 more than the desired value and should never be programmed to either 0 or 1.				

7.0 Package Overview

CBGA packages are suited for applications requiring high I/O counts and high electrical performance. They are recommended for high-power applications, having high noise immunity requirements.

7.1 Features

- Flip chip die attach; surface mount second-level interconnect
- High electrical performance
- High I/O counts
- Area array I/O options
- Multiple power zone offering supports core and four additional voltages
- JEDEC-compliant package

7.2 Package Specifics for the IXF1010

The IXF1010 uses the following packaging (see [Figure 39, “IXF1010 552-Ceramic Ball Grid Array \(CBGA\) Package Specification”](#) on page 141):

- 552-ball CBGA
- Ball pitch of 1.0 mm
- Overall package dimensions of 25 mm x 25 mm

Figure 39. IXF1010 552-Ceramic Ball Grid Array (CBGA) Package Specification

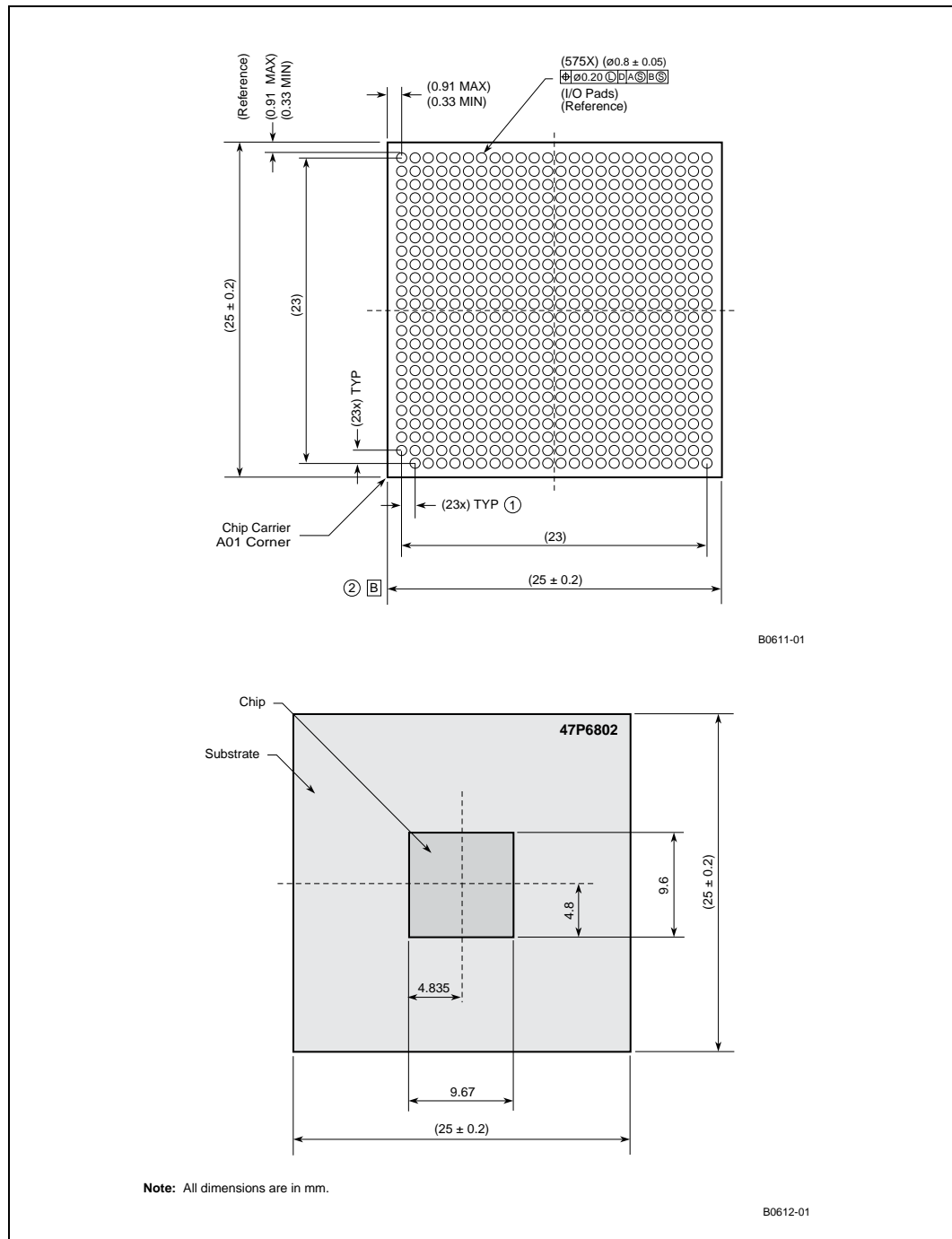
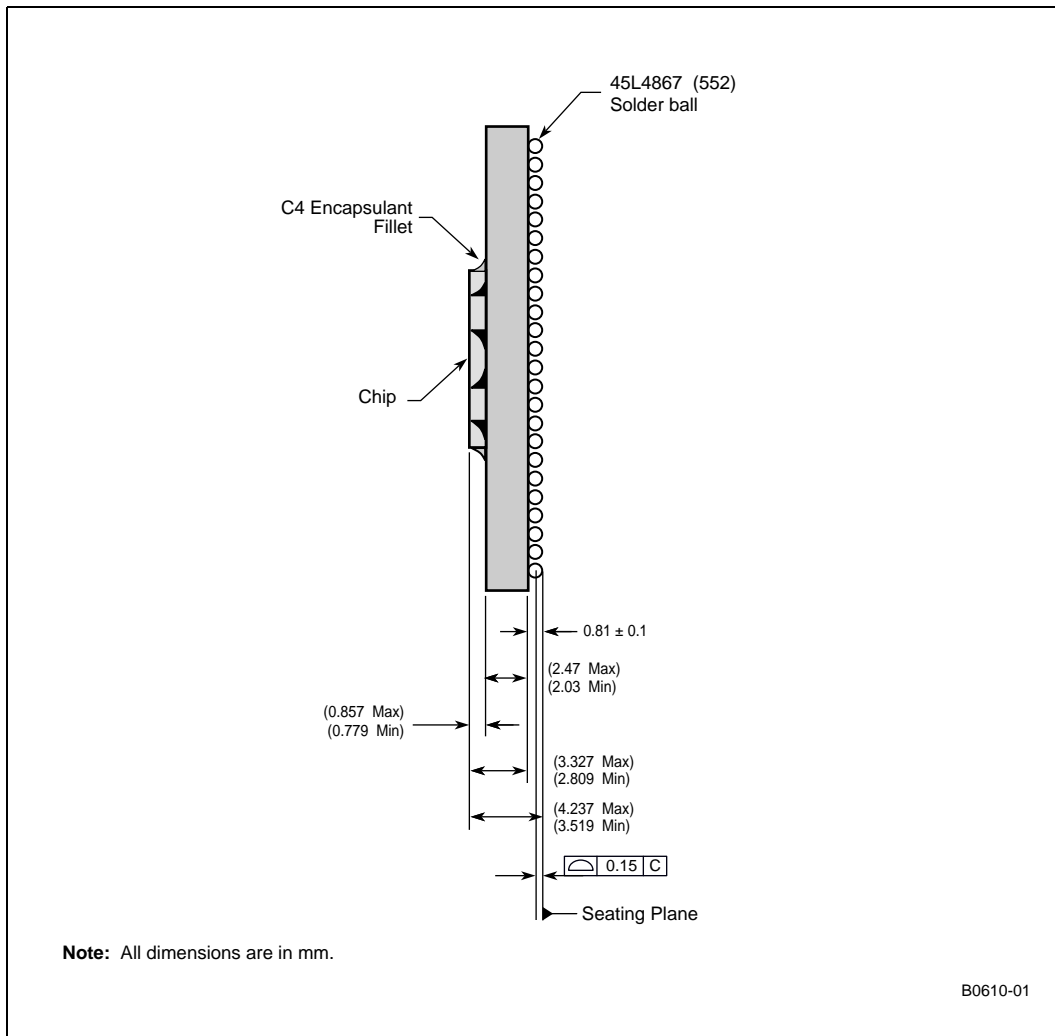


Figure 40. IXF1010 CBGA Package Side View Diagram



8.0 Product Ordering Information

Table 97. Product Information

Number	Revision	Qualification	MM Number	Ship Media
HFIXF1010CC.A2 QE000	A2	Q	848596	Tray
HF1010CC.A2 SMPL QE000	A2	Q	849908	Tray

Figure 41. Ordering Information - Sample

