Signetics

FAST Products

FAST 74F597, 74F598
Shift Registers

74F597 8-Bit Shift Register with Input Latches
74F598 8-Bit Shift Register with Input Latches (3-State)
Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F597	120MHz	75mA
74F598	120MHz	75mA

FEATURES

- **High impedance NPN base input for reduced loading (20μA in High and Low states)**
- **8-bit Parallel storage register**
- **Shift register has asynchronous direct overriding load and reset**
- **Guaranteed shift frequency DC to 120MHz**
- **Parallel 3-State I/O, Storage register inputs**
- **Shift register outputs-'F598**

DESCRIPTION

The 74F597 consists of an 8-bit storage register feeding a parallel-in, serial out 8-bit shift register. The storage register and shift register have separate positive edge triggered clocks. The shift register also has asynchronous direct load (from storage) and reset inputs.

The 74F598 consists of an 8-bit storage register feeding a parallel/serial-in, parallel/serial out 8-bit shift register. Both the storage register and shift register have positive edge triggered clocks. The shift register also has asynchronous direct load (from storage) and reset inputs. The 'F598 has 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data input.

ORDERING INFORMATION

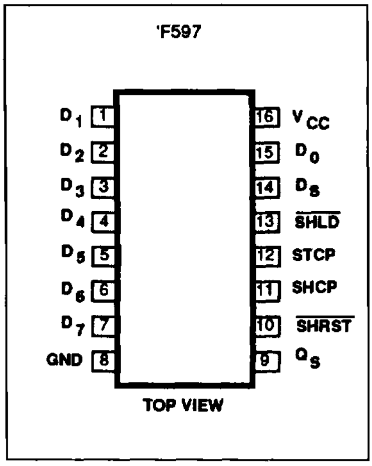
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F597N
20-Pin Plastic DIP	N74F598N
16-Pin Plastic SO	N74F597D
20-Pin Plastic SOL	N74F598D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

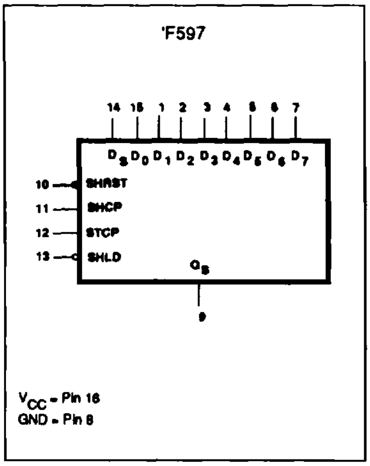
	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F597	D_S	Serial data input	1.0/0.033	20μA/20μA
	D_0-D_7	Parallel data inputs	1.0/0.033	20μA/20μA
	SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
	STCP	Storage register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20μA/20μA
	$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
	Q_S	Serial data output	50/33	1.0mA/20mA
'F598	I/O_n	Parallel data inputs	1.0/0.033	20μA/20μA
	D_{S0}, D_{S1}	Serial data inputs	1.0/0.033	20μA/20μA
	SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{STCP}$	Storage register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{SHCPEN}$	Shift register clock pulse enable input	1.0/0.033	20μA/20μA
	$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20μA/20μA
	$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
	S	Serial data selector input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
	Q_S	Serial data output	50/33	1.0mA/20mA
	I/O_n	Parallel data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

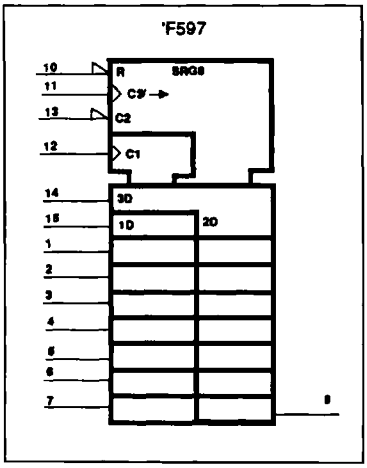
PIN CONFIGURATION



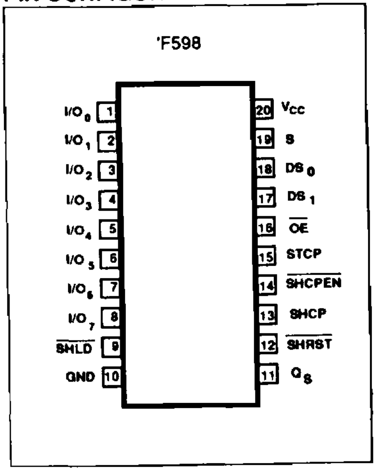
LOGIC SYMBOL



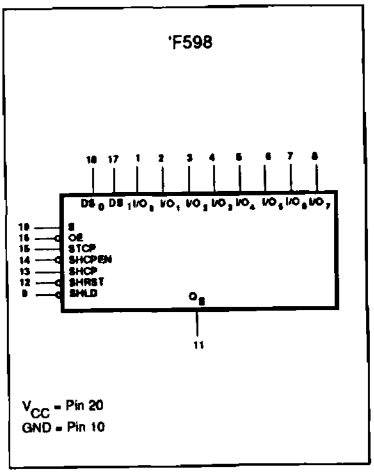
LOGIC SYMBOL(IEEE/IEC)



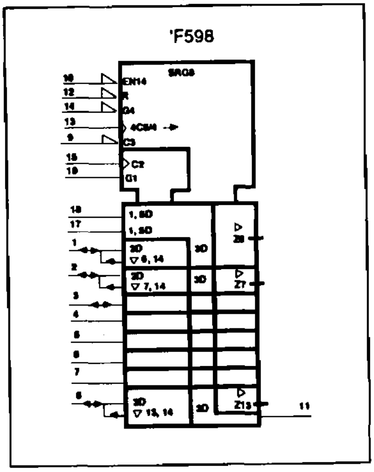
PIN CONFIGURATION



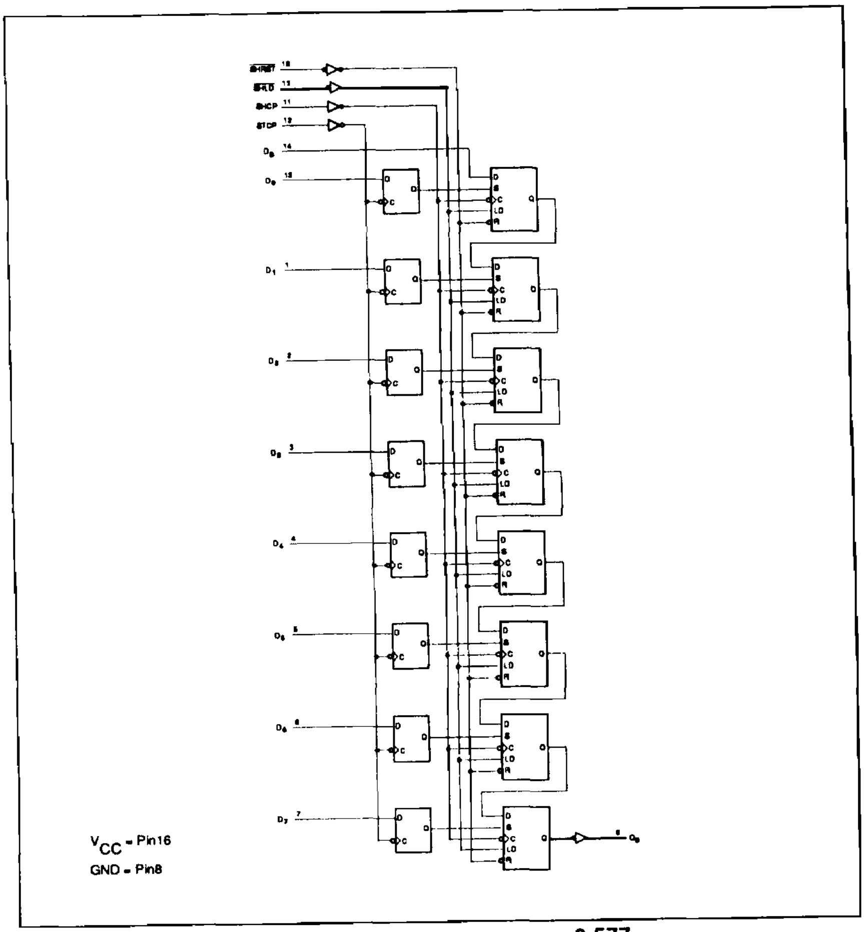
LOGIC SYMBOL



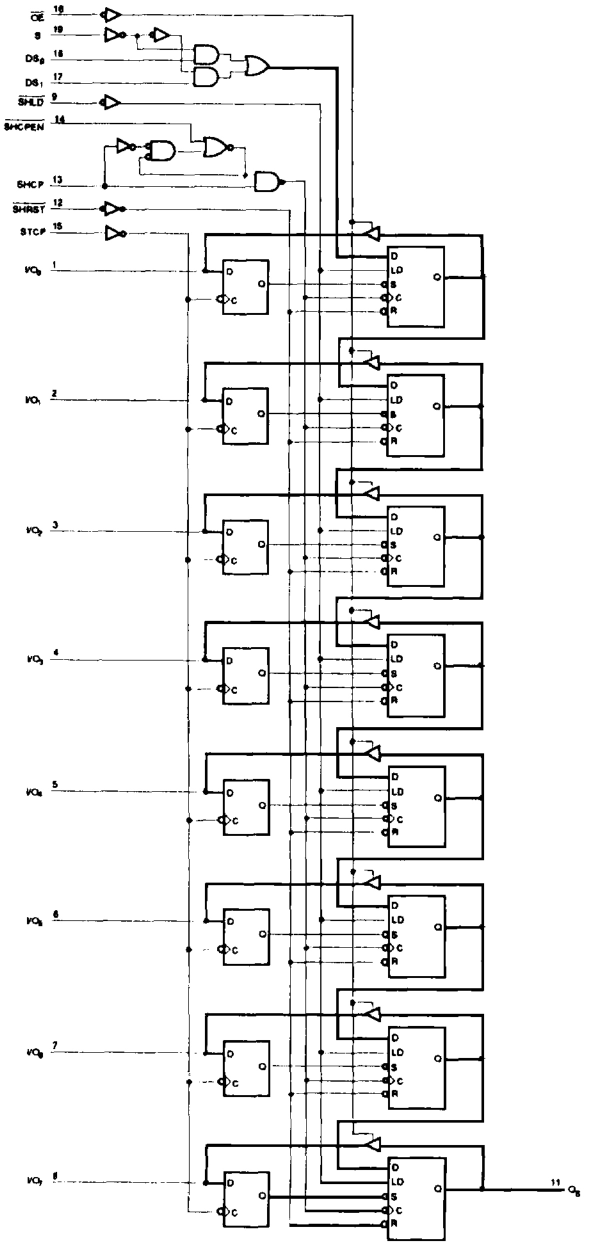
LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM for 'F597



LOGIC DIAGRAM FOR 'F598



V_{CC} = Pin 20
GND = Pin 10

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		I/O_0- I/O_7	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_S			-1	mA
		I/O_0- I/O_7			-3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		I/O_0- I/O_7			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_S		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
						±5%V_{CC}	2.7	3.4		V
		I/O_n			I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MI	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
						±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others		V_{CC} = 0.0V, V_I = 7.0V					100	μA
		I/O_n		V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	μA
$I_{OZH}+I_{IH}$	Off-state output current High-level voltage applied	I/O_n only		V_{CC} = MAX, V_O= 2.7V					70	μA
$I_{OZL}+I_{IL}$	Off-state output current Low-level voltage applied			V_{CC} = MAX, V_O= 0.5V					-70	μA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	'F597	I_{CCH}	V_{CC} = MAX				45	70	mA
			I_{CCL}					48	75	mA
		'F598	I_{CCH}					75	90	mA
			I_{CCL}					78	95	mA
			I_{CCZ}					85	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 'F597

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximun clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to Q_S	Waveform 3	4.0	8.0	10.0	4.0	11.0	ns

AC SETUP REQUIREMENTS for 'F597

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_S to SHCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_S to SHCP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low STCP to $\overline{SHLD}$	Waveform 4	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low STCP to $\overline{SHLD}$	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	SHCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	STCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{SHRST}$ pulse width, Low	Waveform 1	4.0			4.0		ns
$t_w(L)$	$\overline{SHLD}$ pulse width, Low	Waveform 1	4.0			4.0		ns
t_{REC}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	6.0			7.0		ns
t_{REC}	Recovery time, $\overline{SHLD}$ to SHCP	Waveform 2	6.0			7.0		ns

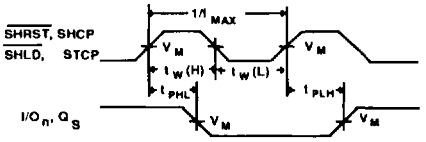
AC ELECTRICAL CHARACTERISTICS for 'F598

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximun clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_S ($\overline{SHLD}$ =Low)	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.0 9.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay SHCP to I/O_n	Waveform 1	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to I/O_n	Waveform 1	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to I/O_n	Waveform 2	4.0	8.0	10.0	4.0	11.0	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to Q_S	Waveform 2	4.0	8.0	10.0	4.0	11.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 5 Waveform 6	4.0 4.0	7.5 7.5	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 5 Waveform 6	3.0 3.0	6.0 6.0	8.0 8.0	3.0 3.0	9.0 9.0	ns

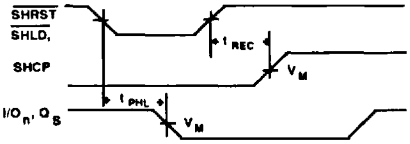
AC SETUP REQUIREMENTS for 'F598

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_{Sn} to SHCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_{Sn} to SHCP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low STCP to $\overline{SHLD}$	Waveform 4	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low STCP to $\overline{SHLD}$	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SHCPEN}$ to SHCP	Waveform 3	6.0 6.0			6.0 6.0		ns
$t_w(H)$ $t_w(L)$	SHCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	STCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{SHRST}$ pulse width, Low	Waveform 1	4.0			4.0		ns
$t_w(L)$	$\overline{SHLD}$ pulse width, Low	Waveform 1	4.0			4.0		ns
t_{REC}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	6.0			7.0		ns
t_{REC}	Recovery time, $\overline{SHLD}$ to SHCP	Waveform 2	6.0			6.0		ns

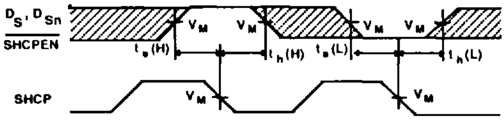
AC WAVEFORMS



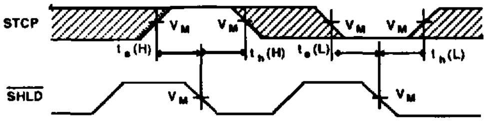
Waveform 1. Propagation Delay, Clock Inputs To Output, Clock Pulse Width, Maximum Clock Frequency, Shift Register Reset And Load Inputs To Serial Data Output



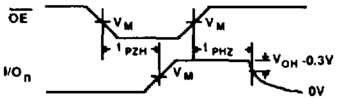
Waveform 2. Propagation Delay, Shift Register Reset And Load Inputs To Serial Data Output, Shift Register Reset And Load Inputs To Shift register Clock Pulse Input Recovery Time



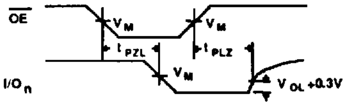
Waveform 3. Setup And Hold Times



Waveform 4. Setup And Hold Times



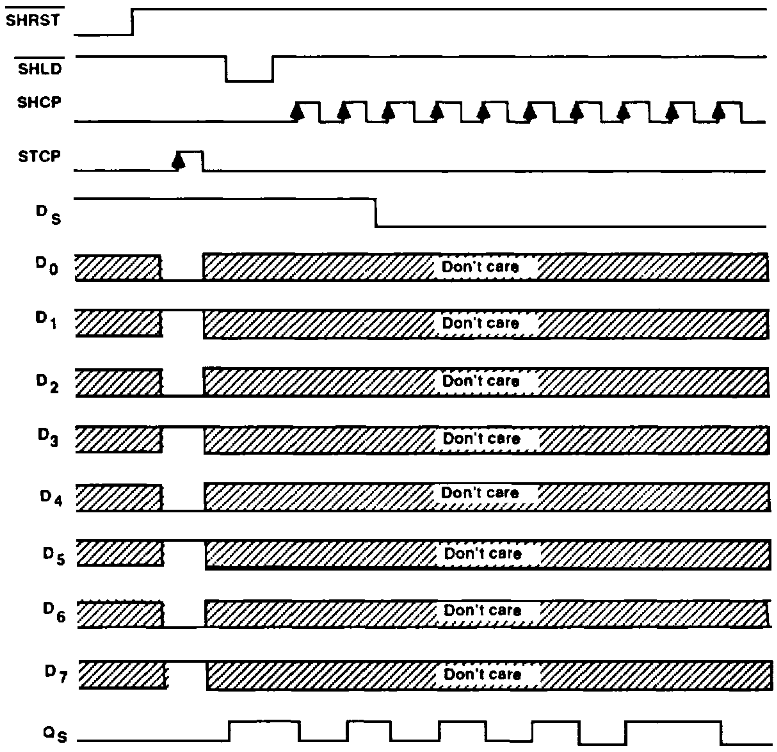
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



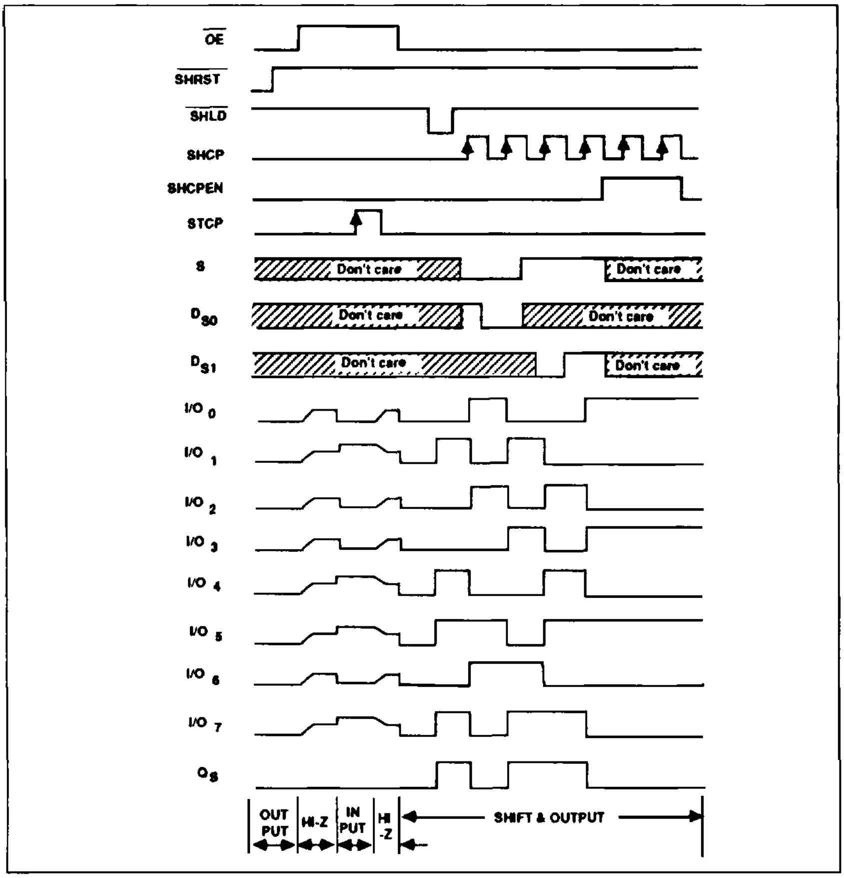
Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

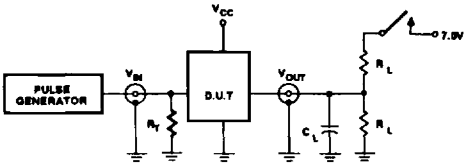
TYPICAL TIMING DIAGRAM for 74F597



TYPICAL TIMING DIAGRAM for 74F598



TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

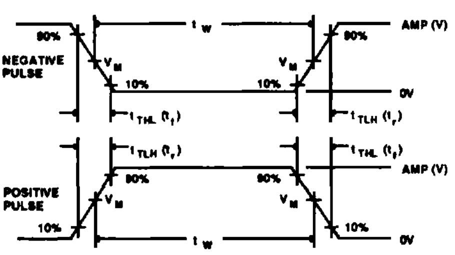
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns