



# DS3106

## Line Card Timing IC

[www.maxim-ic.com](http://www.maxim-ic.com)

### GENERAL DESCRIPTION

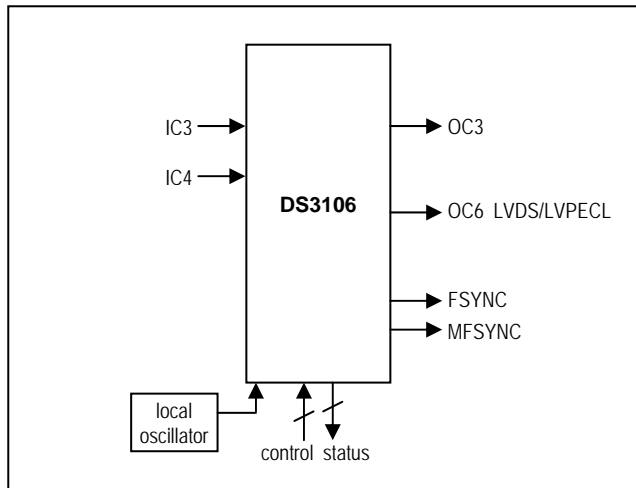
The DS3106 is a low-cost timing IC for telecom line cards. The device accepts two reference clocks from dual redundant system timing cards, continually monitors both inputs, and performs manual reference switching if the primary reference fails. The highly programmable DS3106 supports numerous input and output frequencies including frequencies required for SONET/SDH, Synchronous Ethernet (1G, 10G and 100Mb/s), wireless basestations and CMTS systems. PLL bandwidths from 18 Hz to 400 Hz are supported, and a wide variety of PLL characteristics and device features can be configured to meet the needs of many different applications.

The DS3106 register set is backward compatible with Semtech's ACS8526 line card timing IC. The DS3106 pinout is similar but not identical to the ACS8526.

### APPLICATIONS

SONET/SDH, Synchronous Ethernet, PDH and Other Line Cards in WAN Equipment Including MSPPs, Ethernet Switches, Routers, DSLAMs, and Wireless Base Stations.

### FUNCTIONAL DIAGRAM



### FEATURES

#### Advanced DPLL Technology

- Programmable PLL bandwidth: 18 Hz to 400 Hz
- Manual Reference Switching
- Holdover on Loss of Input Reference
- Frequency Conversion Among SONET/SDH, PDH, Ethernet, Wireless and CMTS Rates

#### 2 Input Clocks

- CMOS/TTL Signal Format ( $\leq 125$  MHz)
- Numerous Input Clock Frequencies Supported
  - SONET/SDH: 6.48, N x 19.44, N x 51.84 MHz
  - Ethernet xMII: 2.5, 25, 125 MHz
  - PDH: N x DS1, N x E1, N x DS2, DS3, E3
  - Frame Sync: 2 kHz, 4 kHz, 8 kHz
  - Custom: Any Multiple of 2 kHz up to 125 MHz

#### 2 Output Clocks

- One CMOS/TTL Output ( $\leq 125$  MHz)
- One LVDS/LVPECL Output ( $\leq 312.50$  MHz)
- Two Optional Frame Sync Outputs: 2 kHz, 8 kHz
- Numerous Output Clock Frequencies Supported
  - SONET/SDH: 6.48, N x 19.44, N x 51.84 MHz
  - Ethernet xMII: 2.5, 25, 125, 156.25, 312.5 MHz
  - PDH: N x DS1, N x E1, N x DS2, DS3, E3
  - Other: 10, 10.24, 13, 30.72 MHz, plus other frequencies available upon request
  - Frame Sync: 2 kHz, 8 kHz
  - Custom Clock Rates: Any Multiple of 2 kHz up to 77.76 MHz, Any Multiple of 8 kHz up to 311.04MHz

#### General

- Suitable line card IC for stratum 3E/3/4, SMC, SEC
- Internal Compensation for Master Clock Oscillator
- SPI Processor Interface
- 1.8V Operation with 3.3V I/O (5V tolerant)
- Industrial Operating Temperature Range

### ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
DS3106GN	-40 to 85°C	LQFP64
DS3106GN+	-40 to 85°C	LQFP64, RoHS compliant

## TABLE OF CONTENTS

1	STANDARDS COMPLIANCE .....	5
2	APPLICATION EXAMPLE.....	6
3	BLOCK DIAGRAM .....	6
4	DETAILED DESCRIPTION .....	7
5	DETAILED FEATURES.....	8
6	PIN DESCRIPTIONS .....	9
7	FUNCTIONAL DESCRIPTION.....	12
7.1	Overview.....	12
7.2	Device Identification and Protection .....	12
7.3	Local Oscillator and Master Clock Configuration .....	12
7.4	Input Clock Configuration .....	12
7.4.1	Signal Format Configuration.....	13
7.4.2	Frequency Configuration .....	13
7.5	Input Clock Monitoring.....	14
7.5.1	Frequency Monitoring.....	14
7.5.2	Activity Monitoring .....	14
7.5.3	Selected Reference Activity Monitoring.....	15
7.6	Input Clock Selection and Switching .....	15
7.7	DPLL Architecture and Configuration.....	16
7.7.1	T0 DPLL State Machine .....	17
7.7.2	Bandwidth.....	19
7.7.3	Damping Factor .....	20
7.7.4	Phase Detectors .....	20
7.7.5	Loss of Phase Lock Detection.....	21
7.7.6	Frequency and Phase Measurement .....	21
7.7.7	Input Jitter Tolerance.....	21
7.7.8	Jitter Transfer .....	21
7.7.9	Output Jitter and Wander .....	22
7.8	Output Clock Configuration .....	22
7.8.1	Signal Format Configuration.....	22
7.8.2	Frequency Configuration .....	22
7.9	Microprocessor Interface.....	30
7.10	Reset Logic.....	32
7.11	Power-Supply Considerations .....	32
7.12	Initialization.....	32
8	REGISTER DESCRIPTIONS.....	33
8.1	Status Bits .....	33
8.2	Configuration Fields.....	33

8.3	Multi-Register Fields .....	33
8.4	Register Definitions .....	34
9	JTAG TEST ACCESS PORT AND BOUNDARY SCAN .....	64
9.1	JTAG Description .....	64
9.2	JTAG TAP Controller State Machine Description .....	64
9.3	JTAG Instruction Register and Instructions .....	66
9.4	JTAG Test Registers .....	67
10	ELECTRICAL CHARACTERISTICS .....	68
10.1	DC Characteristics .....	68
10.2	Input Clock Timing .....	71
10.3	Output Clock Timing .....	71
10.4	SPI Interface Timing .....	72
10.5	JTAG Interface Timing .....	73
10.6	Reset Pin Timing .....	74
11	PIN ASSIGNMENTS .....	75
12	MECHANICAL INFORMATION .....	77
13	ACRONYMS AND ABBREVIATIONS .....	79
14	DATA SHEET REVISION HISTORY .....	80

## LIST OF FIGURES

Figure 2-1.	Typical Application Example .....	6
Figure 3-1.	Functional Block Diagram .....	6
Figure 7-1.	DPLL Block Diagram .....	16
Figure 7-2.	T0 DPLL State Transition Diagram .....	18
Figure 7-3.	FSYNC 8 kHz Options .....	29
Figure 7-4.	SPI Clock Phase Options .....	31
Figure 7-5.	SPI Bus Transactions .....	31
Figure 9-1.	JTAG Block Diagram .....	64
Figure 9-2.	JTAG TAP Controller State Machine .....	66
Figure 10-1.	Recommended Termination for LVDS Output Pins .....	70
Figure 10-2.	Recommended Termination for LVPECL Level-Compatible Output Pins .....	70
Figure 10-3.	SPI Interface Timing Diagram .....	72
Figure 10-4.	JTAG Timing Diagram .....	73
Figure 10-5.	Reset Pin Timing Diagram .....	74
Figure 11-1.	Pin Assignment Diagram .....	76
Figure 12-1.	LQFP Mechanical Dimensions .....	77

## LIST OF TABLES

Table 1-1. Applicable Telecom Standards.....	5
Table 6-1. Input Clock Pin Descriptions .....	9
Table 6-2. Output Clock Pin Descriptions.....	9
Table 6-3. Global Pin Descriptions .....	9
Table 6-4. SPI Bus Mode Pin Descriptions .....	10
Table 6-5. JTAG Interface Pin Descriptions .....	11
Table 6-6. Power Supply Pin Descriptions .....	11
Table 7-1. Input Clock Capabilities.....	13
Table 7-2. Input Clock Default Frequency Configuration.....	13
Table 7-3. Locking Frequency Modes .....	13
Table 7-4. Damping Factors and Peak Jitter/Wander Gain.....	20
Table 7-5. Output Clock Capabilities .....	22
Table 7-6. Digital1 Frequencies.....	23
Table 7-7. Digital2 Frequencies.....	24
Table 7-8. APLL Frequency to Output Frequencies (T0 APLL and T4 APLL) .....	24
Table 7-9. T0 APLL Frequency Configuration .....	24
Table 7-10. T0 APLL2 Frequency Configuration .....	24
Table 7-11. T4 APLL Frequency Configuration.....	25
Table 7-12. OC3 and OC6 Output Frequency Selection.....	25
Table 7-13. Possible Frequencies for Programmable Outputs .....	26
Table 7-14 T0CR1.T0FREQ Default Settings .....	28
Table 7-15 T4CR1.T4FREQ Default Settings .....	28
Table 7-16 OC6 Default Frequency Configuration .....	28
Table 7-17 OC3 Default Frequency Configuration .....	28
Table 8-1. Register Map .....	34
Table 9-1. JTAG Instruction Codes .....	66
Table 9-2. JTAG ID Code .....	67
Table 10-1. Recommended DC Operating Conditions.....	68
Table 10-2. DC Characteristics.....	68
Table 10-3. CMOS/TTL Pins .....	69
Table 10-4. LVDS Output Pins .....	69
Table 10-5. LVPECL Level-Compatible Output Pins.....	69
Table 10-6. Input Clock Timing.....	71
Table 10-7. Input Clock to Output Clock Delay .....	71
Table 10-8. Output Clock Phase Alignment, Frame Sync Alignment Mode.....	71
Table 10-9. SPI Interface Timing .....	72
Table 10-10. JTAG Interface Timing.....	73
Table 10-11. Reset Pin Timing .....	74
Table 11-1. Pin Assignments Sorted by Signal Name.....	75
Table 12-1. LQFP Thermal Properties, Natural Convection.....	78
Table 12-2. LQFP Theta-JA ( $\theta_{JA}$ ) vs. Airflow .....	78

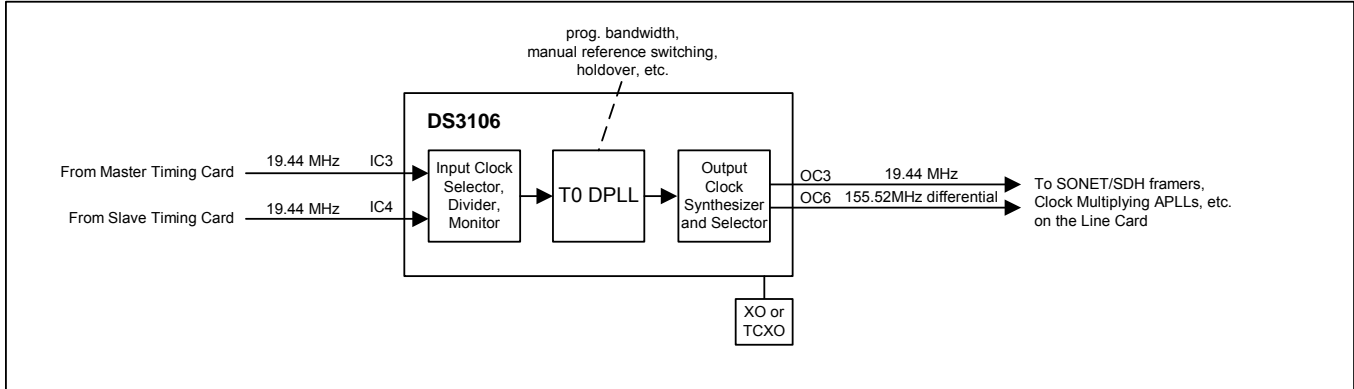
# 1 STANDARDS COMPLIANCE

**Table 1-1. Applicable Telecom Standards**

<b>SPECIFICATION</b>	<b>SPECIFICATION TITLE</b>
<b>ANSI</b>	
T1.101	<i>Synchronization Interface Standard, 1999</i>
TIA/EIA-644-A	<i>Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, 2001</i>
<b>ETSI</b>	
EN 300 417-6-1	<i>Transmission and Multiplexing (TM); Generic Requirements of Transport Functionality of Equipment; Part 6-1: Synchronization Layer Functions, v1.1.3 (1999-05)</i>
EN 300 462-3-1	<i>Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 3-1: The Control of Jitter and Wander within Synchronization Networks, v1.1.1 (1998-05)</i>
EN 300 462-5-1	<i>Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 5-1: Timing Characteristics of Slave Clocks Suitable for Operation in Synchronous Digital Hierarchy (SDH) Equipment, v1.1.1 (1998-05)</i>
<b>IEEE</b>	
IEEE 1149.1	<i>Standard Test Access Port and Boundary-Scan Architecture, 1990</i>
<b>ITU-T</b>	
G.783	<i>ITU G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003)</i>
G.813	<i>Timing characteristics of SDH equipment slave clocks (SEC) (03/2003)</i>
G.823	<i>The Control of Jitter and Wander within Digital Networks which are Based on the 2048kbps Hierarchy (03/2000)</i>
G.824	<i>The Control of Jitter and Wander within Digital Networks which are Based on the 1544kbps Hierarchy (03/2000)</i>
G.825	<i>The Control of Jitter and Wander within Digital Networks which are Based on the Synchronous Digital Hierarchy (SDH) (03/2000)</i>
G.8261	<i>Timing and Synchronization Aspects in Packet Networks (05/2006)</i>
G.8262	<i>Timing characteristics of Synchronous Ethernet Equipment slave clock (EEC) (06/2007, pre-published)</i>
<b>TELCORDIA</b>	
GR-253-CORE	<i>SONET Transport Systems: Common Generic Criteria, Issue 3, September 2000</i>
GR-1244-CORE	<i>Clocks for the Synchronized Network: Common Generic Criteria, Issue 2, December 2000</i>

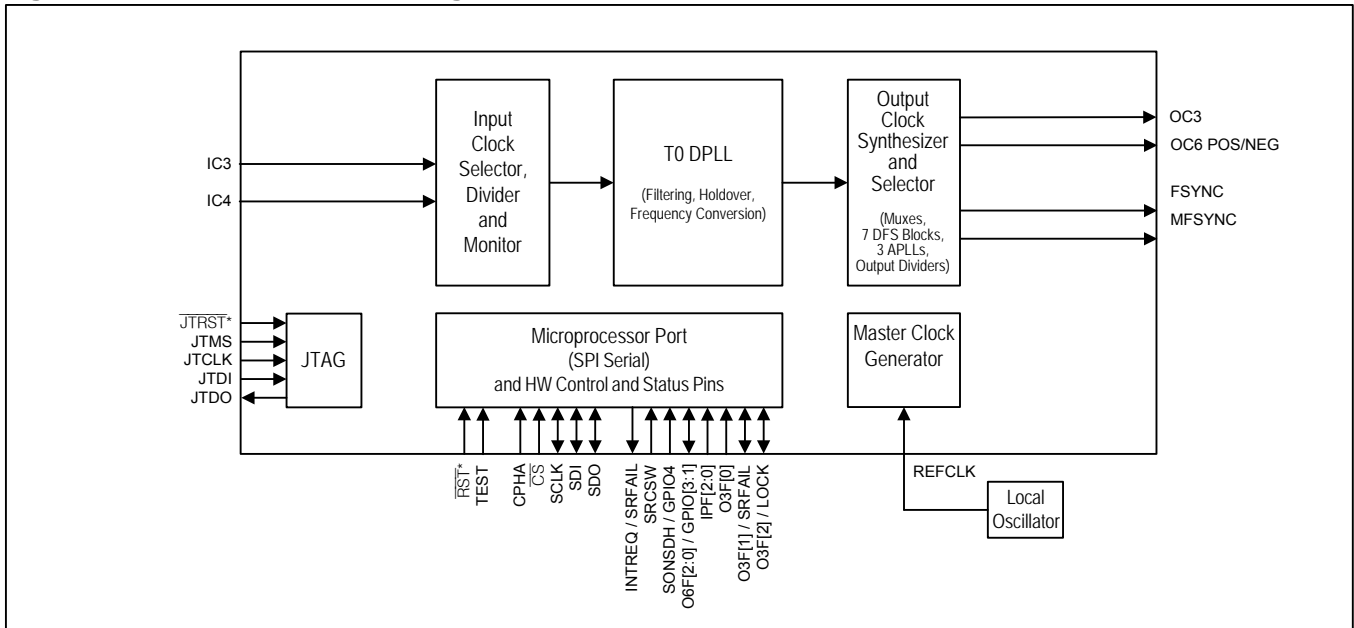
## 2 APPLICATION EXAMPLE

Figure 2-1. Typical Application Example



## 3 BLOCK DIAGRAM

Figure 3-1. Functional Block Diagram



## 4 DETAILED DESCRIPTION

[Figure 3-1](#) illustrates the blocks described in this section and how they relate to one another. [Section 5](#) provides a detailed feature list.

The DS3106 is a complete line card timing IC. At the core of this device is a digital phase-locked loop (DPLL). DPLL technology makes use of digital-signal processing (DSP) and digital-frequency synthesis (DFS) techniques to implement PLLs that are precise, flexible, and have consistent performance over voltage, temperature, and manufacturing process variations. The DS3106's T0<sup>1</sup> DPLL is digitally configurable for input and output frequencies, loop bandwidth, damping factor, pull-in/hold-in range, and a variety of other factors. The T0 DPLL can directly lock to many common telecom frequencies and also can lock at 8 kHz to any multiple of 8 kHz up to 125 MHz. The DPLL can also tolerate and filter significant amounts of jitter and wander.

In typical line card applications, the T0 DPLL takes reference clock signals from two redundant system timing cards, monitors both, selects one, and uses that reference to produce a variety of clocks that are needed to time the outgoing traffic interfaces of the line card (SONET/SDH, PDH, Synchronous Ethernet, etc.). To perform this role in a variety of systems with diverse performance requirements, the T0 DPLL has a sophisticated feature set and is highly configurable. T0 can automatically transition among free-run, locked and holdover states without software intervention. In free-run, T0 generates a stable, low-noise clock with the same frequency accuracy as the external oscillator connected to the REFCLK pin. With software calibration the DS3106 can even improve the accuracy to within  $\pm 0.02$  ppm. When the selected input reference clock has been validated, T0 transitions to the locked state in which its output clock accuracy is equal to the accuracy of the input reference. While in the locked state, T0 acquires an average frequency value to use as the holdover frequency. When its selected reference fails, T0 can very quickly detect the failure and enter the holdover state to avoid affecting its output clock. From holdover it can be manually switched to the other input reference. When all input references are lost, T0 stays in the holdover state in which it generates a stable low-noise clock with initial frequency accuracy equal to its stored holdover value and drift performance determined by the quality of the external oscillator.

At the front end of the T0 DPLL is the Input Clock Selector, Divider, and Monitor (ICSDM) block. This block continuously monitors both input clocks for activity and coarse frequency accuracy. In addition, ICSDM can manually select one of the input clocks to be the selected reference for the T0 DPLL. The ICSDM block can also divide the selected clock down to a lower rate as needed by the DPLL.

The Output Clock Synthesizer and Selector (OCSS) block shown in [Figure 3-1](#) and in more detail in [Figure 7-1](#) contains three output APLLs—the T0 APLL, the T0 APLL2 and the T4 APLL—and their associated DFS engines and output divider logic plus several additional DFS engines. The APLL DFS blocks do frequency translation, creating clocks of various frequencies that are phase/frequency locked to the output clock of the T0 DPLL. The APLLs multiply the clock rates from the APLL DFS blocks and simultaneously attenuate jitter. Altogether the output blocks of the DS3106 can produce more than 90 different output frequencies including common SONET/SDH, PDH and Synchronous Ethernet rates plus 2 kHz and 8 kHz frame sync pulses.

The entire chip is clocked from the external oscillator connected to the REFCLK pin. Thus the free-run and holdover stability of the DS3106 is entirely a function of the stability of the external oscillator, the performance of which can be selected to match the application: typically XO or TCXO. The 12.8MHz clock from the external oscillator is multiplied by 16 by the Master Clock Generator block to create the 204.8MHz master clock used by the rest of the device.

---

<sup>1</sup> The labels T0 and T4 in this document are adapted from output ports of the SETS function specified in ITU and ETSI standards such as ETSI EN 300 462-2-1. Although strictly speaking these names are appropriate only for timing card ICs such as the DS3100 that can serve as the SETS function, the names have been carried over to the DS3106 so that all of the products in Dallas/Maxim's timing IC product line have consistent nomenclature.

## 5 DETAILED FEATURES

### Input Clock Features

- Two programmable-frequency CMOS/TTL input clocks
- Input clocks accept any multiple of 2kHz up to 125MHz
- All input clocks are constantly monitored by programmable activity monitors

### DPLL Features

- High-resolution DPLL plus three low-jitter output APLLs
- Sophisticated state machine automatically transitions between free-run, locked and holdover states
- Programmable bandwidth from 18 Hz to 400 Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10 or 20
- Multiple phase detectors: phase/frequency, early/late, and multi-cycle
- Phase/frequency locking ( $\pm 360^\circ$  capture) or nearest-edge phase locking ( $\pm 180^\circ$  capture)
- Multi-cycle phase detection and locking (up to  $\pm 8191$  UI) improves jitter tolerance and lock time
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 1 second interval
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8 kHz) and multi-frame sync (2 kHz) aligned with output clocks

### Output APLL Features

- Three separate clock-multiplying, jitter attenuating APLLs can simultaneously produce SONET/SDH rates, Fast/Gigabit Ethernet rates and 10G Ethernet rates, all locked to a common reference clock
- The T0 APLL, has frequency options suitable for Nx19.44MHz, NxDS1, NxE1, Nx25MHz and Nx62.5MHz
- The T4 APLL has frequency options suitable for Nx19.44MHz, NxDS1, NxE1, NxDS2, DS3, E3, Nx10MHz, Nx10.24 MHz, Nx13MHz, Nx25 MHz and Nx62.5 MHz
- The T0 APLL2 produces 312.5 MHz for 10G Synchronous Ethernet applications

### Output Clock Features

- Two output clocks: one CMOS/TTL ( $\leq 125$  MHz) and one LVDS/LVPECL ( $\leq 312.50$  MHz)
- Output clock rates include 2 kHz, 8 kHz, NxDS1, NxE1, DS2, DS3, E3, 6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 2.5 MHz, 25 MHz, 125 MHz, 156.25 MHz, 312.50 MHz, 10 MHz, 10.24 MHz, 13 MHz, 30.72 MHz and various multiples and submultiples of these rates
- Custom clock rates also available: any multiple of 2 kHz up to 77.76 MHz and any multiple of 8 kHz up to 311.04MHz
- All outputs have  $< 1$  ns peak-to-peak output jitter; outputs from APLLs have  $< 0.5$  ns peak-to-peak
- 8kHz frame sync and 2kHz multiframe sync outputs have programmable polarity and pulse width and can be disciplined by a 2 kHz or 8 kHz sync input

### General Features

- Operates from a single external 12.800 MHz local oscillator (XO or TCXO)
- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write-protected

## 6 PIN DESCRIPTIONS

**Table 6-1. Input Clock Pin Descriptions**

Pin Name <sup>(1)</sup>	Type <sup>(2)</sup>	Pin Description
REFCLK	I	<b>Reference Clock.</b> Connect to a 12.800 MHz, high-accuracy, high-stability, low-noise local oscillator (XO or TCXO). See section 7.3.
IC3	I <sub>PD</sub>	<b>Input Clock 3.</b> CMOS/TTL. Programmable frequency. Default frequency selected by IPF[2:0] pins when the $\overline{\text{RST}}$ pin goes high, 8kHz if IPF[2:0] pins left open).
IC4	I <sub>PD</sub>	<b>Input Clock 4.</b> CMOS/TTL. Programmable frequency. Default frequency selected by IPF[2:0] pins when the $\overline{\text{RST}}$ pin goes high, 8kHz if IPF[2:0] pins left open).

**Table 6-2. Output Clock Pin Descriptions**

Pin Name <sup>(1)</sup>	Type <sup>(2)</sup>	Pin Description
OC3	O	<b>Output Clock 3.</b> CMOS/TTL. Programmable frequency. Default frequency selected by O3F[2:0] pins when the $\overline{\text{RST}}$ pin goes high, 19.44 MHz if O3F[2:0] pins left open). See Table 7-17.
OC6POS, OC6NEG	O <sub>DIFF</sub>	<b>Output Clock 6.</b> LVDS/LVPECL. Programmable frequency. Default frequency selected by O6F[2:0] pins when the $\overline{\text{RST}}$ pin goes high, 38.88 MHz if O6F[2:0] pins left open). The output mode is selected by MCR8.OC6SF[1:0]. See Table 10-4, Table 10-5, Figure 10-1 and Figure 10-2.
FSYNC	O <sub>3</sub>	<b>8 kHz FSYNC.</b> CMOS/TTL. 8 kHz frame sync or clock. (default 50% duty cycle clock, non-inverted) The pulse polarity and width are selectable using FSCR1.8KINV and FSCR1.8KPUL.
MFSYNC	O <sub>3</sub>	<b>2 kHz MFSYNC.</b> CMOS/TTL. 2 kHz frame sync or clock. (default 50% duty cycle clock, non-inverted) The pulse polarity and width are selectable using FSCR1.2KINV and FSCR1.2KPUL.

**Table 6-3. Global Pin Descriptions**

Pin Name <sup>(1)</sup>	Type <sup>(2)</sup>	Pin Description
$\overline{\text{RST}}$	I <sub>PU</sub>	<b>Reset (active low).</b> When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{\text{RST}}$ is low. $\overline{\text{RST}}$ should be held low for at least two REFCLK cycles after the external oscillator has stabilized and is providing valid clock signals.
SRCSW	I <sub>PD</sub>	<b>Source Switching.</b> Input reference selection pin. Selects IC3 when high and IC4 when low. See section 7.6..
TEST	I <sub>PD</sub>	<b>Factory Test Mode Select.</b> Wire this pin to VSS for normal operation.
IPF0	I <sub>PD</sub>	<b>Input Frequency Select 0.</b> Together with IPF1 and IPF2 this pin sets the default frequency of the IC3 and IC4 input clock pins. The value is sampled when $\overline{\text{RST}}$ goes high, and the FREQ[3:0] fields of ICR3 and ICR4 are set accordingly. See Table 7-2. After $\overline{\text{RST}}$ goes high this pin is ignored.
IPF1	I <sub>PD</sub>	<b>Input Frequency Select 1.</b> Together with IPF0 and IPF2 this pin sets the default frequency of the IC3 and IC4 input clock pins. The value is sampled when $\overline{\text{RST}}$ goes high, and the FREQ[3:0] fields of ICR3 and ICR4 are set accordingly. See Table 7-2. After $\overline{\text{RST}}$ goes high this pin is ignored.
IPF2	I <sub>PD</sub>	<b>Input Frequency Select 2.</b> Together with IPF0 and IPF1 this pin sets the default frequency of the IC3 and IC4 input clock pins. The value is sampled when $\overline{\text{RST}}$ goes high, and the FREQ[3:0] fields of ICR3 and ICR4 are set accordingly. See Table 7-2. After $\overline{\text{RST}}$ goes high this pin is ignored.
O3F0	I <sub>PU</sub>	<b>OC3 Frequency Select 0.</b> This pin is sampled when the $\overline{\text{RST}}$ pin goes high and the value is used as O3F0 which together with O3F2 and O3F1 sets the default frequency of the OC3 output clock pin. See Table 7-17. After $\overline{\text{RST}}$ goes high this pin is ignored.

Pin Name <sup>(1)</sup>	Type <sup>(2)</sup>	Pin Description
O3F1 / SRFAIL	IO <sub>PU</sub>	<b>OC3 Frequency Select 1 / SRFAIL Status Pin.</b> This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O3F1 which together with O3F2 and O3F0 sets the default frequency of the OC3 output clock pin. See <a href="#">Table 7-17</a> . After $\overline{RST}$ goes high, if <code>MCR10:SRFPIN = 1</code> , this pin follows the state of the SRFAIL status bit in the <code>MSR2</code> register. This gives the system a very fast indication of the failure of the selected reference. When <code>MCR10:SRFPIN = 0</code> , SRFAIL is disabled (low).
O3F2 / LOCK	IO <sub>PD</sub>	<b>OC3 Frequency Select 2 / T0 DPLL LOCK Status.</b> This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O3F2 which together with O3F1 and O3F0 sets the default frequency of the OC3 output clock pin. See <a href="#">Table 7-17</a> . After $\overline{RST}$ goes high, if <code>MCR1.LOCKPIN=1</code> , this pin indicates the lock state of the T0 DPLL. When <code>MCR1.LOCKPIN=0</code> , LOCK is disabled (low). 0 = Not Locked 1 = Locked
O6F0 / GPIO1	IO <sub>PD</sub>	<b>OC6 Frequency Select 0 / General Purpose I/O Pin 1.</b> This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O6F0 which together with O6F2 and O6F1 sets the default frequency of the OC6 output clock pin. See <a href="#">Table 7-16</a> . After $\overline{RST}$ goes high this pin can be used as a general purpose I/O pin. <code>GPCR:GPIO1D</code> configures this pin as an input or an output. <code>GPCR:GPIO1O</code> specifies the output value. <code>GPSR:GPIO1</code> indicates the state of the pin.
O6F1 / GPIO2	IO <sub>PD</sub>	<b>OC6 Frequency Select 1 / General Purpose I/O Pin 2.</b> This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O6F1 which together with O6F2 and O6F0 sets the default frequency of the OC6 output clock pin. See <a href="#">Table 7-16</a> . After $\overline{RST}$ goes high this pin can be used as a general purpose I/O pin. <code>GPCR:GPIO2D</code> configures this pin as an input or an output. <code>GPCR:GPIO2O</code> specifies the output value. <code>GPSR:GPIO2</code> indicates the state of the pin.
O6F2 / GPIO3	IO <sub>PU</sub>	<b>OC6 Frequency Select 2 / General Purpose I/O Pin 3.</b> This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O6F2 which together with O6F1 and O6F0 sets the default frequency of the OC6 output clock pin. See <a href="#">Table 7-16</a> . After $\overline{RST}$ goes high this pin can be used as a general purpose I/O pin. <code>GPCR:GPIO3D</code> configures this pin as an input or an output. <code>GPCR:GPIO3O</code> specifies the output value. <code>GPSR:GPIO3</code> indicates the state of the pin.
SONSDH / GPIO4	IO <sub>PD</sub>	<b>SONET/SDH Frequency Select Input or GPIO4 Pin.</b> When $\overline{RST}$ goes high the state of this pin sets the reset-default state of <code>MCR3:SONSDH</code> , <code>MCR6:DIG1SS</code> and <code>MCR6:DIG2SS</code> . After $\overline{RST}$ goes high this pin can be used as a general purpose I/O pin. <code>GPCR:GPIO4D</code> configures this pin as an input or an output. <code>GPCR:GPIO4O</code> specifies the output value. <code>GPSR:GPIO4</code> indicates the state of the pin. Reset latched values: 0 = SDH rates (N x 2.048 MHz) 1 = SONET rates (N x 1.544 MHz)
INTREQ / LOS	O <sub>3</sub>	<b>Interrupt Request / Loss of Signal.</b> Programmable (default: INTREQ). The <code>INTCR:LOS</code> bit determines whether the pin is indicates interrupt requests or loss of signal (i.e. loss of selected reference). <b>INTCR:LOS=0: INTREQ mode</b> The behavior of this pin is configured in the <code>INTCR</code> register. Polarity can be active-high or active-low. Drive action can be push-pull or open-drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed. <b>INTCR:LOS=1: LOS mode</b> This pin indicates the real-time state of the selected reference activity monitor (see section <a href="#">7.5.3</a> ).

**Table 6-4. SPI Bus Mode Pin Descriptions**See section [7.9](#) for functional description and section [10.4](#) for timing specifications.

Pin Name <sup>(1)</sup>	Type <sup>(2)</sup>	Pin Description
$\overline{CS}$	I <sub>PU</sub>	<b>Chip Select.</b> This pin must be asserted (low) to read or write internal registers.
SCLK	I	<b>Serial Clock.</b> SCLK is always driven by the SPI bus master.
SDI	I	<b>Serial Data Input.</b> The SPI bus master transmits data to the device on this pin.

Pin Name <sup>(1)</sup>	Type <sup>(2)</sup>	Pin Description
SDO	O	<b>Serial Data Output.</b> The device transmits data to the SPI bus master on this pin.
CPHA	I	<b>Clock Phase</b> See <a href="#">Figure 7-4</a> . 0 = data is latched on the leading edge of the SCLK pulse 1 = data is latched on the trailing edge of the SCLK pulse

**Table 6-5. JTAG Interface Pin Descriptions**

See section 9 for functional description and section 10.5 for timing specifications.

Pin Name <sup>(1)</sup>	Type <sup>(2)</sup>	Pin Description
$\overline{\text{JTRST}}$	I <sub>PU</sub>	<b>JTAG Test Reset (active low).</b> Asynchronously resets the test access port (TAP) controller. If not used, $\overline{\text{JTRST}}$ can be held low or high.
JTCLK	I	<b>JTAG Clock,</b> Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high.
JTDI	I <sub>PU</sub>	<b>JTAG Test Data Input.</b> Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high.
JTDO	O <sub>3</sub>	<b>JTAG Test Data Output.</b> Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave floating.
JTMS	I <sub>PU</sub>	<b>JTAG Test Mode Select.</b> Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used connect to VDDIO or leave floating.

**Table 6-6. Power Supply Pin Descriptions**

Pin Name <sup>(1)</sup>	Type <sup>(2)</sup>	Pin Description
VDD	P	<b>Core Power Supply.</b> 1.8V ±10%.
VDDIO	P	<b>I/O Power Supply.</b> 3.3V ±5%.
VSS	P	<b>Ground Reference .</b>
AVDD_DL	P	<b>Power Supply for OC6 Digital Logic.</b> 1.8V ±10%.
AVSS_DL	P	<b>Return for OC6 Digital Logic.</b>
VDD_OC6	P	<b>Power Supply for Differential Output OC6POS/NEG.</b> 1.8V ±10%.
VSS_OC6	P	<b>Return for LVDS Differential Output OC6POS/NEG.</b>
AVDD_PLL1	P	<b>Power Supply for Master Clock Generator APLL.</b> 1.8V ±10%.
AVSS_PLL1	P	<b>Return for Master Clock Generator APLL.</b>
AVDD_PLL2	P	<b>Power Supply for T0 APLL.</b> 1.8V ±10%.
AVSS_PLL2	P	<b>Return for T0 APLL.</b>
AVDD_PLL3	P	<b>Power Supply for T4 APLL.</b> 1.8V ±10%.
AVSS_PLL3	P	<b>Return for T4 APLL.</b>
AVDD_PLL4	P	<b>Power Supply for T0 APLL2.</b> 1.8V ±10%.
AVSS_PLL4	P	<b>Return for T0 APLL2.</b>

**Note 1:** All pin names with an overbar (e.g.  $\overline{\text{RST}}$ ) are active low.**Note 2:** All pins, except power and analog pins, are CMOS/TTL unless otherwise specified in the pin description.**PIN TYPES**

I = input pin

I<sub>DIFF</sub> = input pin that is LVDS/LVPECL differential signal compatibleI<sub>PD</sub> = input pin with internal 50kΩ pull-downI<sub>PU</sub> = input pin with internal 50kΩ pull-up

I/O = input/output pin

IO<sub>PD</sub> = input/output pin with internal 50kΩ pull-downIO<sub>PU</sub> = input/output pin with internal 50kΩ pull-up

O = output pin

O<sub>3</sub> = output pin that can tri-stated (i.e. placed in a high-impedance state)O<sub>DIFF</sub> = output pin that is LVDS/LVPECL differential signal compatible

P = power-supply pin

**Note 3:** All digital pins, except OCn, are I/O pins in JTAG mode. OCn pins do not have JTAG functionality.

## 7 FUNCTIONAL DESCRIPTION

### 7.1 Overview

The DS3106 has two input clocks, two output clocks and a high-performance DPLL known as T0. See [Figure 3-1](#). The two input clocks are CMOS/TTL (5V tolerant) and can accept signals from 2 kHz to 125 MHz. Each input clock is monitored continually for activity. SRFAIL is set or cleared based on the activity of the selected input.

The T0 DPLL can directly lock to many common datacom and telecom frequencies, including, but not limited to 8 kHz, DS1, E1, 10 MHz, 19.44 MHz, and 38.88 MHz as well as Ethernet frequencies including 25 MHz, 62.5 MHz, and 125 MHz. The DPLL can also lock to multiples of the standard direct-lock frequencies including 8 kHz. The T0 DPLL has all the features needed for synchronizing a line card to dual redundant system timing cards.

The T0 DPLL has these features:

- A full state machine for automatic transitions among free-run, locked, and holdover states
- Adjustable PLL characteristics, including bandwidth, pull-in range, and damping factor
- Six bandwidth selections from 18 Hz to 400 Hz
- Frequency conversion between input and output using digital frequency synthesis
- Combined performance of a stable, consistent digital PLL and low-jitter analog output PLLs
- Ability to lock to several common telecom and ethernet frequencies plus multiples of the standard direct lock frequencies including 8 KHz
- Instant digital one-second averaging and free-run holdover modes

Typically the internal state machine controls the T0 DPLL, but manual control by system software is also available.

The outputs of the T0 DPLL can be connected to seven output DFS engines. See [Figure 7-1](#). Three of these output DFS engines are associated with high-speed APLLs that multiply the DPLL clock rate and filter DPLL output jitter. The outputs of the APLLs are divided down to make a wide variety of possible frequencies available at the output clock pins.

The OC3 and OC6 output clocks can be configured for a variety of different frequencies that are frequency and phase locked to the T0 DPLL. The OC6 output is LVDS/LVPECL. The OC3 output is CMOS/TTL. Altogether more than 60 output frequencies are possible, ranging from 2 kHz to 312.5 MHz. The FSYNC output clock is always 8 kHz, and the MFSYNC output clock is always 2 kHz.

### 7.2 Device Identification and Protection

The 16-bit read-only ID field in the [ID1](#) and [ID2](#) registers is set to 0C22h = 3106 decimal. The device revision can be read from the [REV](#) register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the [PROT](#) register.

### 7.3 Local Oscillator and Master Clock Configuration

The T0 DPLL and the output DFS engines operate from a 204.8 MHz master clock. The master clock is synthesized from a 12.800 MHz clock originating from a local oscillator attached to the REFCLK pin. The stability of the T0 DPLL in freerun or holdover is equivalent to the stability of the local oscillator. Selection of an appropriate local oscillator is therefore of crucial importance if the telecom standards listed in [Table 1-1](#) are to be met. Simple XOs can be used in less stringent cases, but TCXOs or even OCXOs may be required in the most demanding applications. Careful evaluation of the local oscillator component is necessary to ensure proper performance. Contact Dallas/Maxim at [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com) for recommended oscillators.

The stability of the local oscillator is very important, but its absolute frequency accuracy is less important because the DPLL can compensate for frequency inaccuracies when synthesizing the 204.8 MHz master clock from the local oscillator clock. The MCLKFREQ field in registers [MCLK1](#) and [MCLK2](#) specifies the frequency adjustment to be applied. The adjust can be from -771 ppm to +514 ppm in 0.0196229 ppm (i.e. ~0.02 ppm) steps.

### 7.4 Input Clock Configuration

The DS3106 has two input clocks, IC3 and IC4. [Table 7-1](#) provides summary information about each clock, including signal format and available frequencies. The device tolerates a wide range of duty cycles on input clocks, out to a minimum high time or minimum low time of 3 ns or 30% of the clock period, whichever is smaller.

### 7.4.1 Signal Format Configuration

Both IC3 and IC4 accept TTL and 3.3V CMOS levels. One key configuration bit that affects the available frequencies is the SONSDH bit in [MCR3](#). When SONSDH=1 (SONET mode), the 1.544 MHz frequency is available. When SONSDH=0 (SDH mode), the 2.048 MHz frequency is available. During reset the default value of this bit is latched from the SONSDH pin.

**Table 7-1. Input Clock Capabilities**

Input Clock	Signal Formats	Frequencies	Default Frequency
IC3	CMOS / TTL	up to 125 MHz <sup>(1)</sup>	Determined by IPF[2:0] and SONSDH pins, see Table 7-2.
IC4	CMOS / TTL	up to 125 MHz <sup>(1)</sup>	Determined by IPF[2:0] and SONSDH pins, see Table 7-2.

**Note 1:** Available frequencies for CMOS/TTL input clocks are: 2 kHz, 4 kHz, 8 kHz, 1.544 MHz (SONET mode), 2.048 MHz (SDH mode), 6.312 MHz, 6.48 MHz, 19.44 MHz, 25.0 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 62.5 MHz, 77.76 MHz, and any multiple of 2 kHz up to 125MHz.

**Table 7-2. Input Clock Default Frequency Configuration**

IPF[2:0]	SONSDH	Default Frequency, lock mode
000	X	8 KHz, direct lock
001	0	2.048 MHz, direct lock
001	1	1.544 MHz, direct lock
010	X	6.48 MHz, direct lock
011	X	19.44 MHz, direct lock
100	X	25.92 MHz, direct lock
101	X	38.88 MHz, direct lock
110	X	51.84 MHz, direct lock
111	X	77.76 MHz, direct lock

### 7.4.2 Frequency Configuration

Input clock frequencies are configured in the **FREQ** field of the [ICR](#) registers. The **DIVN** and **LOCK8K** bits of these same registers specify the locking frequency mode, as shown in [Table 7-3](#).

**Table 7-3. Locking Frequency Modes**

DIVN	LOCK8K	Locking Frequency Mode
0	0	Direct Lock mode
0	1	LOCK8K mode
1	0	DIVN mode
1	1	Alternate Direct Lock mode

#### 7.4.2.1 Direct Lock Mode

In direct lock mode, the T0 DPLL locks to the selected reference at the frequency specified in the corresponding [ICR](#) register. Direct lock mode can only be used for input clocks with these specific frequencies: 2 kHz, 4 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 5 MHz, 6.312 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 31.25 MHz, 38.88 MHz, 51.84 MHz and 77.76 MHz. The **DIVN** mode can be used to divide an input down to any of these frequencies.

MTIE figures may be marginally better in direct lock mode because the higher frequencies allow more frequent phase updates.

### 7.4.2.2 Alternate Direct Lock Mode

Alternate direct lock mode is the same as direct lock mode except an alternate list of direct lock frequencies is used (see the **FREQ** field definition in the **ICR** register description). The alternate frequencies are included to support clock rates found in Ethernet, CMTS, wireless and GPS applications. The alternate frequencies are: 10 MHz, 25 MHz, 62.5 MHz and 125 MHz. The frequencies 62.5 MHz and 125 MHz are internally divided down to 31.25 MHz, while 10 MHz and 25 MHz are internally divided down to 5 MHz.

### 7.4.2.3 LOCK8K Mode

In LOCK8K mode, an internal divider is configured to divide the selected reference down to 8 kHz. The DPLL locks to the 8 kHz output of the divider. LOCK8K mode can only be used for input clocks with the standard direct lock frequencies: 8 kHz, 1.544 MHz, 2.048 MHz, 5 MHz, 6.312 MHz, 6.48 MHz, 19.44 MHz, 25.0 MHz, 25.92 MHz, 31.25 MHz, 38.88 MHz, 51.84 MHz, 62.5 MHz and 77.76 MHz. LOCK8K mode is enabled for a particular input clock by setting the LOCK8K bit in the corresponding **ICR** register.

LOCK8K mode gives a greater tolerance to input jitter when the multi-cycle phase detector is disabled because it uses lower frequencies for phase comparisons. The clock edge to lock to on the selected reference can be configured using the 8KPOL bit in the **TEST1** register. For 2 kHz and 4 kHz clocks the LOCK8K bit is ignored and direct-lock mode is used.

### 7.4.2.4 DIVN Mode

In DIVN mode, an internal divider is configured from the value stored in the **DIVN** registers. The DIVN value must be chosen so that when the selected reference is divided by DIVN+1, the resulting clock frequency is the same as the standard direct lock frequency selected in the **FREQ** field of the **ICR** register. The DPLL locks to the output of the divider. DIVN mode can only be used for input clocks whose frequency is less than or equal to 125 MHz. The DIVN register field can range from 0 to 65,535 inclusive. The same DIVN+1 factor is used for all input clocks configured for DIVN mode.

## 7.5 Input Clock Monitoring

Each input clock is continuously monitored for activity. Activity monitoring is described in sections 7.5.2 and 7.5.3. The valid/invalid state of each input clock is reported in the corresponding real-time status bit in register **VALSR1**. When the valid/invalid state of a clock changes, the corresponding latched status bit is set in registers **MSR1**, and an interrupt request occurs if the corresponding interrupt enable bit is set in registers **IER1**.

### 7.5.1 Frequency Monitoring

The DS3106 monitors the frequency of each input clock and invalidates any clock whose frequency is more than 10,000 ppm away from nominal. The frequency range monitor can be disabled by clearing the **MCR1.FREN** bit. The frequency range measurement uses the internal 204.8 MHz master clock as the frequency reference.

### 7.5.2 Activity Monitoring

Each input clock is monitored for activity and proper behavior using a leaky bucket accumulator. A leaky bucket accumulator is similar to an analog integrator: the output amplitude increases in the presence of input events and gradually decays in the absence of events. When events occur infrequently, the accumulator value decays fully between events and no alarm is declared. When events occur close enough together, the accumulator increments faster than it can decay and eventually reaches the alarm threshold. After an alarm has been declared, if events occur infrequently enough, the accumulator can decay faster than it is incremented and eventually reaches the alarm clear threshold. The leaky bucket events come from the frequency range and fast activity monitors.

There is one leaky bucket configuration common to both inputs which has programmable size, alarm declare threshold, alarm clear threshold, and decay rate, all of which are specified in the **LBxy** registers.

Activity monitoring is divided into 128-ms intervals. The accumulator is incremented once for each 128ms interval in which the input clock is inactive for more than two cycles (more than four cycles for 125 MHz, 62.5 MHz, 25 MHz and 10 MHz input clocks). Thus the “fill” rate of the bucket is at most 1 unit per 128 ms, or approximately 8 units/second. During each period of 1, 2, 4 or 8 intervals (programmable), the accumulator decrements if no irregularities occur. Thus the “leak” rate of the bucket is approximately 8, 4, 2 or 1 units/second. A leak is prevented when a fill event occurs in the same interval.

When the value of an accumulator reaches the alarm threshold (**LBxU** register), the corresponding ACT alarm bit is set to 1 in the **ISR** registers, and the clock is marked invalid in the **VALSR** registers. When the value of an accumulator reaches the alarm clear threshold (**LBxL** register), the activity alarm is cleared by clearing the clock's ACT bit. The accumulator cannot increment past the size of the bucket specified in the **LBxS** register. The decay rate of the accumulator is specified in the **LBxD** register. The values stored in the leaky bucket configuration registers must have the following relationship at all times:  $LBxS \geq LBxU > LBxL$ .

When the leaky bucket is empty, the minimum time to declare an activity alarm in seconds is  $LB0U / 8$ . The minimum time to clear an activity alarm in seconds is  $2^{LB0D} * (LB0S - LB0L) / 8$ . As an example, assume  $LB0U = 8$ ,  $LB0L = 1$ ,  $LB0S = 10$  and  $LB0D = 0$ . The minimum time to declare an activity alarm would be  $8 / 8 = 1$  second. The minimum time to clear the activity alarm would be  $2^0 * (10 - 1) / 8 = 1.125$  seconds.

### 7.5.3 Selected Reference Activity Monitoring

The input clock the T0 DPLL is currently locked to is called the selected reference. The quality of the DPLL's selected reference is exceedingly important, since missing cycles and other anomalies on the selected reference can cause unwanted jitter, wander or frequency offset on the output clocks. When anomalies occur on the selected reference they must be detected as soon as possible to give the DPLL opportunity to temporarily disconnect from the reference until the reference is available again. By design, the regular input clock activity monitor (section 7.5.2) is too slow to be suitable for monitoring the selected reference. Instead, the DPLL has a fast activity monitor that detects that the frequency is within range (approximately 10,000 ppm) and detects inactivity within approximately two missing reference clock cycles (approximately four missing cycles for 125 MHz, 62.5 MHz, 25 MHz and 10 MHz references).

When the T0 DPLL detects a no-activity event, it immediately enters mini-holdover mode to isolate itself from the selected reference and sets the SRFAIL latched status bit in **MSR2**. The setting of the SRFAIL bit can cause an interrupt request if the corresponding enable bit is set in **IER2**. If **MCR10:SRFPIN=1**, the SRFAIL output pin follows the state of the SRFAIL status bit. When **PHLIM1:NALOL=0** (default), the T0 DPLL does not declare loss-of-lock during no-activity events. If the selected reference becomes available again before any alarms are declared by the activity monitor, then the T0 DPLL continues to track the selected reference using nearest-edge locking ( $\pm 180^\circ$ ) to avoid cycle slips. When **NALOL=1**, the T0 DPLL declares loss-of-lock during no-activity events. This causes the T0 DPLL state machine to transition to the loss-of-lock state, which sets the **MSR2:STATE** bit and causes an interrupt request if enabled. If the selected reference becomes available again before any alarms are declared by the activity monitor, then the T0 DPLL tracks the selected reference using phase/frequency locking ( $\pm 360^\circ$ ) until phase lock is reestablished.

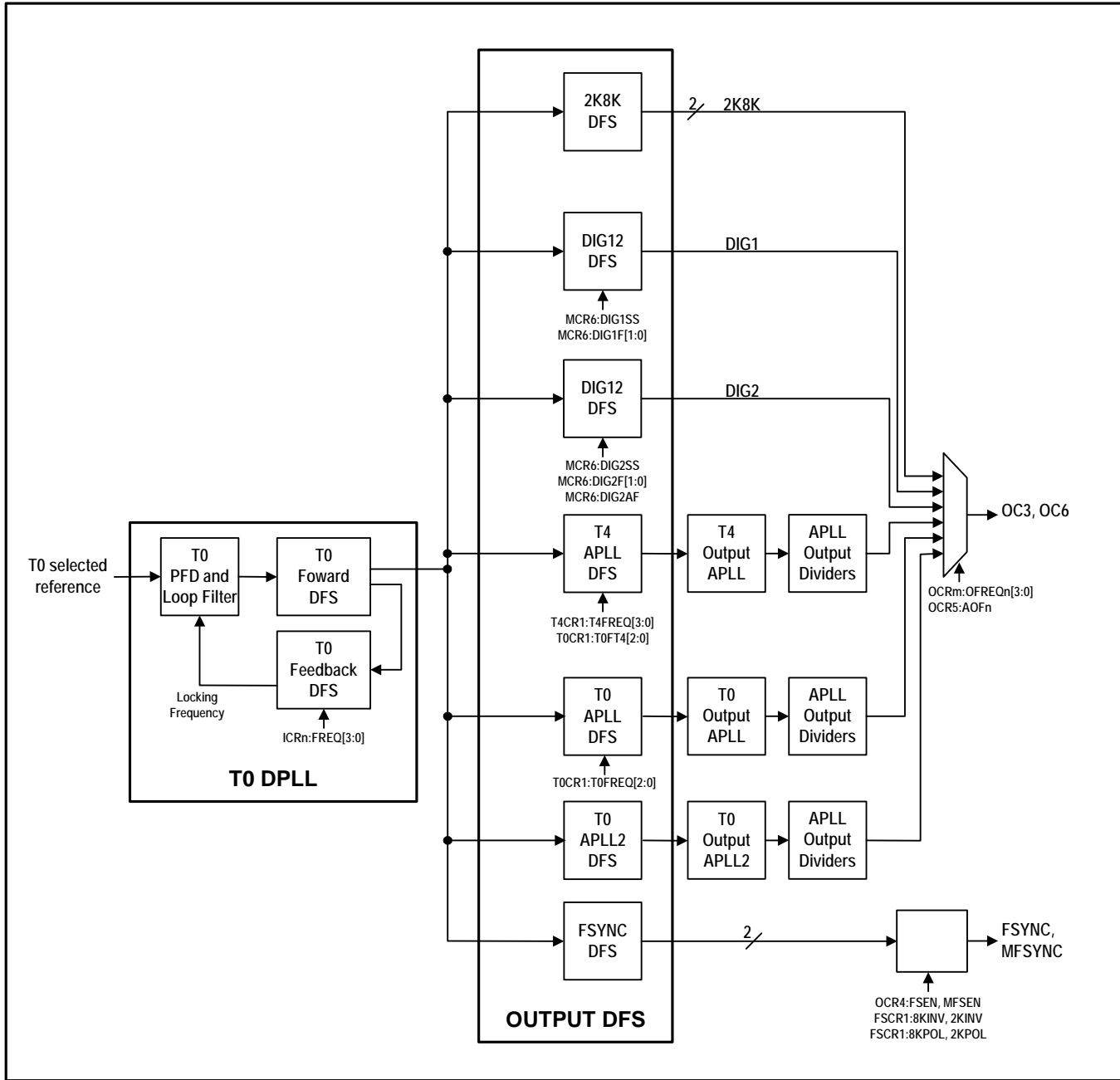
## 7.6 Input Clock Selection and Switching

The SRCSW input pin controls reference switching between two clock inputs. In this mode, if the SRCSW pin is high, the T0 DPLL is forced to lock to input IC3. If the SRCSW pin is low the device is forced to lock to input IC4. The currently selected reference is indicated in the **PTAB1:SELREF** field.

### 7.7 DPLL Architecture and Configuration

The T0 DPLL is a digital PLL with analog PLLs (APLLs) as output stages as well as some outputs that are not cleaned up by an APLL. This architecture combines the benefits of both PLL types. See [Figure 7-1](#).

**Figure 7-1. DPLL Block Diagram**



Digital PLLs have two key benefits: (1) stable, repeatable performance that is insensitive to process variations, temperature and voltage, and (2) flexible behavior that is easily programmed via configuration registers. DPLLs use digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8 MHz) is multiplied up from the 12.800 MHz local oscillator clock applied to the REFCLK pin. This master clock is then digitally divided down to the desired output frequency. The DFS output clock has jitter of about 1 nsec pk-pk.

The analog PLLs filter the jitter from the DPLL, reducing the 1 ns pk-pk jitter to less than 0.5 ns pk-pk and 60 ps RMS, typical, measured broadband (10 Hz to 1 GHz).

The DPLL in the device is configurable for many PLL parameters including bandwidth, damping factor, input frequency, pull-in/hold-in range and more. No knowledge of loop equations or gain parameters is required to configure and operate the device. No external components are required for the DPLL or the APLLs except the high-quality local oscillator connected to the REFCLK pin.

The DPLL has a full free-run/locked/holdover state machine and full programmability.

### 7.7.1 T0 DPLL State Machine

The T0 DPLL has three main timing modes: locked, holdover and free-run. The control state machine for the T0 DPLL has states for each timing mode as well as three temporary states: pre-locked, pre-locked 2 and loss-of-lock. The state transition diagram is shown in [Figure 7-2](#). Descriptions of each state are given in the paragraphs below. During normal operation the state machine controls state transitions. When necessary, however, the state can be forced using the T0STATE field of the [MCR1](#) register.

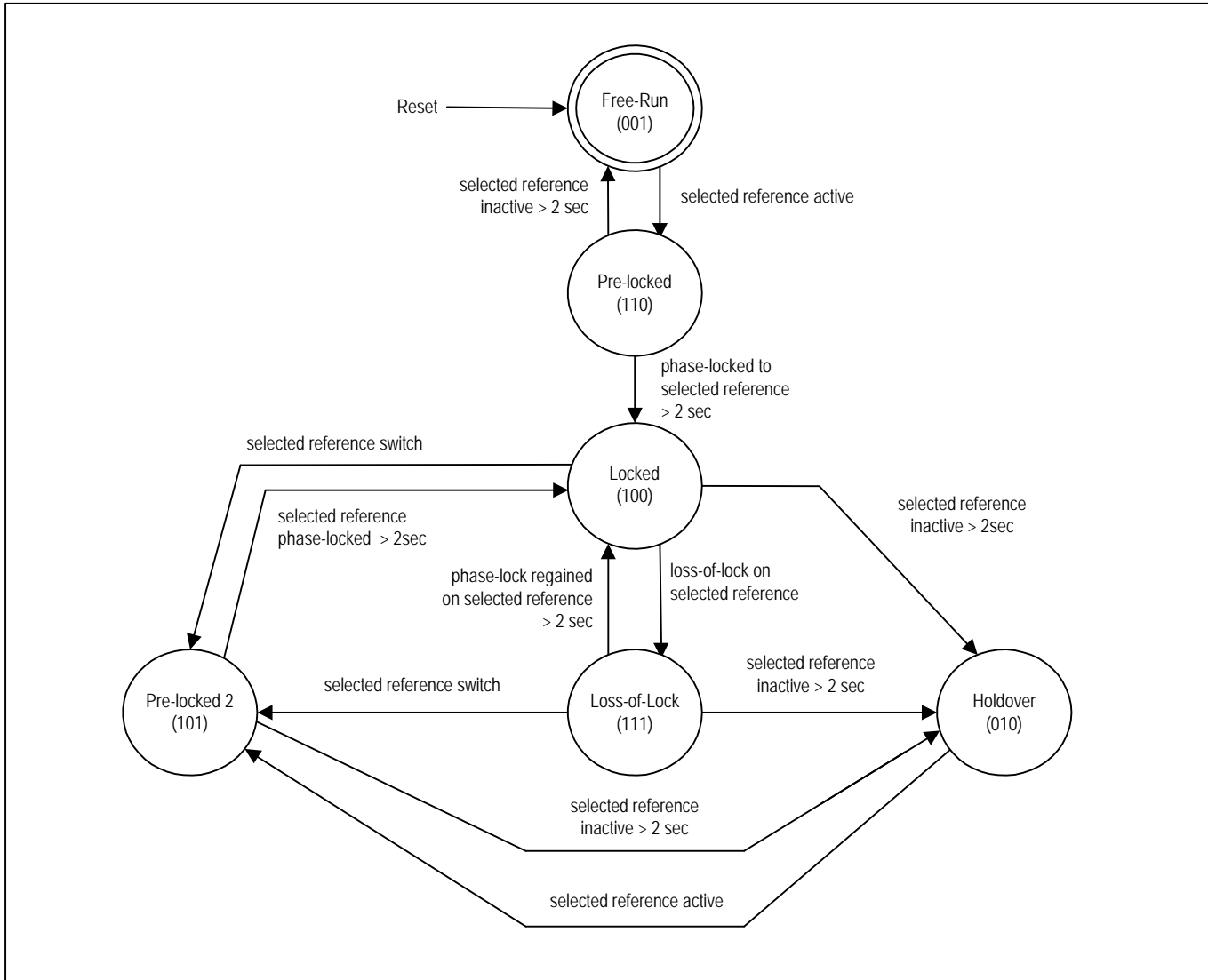
Whenever the T0 DPLL changes state, the STATE bit in [MSR2](#) is set, which can cause an interrupt request if enabled. The current T0 DPLL state can be read from the T0STATE field of the [OPSTATE](#) register.

#### 7.7.1.1 Free-Run State

Free-run mode is the reset default state. In free-run all output clocks are derived from the 12.800 MHz local oscillator attached to the REFCLK pin. The frequency of each output clock is a specific multiple of the local oscillator. The frequency accuracy of each output clock is equal to the frequency accuracy of the master clock, which can be calibrated using the MCLKFREQ field in registers [MCLK1](#) and [MCLK2](#) (see section [7.3](#)). The state machine transitions from free-run to the pre-locked state when the selected reference becomes active.

#### 7.7.1.2 Prelocked State

If phase lock (see section [7.7.5](#)) is achieved for at least 2 seconds then the state machine transitions to locked mode. If the selected reference becomes inactive for 2 seconds then the state machine transitions back to the free-run state.

**Figure 7-2. T0 DPLL State Transition Diagram****Notes:**

- Phase lock is declared internally when the DPLL has maintained phase lock continuously for approximately 1 to 2 seconds.
- When selected reference is invalid and the DPLL is not in freerun or holdover, the DPLL is in a temporary holdover state.

**7.7.1.3 Locked State**

The T0 DPLL state machine can reach the locked state from the pre-locked, pre-locked 2 or loss-of-lock states when the DPLL has locked to the selected reference for at least two seconds (see section 7.7.5). In the locked state the output clocks track the phase and frequency of the selected reference.

If the `MCR1.LOCKPIN` bit is set, the LOCK pin is driven high when the T0 DPLL is in the Locked state.

While in the locked state, if the selected reference becomes inactive, then an activity alarm is raised (corresponding ACT bit set in the `ISR` register), the selected reference is marked invalid (ICn bit goes low in `VALSR` register) and the LOS pin is asserted. If the input stays inactive for 2 seconds then the state machine transitions to the holdover state. If the DPLL is switched to the other input and that input is active then the state machine transitions to the pre-locked 2 state.

**7.7.1.4 Loss-of-Lock State**

When the loss-of-lock detectors (see section 7.7.5) indicate loss of phase lock, the state machine immediately transitions from the locked state to the loss-of-lock state. If phase lock is regained for more than 2 seconds while in the loss-of-lock state then the state machine transitions back to the locked state.

While in the loss-of-lock state, if the selected reference becomes inactive then an activity alarm is raised (corresponding ACT bit set in the [ISR](#) register), the selected reference is marked invalid (ICn bit goes low in [VALSR](#) register) and the LOS pin is asserted. If the input stays inactive for 2 seconds then the state machine transitions to the holdover state. If the DPLL is switched to the other input and that input is valid then the state machine switches to the pre-locked 2 state.

#### 7.7.1.5 Prelocked 2 State

The pre-locked and pre-locked 2 states are similar. If phase lock (see section [7.7.5](#)) is achieved for more than 2 seconds then the state machine transitions to locked mode. While in the pre-locked 2 state, if the selected reference becomes inactive then an activity alarm is raised (corresponding ACT bit set in the [ISR](#) register), the selected reference is marked invalid (ICn bit goes low in [VALSR](#) register) and the LOS pin is asserted. If the input stays inactive for 2 seconds then the state machine transitions to the holdover state.

#### 7.7.1.6 Holdover State

The device reaches the holdover state when it declares its selected reference inactive for 2 seconds. During holdover the T0 DPLL is not phase locked to any input clock but instead generates its output frequency based on previous frequencies while it was locked. When the selected reference becomes active the state machine immediately transitions from holdover to the pre-locked 2 state and tries to lock to selected reference.

##### 7.7.1.6.1 Automatic Holdover

For automatic holdover (FRUNHO=0 in [MCR3](#)), the device can be further configured for instantaneous mode or averaged mode. In *instantaneous mode* (AVG=0 in [HOCR3](#)), the holdover frequency is set to the DPLL's current frequency 50 to 100 ms before entry into holdover (i.e. the value of the FREQ field in the [FREQ1](#), [FREQ2](#) and [FREQ3](#) registers). The FREQ field is the DPLL's integral path and therefore is an average frequency with a rate of change inversely proportional to the DPLL bandwidth. The DPLL's proportional path is not used in order to minimize the effect of recent phase disturbances on the holdover frequency.

In *averaged mode* (AVG=1 in [HOCR3](#) and FRUNHO=1 in [MCR3](#)), the holdover frequency is set to an internally averaged value. During locked operation the frequency indicated in the FREQ field is internally averaged over a one-second period. The T0 DPLL indicates that it has acquired a valid holdover value by setting the HORDY status bit in [MSR4](#) (latched status). If the T0 DPLL must enter holdover before the 1-second average is available, an instantaneous value 50 to 100 ms old from the integral path is used instead.

##### 7.7.1.6.2 Free-Run Holdover

For free-run holdover (FRUNHO=1 in [MCR3](#)), the output frequency accuracy is generated with the accuracy of the external oscillator frequency. The actual frequency is the frequency of the external oscillator plus the value of the MCLK offset specified in the MCLKFREQ field in registers [MCLK1](#) and [MCLK2](#) (see section [7.3](#)). When [MCR3.FRUNHO](#) is set the [HOCR3:AVG](#) bit is ignored.

##### 7.7.1.7 Mini-Holdover

When the selected reference fails, the fast activity monitor (section [7.5.3](#)) isolates the T0 DPLL from the reference within one or two clock cycles to avoid adverse effects on the DPLL frequency. When this fast isolation occurs, the DPLL enters a temporary mini-holdover mode, with a frequency equal to an instantaneous value 50 to 100 ms old from the integral path of the loop filter. Mini-holdover lasts until the selected reference becomes active or the state machine enters the holdover state. If the free-run holdover mode is set (FRUNHO=1 in [MCR3](#)), the mini-holdover frequency accuracy is exactly the same as the external oscillator accuracy plus the offset set by the MCLKFREQ field in registers [MCLK1](#) and [MCLK2](#) (see section [7.3](#)).

## 7.7.2 Bandwidth

The bandwidth of the T0 DPLL is configured in the [T0ABW](#) and [T0LBW](#) registers for various values from 18 Hz to 400 Hz. The AUTOBW bit in the [MCR9](#) register controls automatic bandwidth selection. When AUTOBW=1, the T0 DPLL uses the T0ABW bandwidth during acquisition (not phase locked) and the T0LBW bandwidth when phase locked. When AUTOBW=0 the T0 DPLL uses the T0LBW bandwidth all the time, both during acquisition and when phase locked.

When LIMINT=1 in the [MCR9](#) register, the DPLL's integral path is limited (i.e. frozen) when the DPLL reaches minimum or maximum frequency. Setting LIMINT=1 minimizes overshoot when the DPLL is pulling in.

### 7.7.3 Damping Factor

The damping factor for the T0 DPLL is configured in the DAMP field of the [T0CR2](#) register. The reset default damping factor is chosen to give a maximum jitter/wander gain peak of approximately 0.1 dB. Available settings are a function of DPLL bandwidth (configured in the [TOABW](#) and [T0LBW](#) registers). See [Table 7-4](#).

**Table 7-4. Damping Factors and Peak Jitter/Wander Gain**

Bandwidth	DAMP[2:0] Value	Damping Factor	Gain Peak, dB
18 Hz	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 to 400 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

### 7.7.4 Phase Detectors

Phase detectors are used to compare a PLL's feedback clock with its input clock. Several phase detectors are available in the T0 DPLL:

- Phase/frequency detector (PFD)
- Early/late phase detector (PD2) for fine resolution
- Multi-cycle phase detector (MCPD) for large input jitter tolerance and/or faster lock times

These detectors can be used in combination to give fine phase resolution combined with large jitter tolerance. As with the rest of the DPLL logic, the phase detectors operate at input frequencies up to 77.76 MHz. The multi-cycle phase detector detects and remembers phase differences of many cycles (up to 8191 UI). When locking to 8 kHz or lower, the normal phase/frequency detectors are always used.

The T0 DPLL phase detectors can be configured for normal phase/frequency locking ( $\pm 360^\circ$  capture) or nearest-edge phase locking ( $\pm 180^\circ$  capture). With nearest-edge detection the phase detectors are immune to occasional missing clock cycles. The DPLL automatically switches to nearest-edge locking when the multi-cycle phase detector is disabled and the other phase detectors determine that phase lock has been achieved. Setting [D180=1](#) in the [TEST1](#) register disables nearest-edge locking and forces the T0 DPLL to use phase/frequency locking.

The early/late phase detector, also known as phase detector 2, is enabled and configured in the PD2\* fields of registers [T0CR2](#). The reset default settings of these registers are appropriate for all operating modes. Adjustments only affect small signal overshoot and bandwidth.

The multicycle phase detector is enabled by setting [MCPDEN=1](#) in the [PHLIM2](#) register. The range of the MCPD—from  $\pm 1$  UI up to  $\pm 8191$  UI—is configured in the [COARSELIM](#) field of [PHLIM2](#). The MCPD tracks phase position over many clock cycles, giving high jitter tolerance. Thus the use of the MCPD is an alternative to the use of [LOCK8K](#) mode for jitter tolerance. When the DPLL is direct locking to 8 kHz, 4 kHz or 2 kHz or in [LOCK8K](#) mode, the multi-cycle phase detector is automatically disabled.

When [USEMCPD=1](#) in [PHLIM2](#), the MCPD is used in the DPLL loop, giving faster pull-in but more overshoot. In this mode the loop has similar behavior to [LOCK8K](#) mode. In both cases large phase differences contribute to the dynamics of the loop. When enabled by [MCPDEN=1](#), the MCPD tracks the phase position whether or not it is used in the DPLL loop.

When the input clock is divided before being sent to the phase detector, the divider output clock edge gets aligned to the feedback clock edge before the DPLL starts to lock to a new input clock signal or after the input clock signal

has a temporary signal loss. This helps ensure locking to the nearest input clock edge which reduces output transients and decreases lock times.

### 7.7.5 Loss of Phase Lock Detection

Loss of phase lock can be triggered by any of the following in both the T0 DPLL:

- The fine phase lock detector (measures phase between input and feedback clocks)
- The coarse phase lock detector (measures whole cycle slips)
- Hard frequency limit detector
- Inactivity detector

The fine phase lock detector is enabled by setting FLEN=1 in the [PHLIM1](#) register. The fine phase limit is configured in the FINELIM field of [PHLIM1](#).

The coarse phase lock detector is enabled by setting CLEN=1 in the [PHLIM2](#) register. The coarse phase limit is configured in the COARSELIM field of [PHLIM2](#). This coarse phase lock detector is part of the multi-cycle phase detector (MCPD) described in section 7.7.4. The COARSELIM field sets both the MCPD range and the coarse phase limit, since the two are equivalent. If loss of phase lock should not be declared for multiple-UI input jitter then the fine phase lock detector should be disabled and the coarse phase lock detector should be used instead.

The hard frequency limit detector is enabled by setting FLLOL=1 in the [DLIMIT3](#) register. The hard limit is configured in registers [DLIMIT1](#) and [DLIMIT2](#). When the DPLL frequency reaches the hard limit, loss-of-lock is declared. The [DLIMIT3](#) register also has the SOFTLIM field to specify a soft frequency limit. Exceeding the soft frequency limit does not cause loss-of-lock to be declared. When the T0 DPLL frequency reaches the soft limit the TOSOFT status bit is set in the [OPSTATE](#) register. Both the SOFT and HARD alarm limits have hysteresis as required by GR-1244.

The inactivity detector is enabled by setting NALOL=1 in the [PHLIM1](#) register. When this detector is enabled the DPLL declares loss-of-lock after one or two missing clock cycles on the selected reference. See section 7.5.3.

When the T0 DPLL declares loss of phase lock, the state machine immediately transitions to the loss-of-lock state, which sets the STATE bit in the [MSR2](#) register and requests an interrupt if enabled.

### 7.7.6 Frequency and Phase Measurement

Accurate measurement of frequency and phase can be accomplished using the T0 DPLL. The REFCLK signal accuracy after being adjusted with MCLKFREQ is used for the frequency reference.

DPLL frequency measurements can be read from the FREQ field spanning registers [FREQ1](#), [FREQ2](#) and [FREQ3](#). This field indicates the frequency of the selected reference. This frequency measurement has a resolution of 0.0003068 ppm over a  $\pm 80$  ppm range. The value read from the FREQ field is the DPLL's integral path value, which is an averaged measurement with an averaging time inversely proportional to DPLL bandwidth.

DPLL phase measurements can be read from the PHASE field spanning registers [PHASE1](#) and [PHASE2](#). This field indicates the phase difference seen by the phase detector. This phase measurement has a resolution of approximately 0.703 degrees and is internally averaged with a -3 dB attenuation point of approximately 100 Hz. Thus for low DPLL bandwidths the PHASE field gives input phase wander in the frequency band from the DPLL corner frequency up to 100 Hz. This information could be used by software to compute a crude MTIE measurement.

### 7.7.7 Input Jitter Tolerance

The device is compliant with the jitter tolerance requirements of the standards listed in [Table 1-1](#). When using the  $\pm 360^\circ / \pm 180^\circ$  PFD, jitter can be tolerated up to the point of eye closure. Either LOCK8K mode (see section 7.4.2.2) or the multi-cycle phase detector (see section 7.7.4) should be used for high jitter tolerance.

### 7.7.8 Jitter Transfer

The transfer of jitter from the selected reference to the output clocks has a programmable transfer function that is determined by the DPLL bandwidth. (See section 7.7.2.) In the T0 DPLL, the 3-dB corner frequency of the jitter transfer function can be set to any of 13 positions from 0.1 Hz to 400 Hz.

### 7.7.9 Output Jitter and Wander

Several factors contribute to jitter and wander on the output clocks, including:

- Jitter and wander amplitude on the selected reference (while in the locked state)
- The jitter transfer characteristic of the device (while in the locked state)
- The jitter and wander on the local oscillator clock signal (especially wander while in the holdover state)

The DPLL in the device has programmable bandwidth (see section 7.7.2). With respect to jitter, the DPLL behaves as a low-pass filter with a programmable pole. The bandwidth of the DPLL is low enough to strongly attenuate most jitter.

## 7.8 Output Clock Configuration

A total of 4 output clock pins, OC3, OC6, FSYNC and MFSYNC are available on the device. Output clocks OC3 and OC6 are individually configurable for a variety of frequencies. Output clocks FSYNC and MFSYNC are more specialized, serving as an 8 KHz frame sync (FSYNC), and a 2 KHz multi-frame sync (MFSYNC). Table 7-5 provides more detail on the capabilities of the output clock pins.

**Table 7-5. Output Clock Capabilities**

Output Clock	Signal Format	Frequencies Supported
OC3	CMOS/TTL	Frequency selection per section 7.8.2.3 and Table 7-6 through Table 7-12
OC6	LVDS/PECL	
OC10	CMOS/TTL	8 KHz frame sync with programmable pulse width and polarity
OC11		2 KHz multiframe sync with programmable pulse width and polarity

### 7.8.1 Signal Format Configuration

Output clock OC6 is an LVDS compatible, LVPECL level-compatible output. The type of output can be selected or the output can be disabled using the OC6SF configuration bits in the MCR8 register. The LVPECL level-compatible mode generates a differential signal that is large enough for most LVPECL receivers. Some LVPECL receivers have a limited common mode signal range which can be accommodated for by using an AC coupled signal. The LVDS electrical specifications are listed in Table 10-4, and the recommended LVDS termination is shown in Figure 10-1. The LVPECL level-compatible electrical specifications are listed in Table 10-5, and the recommended LVPECL receiver termination is shown in Figure 10-2. This differential output can be easily interfaced to an LVDS, LVPECL or CML input on a neighboring IC using a few external passive components. See [Maxim App Note HFAN-1.0](#) for details.

Output clocks OC3, FSYNC, and MFSYNC are CMOS/TTL signal format.

### 7.8.2 Frequency Configuration

The frequency of output clocks OC3 and OC6 is a function of the settings used to configure the components of the T0 PLL paths. These components are shown in the detailed block diagram of Figure 7-1.

The DS3106 uses digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8 MHz) is divided down to the desired output frequency by adding a number to an accumulator. The DFS output is a coding of the clock output phase which is used by a special circuit to determine where to put the edges of the output clock between the clock edges of the master clock. The edges of the output clock, however, are not ideally located in time resulting in jitter with an amplitude typically less than 1 nsec pk-pk.

#### 7.8.2.1 T0 DPLL and Feedback DFS Details

See Figure 7-1. The T0 forward DFS block use the 204.8 MHz master clock and DFS technology to synthesize internal clocks from which the output and feedback clocks are derived. The feedback DFS block synthesizes the appropriate locking frequency for use by the input phase-frequency detector (PFD). See section 7.4.2.

#### 7.8.2.2 Output DFS and APLL Details

See Figure 7-1. The output clock frequencies are determined by two 2kHz/8kHz DFS blocks, two DIG12 DFS blocks and three APLL DFS blocks. The T0 APLL, the T0 APLL2 and the T4 APLL (and their output dividers) get

their frequency references from three associated APLL DFS blocks. All of the output DFS blocks are connected to the T0 DPPLL..

The 2K8K DFS and FSYNC DFS blocks generate both 2 kHz and 8 kHz signals which have about 1 ns pk-pk jitter. The FSYNC (8 kHz) and MFSYNC(2 kHz) signals come from the FSYNC DFS block. The 2kHz and 8 kHz signals that can be output on OC3 or OC6 always come from the 2K8K DFS..

The DIG1 DFS can generate an NxDS1 or NxE1 signal with about 1 ns pk-pk jitter. The DIG2 DFS can generate an NxDS1, NxE1, 6.312 MHz, 10 MHz or Nx19.44 MHz clock with approximately 1 ns pk-pk jitter. The frequency of the DIG1 clock is configured by the DIG1SS bit in [MCR6](#) and the DIG1F[1:0] field in [MCR7](#). The frequency of the DIG2 clock is configured by the DIG2AF and DIG2SS bits in [MCR6](#) and the DIG2F[1:0] field in [MCR7](#). DIG1 and DIG2 can be independently configured for any of the frequencies shown in [Table 7-6](#) and [Table 7-7](#), respectively.

The APLL DFS blocks and their associated output APLLs and output dividers can generate many different frequencies. The T0 APLL frequencies that can be generated are listed in [Table 7-9](#). The T0 APLL2 frequency is always 312.500 MHz. The T4 APLL frequencies that can be generated are listed in [Table 7-11](#). The output frequencies that can be generated from the APLL circuits are listed in [Table 7-8](#).

### 7.8.2.3 OC3 and OC6 Configuration

The following is a step-by-step procedure for configuring the frequencies of output clocks OC3 and OC6:

1. Use [Table 7-8](#) to select a set of output frequencies for each APLL, T0 and T4. Each APLL can only generate one set of output frequencies. (In SONET/SDH equipment the T0 APLL is typically configured for a frequency of 311.04 MHz in order to get Nx19.44 MHz output clocks for use on line cards.)
2. Determine from [Table 7-8](#) the T0 and T4 APLL frequencies required for the frequency sets chosen in step 2.
3. Configure the T0FREQ field in register T0CR1 as shown in [Table 7-9](#) for the T0 APLL frequency determined in step 3. Configure fields T4CR1:T4FREQ, T0CR1:T4APT0 and T0CR1:T0FT4 as shown in [Table 7-11](#) for the T4 APLL frequency determined in step 3.
4. Using [Table 7-8](#) and [Table 7-12](#), configure the frequencies of output clocks OC3 and OC6 in the OFREQn fields of registers [OCR2](#) and [OCR4](#) and the AOFn bits in the [OCR5](#) register.

[Table 7-13](#) lists all possible frequencies for the output clocks and specifies how to configure the T0 APLL and/or the T4 APLL to obtain each frequency. [Table 7-13](#) also indicates the expected jitter amplitude for each frequency.

**Table 7-6. Digital1 Frequencies**

DIG1F[1:0] Setting in <a href="#">MCR7</a>	DIG1SS Setting in <a href="#">MCR6</a>	Frequency, MHz	Jitter, pk-pk nsec, typical
00	0	2.048	< 1
01	0	4.096	< 1
10	0	8.192	< 1
11	0	16.384	< 1
00	1	1.544	< 1
01	1	3.088	< 1
10	1	6.176	< 1
11	1	12.352	< 1

Table 7-7. Digital2 Frequencies

DIG2AF Setting in MCR6	DIG2F[1:0] Setting in MCR7	DIG2SS Setting in MCR6	Frequency, MHz	Jitter, pk-pk nsec, typical
1	00	0	6.312	< 1
1	10	0	10.000	<1
1	00	1	19.440	< 1
1	01	1	38.880	< 1
0	00	0	2.048	< 1
0	01	0	4.096	< 1
0	10	0	8.192	< 1
0	11	0	16.384	< 1
0	00	1	1.544	< 1
0	01	1	3.088	< 1
0	10	1	6.176	< 1
0	11	1	12.352	< 1

Table 7-8. APLL Frequency to Output Frequencies (T0 APLL and T4 APLL)

APLL Frequency	APLL / 2	APLL / 4	APLL / 5	APLL / 6	APLL / 8	APLL / 10	APLL / 12	APLL / 16	APLL / 20	APLL / 48	APLL / 64
312.5	<b>156.25</b>	--	<b>62.5</b>	--	--	31.25	--	--	--	--	--
311.04	<b>155.52</b>	<b>77.76</b>	62.208	<b>51.84</b>	<b>38.88</b>	31.104	25.92	<b>19.44</b>	15.552	<b>6.48</b>	4.86
274.944	137.472	68.376	--	45.824	<b>34.368</b>	--	22.912	17.184	--	5.728	4.296
250	<b>125</b>	<b>62.5</b>	50	--	31.25	<b>25</b>	--	--	12.5	--	--
178.944	89.472	<b>44.736</b>	--	29.824	22.368	--	14.912	11.184	--	3.728	2.796
160	80	40	32	--	20	16	--	<b>10</b>	8	--	2.5
148.224	74.112	37.056	--	24.704	18.528	--	12.352	9.264	--	<b>3.088</b>	2.316
131.072	65.536	<b>32.768</b>	--	--	<b>16.384</b>	--	--	<b>8.192</b>	--	--	<b>2.048</b>
122.88	61.44	<b>30.72</b>	24.576	20.48	15.36	12.288	<b>10.24</b>	7.68	6.144	2.56	1.92
104	52	26	20.8	--	<b>13</b>	10.4	--	6.5	5.2	--	--
100.992	50.496	25.248	--	16.832	12.624	--	8.416	<b>6.312</b>	--	2.104	1.578
98.816	49.408	24.704	--	--	12.352	--	--	<b>6.176</b>	--	--	<b>1.544</b>
98.304	49.152	24.576	--	<b>16.384</b>	12.288	--	<b>8.192</b>	6.144	--	<b>2.048</b>	1.536

All frequencies in MHz. Common telecom, datacom and synchronization frequencies are in **bold** type.

Table 7-9. T0 APLL Frequency Configuration

T0 APLL Frequency, MHz	T0 APLL DFS Frequency, MHz	T0 APLL Frequency Mode	T0FREQ[2:0] Setting in TOCR1	Output Jitter, pk-pk, ns, typ
311.04	77.76	77.76 MHz	000	< 0.5
311.04	77.76	77.76 MHz	001	< 0.5
98.304	24.576	12 x E1	010	< 0.5
131.072	32.768	16 x E1	011	< 0.5
148.224	37.056	24 x DS1	100	< 0.5
98.816	24.704	16 x DS1	101	< 0.5
100.992	25.248	4 x 6312 kHz	110	< 0.5
250.000	62.5	GbE ÷ 16	111	< 0.5

Table 7-10. T0 APLL2 Frequency Configuration

T0 APLL2 Frequency, MHz	T0 APLL2 DFS Frequency, MHz	Output Jitter, pk-pk, ns, typ
312.500	62.500	<0.5

**Table 7-11. T4 APLL Frequency Configuration**

T4 APLL Frequency, MHz	T4 APLL DFS Freq, MHz	T4 APLL Frequency Mode	T4APT0 Setting in T0CR1	T4FREQ[3:0] Setting in T4CR1	T0FT4[2:0] Setting in T0CR1	Output Jitter, pk-pk, ns, typ
Disabled	77.76	Squelched	0	0000	XXX	< 0.5
311.04	77.76	77.76 MHz	0	0001	XXX	< 0.5
98.304	24.576	12 x E1	0	0010	XXX	< 0.5
131.072	32.768	16 x E1	0	0011	XXX	< 0.5
148.224	37.056	24 x DS1	0	0100	XXX	< 0.5
98.816	24.704	16 x DS1	0	0101	XXX	< 0.5
274.944	68.736	2 x E3	0	0110	XXX	< 0.5
178.944	44.736	DS3	0	0111	XXX	< 0.5
100.992	25.248	4 x 6312 kHz	0	1000	XXX	< 0.5
250.000	62.500	GbE ÷ 16	0	1001	XXX	< 0.5
122.88	30.720	3 x 10.24	0	1010	XXX	< 0.5
160.000	40.000	4 x 10	0	1011	XXX	< 0.5
104.000	26.000	2 x 13	0	1100	XXX	< 0.5
98.304	24.576	T0 12 x E1	1	XXXX	000	< 0.5
250.000	62.500	T0 GbE ÷ 16	1	XXXX	001	< 0.5
131.072	32.768	T0 16 x E1	1	XXXX	010	< 0.5
148.224	37.056	T0 24 x DS1	1	XXXX	100	< 0.5
98.816	24.704	T0 16 x DS1	1	XXXX	110	< 0.5
100.992	25.248	T0 4 x 6312 kHz	1	XXXX	111	< 0.5

**Table 7-12. OC3 and OC6 Output Frequency Selection**

AOF Bit	OFREQ <sup>(1)</sup>	OC3 Frequency	OC6 Frequency
0	0000	disabled	disabled
0	0001	2 kHz	2 kHz
0	0010	8 kHz	8 kHz
0	0011	Digital2	T0 / 2
0	0100	Digital1	Digital1
0	0101	T0 / 48	T0 / 1
0	0110	T0 / 16	T0 / 16
0	0111	T0 / 12	T0 / 12
0	1000	T0 / 8	T0 / 8
0	1001	T0 / 6	T0 / 6
0	1010	T0 / 4	T0 / 4
0	1011	T4 / 64	T4 / 64
0	1100	T4 / 48	T4 / 48
0	1101	T4 / 16	T4 / 16
0	1110	T4 / 8	T4 / 8
0	1111	T4 / 4	T4 / 4
1	0000	disabled	disabled
1	0001	T0 / 64	T4 / 5
1	0010	T4 / 20	T4 / 2
1	0011	T4 / 12	T4 / 1
1	0100	T4 / 10	T02 / 5
1	0101	T4 / 5	T02 / 2
1	0110	T4 / 2	T02 / 1

Note 1: The value of the OFREQn field (in the [OCR2](#) and [OCR3](#) registers) corresponding to output clock OCn.

**Table 7-13. Standard Frequencies for Programmable Outputs**

Frequency, MHz		T0 APLL		T4 APLL		OFREQn	Jitter (typ)	
		T0FREQ	T4FT0	T4FREQ	rms (ps)		pk-pk (ns)	
<b>2 kHz</b>						2 kHz	100	1.00
<b>8 kHz</b>						8 kHz	100	1.00
1.536	not OC6 from T0 APLL	12 x E1	12 x E1	12 x E1		APLL/64	50	0.50
<b>1.544</b>	not OC6 from DIG2					DIG1,DIG2	100	1.00
<b>1.544</b>	not OC6 from T0 APLL	16 x DS1	16 x DS1	16 x DS1		APLL/64	50	0.50
1.578	not OC6 from T0 APLL	4 x 6.312	4 x 6.312	4 x 6.312		APLL/64	50	0.50
<b>2.048</b>	not OC6 from DIG2					DIG1,DIG2	100	1.00
<b>2.048</b>	not OC6 from T0 APLL	12 x E1	12 x E1	12 x E1		APLL/48	50	0.50
<b>2.048</b>	not OC6 from T0 APLL	16 x E1	16 x E1	16 x E1		APLL/64	50	0.50
2.104	not OC6 from T0 APLL	4 x 6.312	4 x 6.312	4 x 6.312		APLL/48	50	0.50
2.316	not OC6 from T0 APLL	24 x DS1	24 x DS1	24 x DS1		APLL/64	50	0.50
2.500				4 x 10		APLL/64	50	0.50
2.560				3 x 10.24		APLL/48	50	0.50
2.796				DS3		APLL/64	50	0.50
3.088	not OC6 from DIG2					DIG1,DIG2	100	1.00
3.088	not OC6 from T0 APLL	24 x DS1	24 x DS1	24 x DS1		APLL/48	50	0.50
3.728				DS3		APLL/48	50	0.50
4.096	not OC6 from DIG2					DIG1,DIG2	100	1.00
4.296				2 x E3		APLL/64	50	0.50
4.860	not OC6 from T0 APLL	77.76		77.76		APLL/64	50	0.50
5.200	OC3 only			2 x 13		APLL/20	50	0.50
5.728				2 x E3		APLL/48	50	0.50
6.144	OC3 only			3 x 10.24		APLL/20	50	0.50
6.144		12 x E1	12 x E1	12 x E1		APLL/16	50	0.50
6.176	not OC6 from DIG2					DIG1,DIG2	100	1.00
6.176		16 x DS1	16 x DS1	16 x DS1		APLL/16	50	0.50
<b>6.312</b>	OC3 only					DIG2	100	1.00
<b>6.312</b>		4 x 6.312	4 x 6.312	4 x 6.312		APLL/16	50	0.50
<b>6.480</b>	not OC6 from T0 APLL	77.76		77.76		APLL/48	60	0.6
8.000	OC3 only			4 x 10		APLL/20	50	0.50
8.192	not OC6 from DIG2					DIG1,DIG2	100	1.00
8.192		12 x E1				APLL/12	50	0.50
8.192		16 x E1	16 x E1	16 x E1		APLL/16	50	0.50
8.416		4 x 6.312				APLL/12	50	0.50
9.264		24 x DS1	24 x DS1	24 x DS1		APLL/16	50	0.50
<b>10.000</b>	not OC6					DIG2	100	1.00
<b>10.000</b>				4 x 10		APLL/16	50	0.50
<b>10.240</b>	OC3 only			3 x 10.24		APLL/12	50	0.50
10.400	OC3 only			3 x 10.24		APLL/10	50	0.50
11.184				DS3		APLL/16	50	0.50
12.288		12 x E1	12 x E1	12 x E1		APLL/8	50	0.50
12.288	OC3 only			2 x 13		APLL/10	50	0.50
12.352		24 x DS1				APLL/12	50	0.50
12.352		16 x DS1	16 x DS1	16 x DS1		APLL/8	50	0.50
12.352	not OC6 from DIG2					DIG1,DIG2	100	1.00
12.500	OC3 only			GbE ÷ 16	GbE ÷ 16	APLL/20	50	0.50
12.624		4 x 6.312	4 x 6.312	4 x 6.312		APLL/8	50	0.50
<b>13.000</b>				2 x 13		APLL/8	50	0.50
15.360				3 x 10.24		APLL/8	50	0.50
15.552	OC3 only			77.76		APLL/20	50	0.50
16.000	OC3 only			4 x 10		APLL/10	50	0.50
16.384	not OC6 from DIG2					DIG1,DIG2	100	1.00
16.384		12 x E1				APLL/6	50	0.50
16.384		16 x E1	16 x E1	16 x E1		APLL/8	50	0.50
16.832		4 x 6.312				APLL/6	50	0.50
17.184				2 x E3		APLL/16	50	0.50
18.528		24 x DS1	24 x DS1	24 x DS1		APLL/8	50	0.50
<b>19.440</b>	OC3 only					DIG2	100	1.00

Frequency, MHz	T0 APLL	T4 APLL		OFREQn	Jitter (typ)	
	T0FREQ	T4FT0	T4FREQ		rms (ps)	pk-pk (ns)
<b>19.440</b>	77.76		77.76	APLL/16	50	0.50
20.000			4 x 10	APLL/8	50	0.50
20.800			2 x 13	APLL/5	50	0.50
22.368			DS3	APLL/8	50	0.50
24.576	12 x E1	12 x E1	12 x E1	APLL/4	50	0.50
24.576			3 x 10.24	APLL/5	50	0.50
24.704	24 x DS1			APLL/6	50	0.50
24.704	16 x DS1	16 x DS1	16 x DS1	APLL/4	50	0.50
<b>25.000</b> OC3 only		GbE ÷ 16	GbE ÷ 16	APLL/10	50	0.50
25.248	4 x 6.312	4 x 6.312	4 x 6.312	APLL/4	50	0.50
25.920	77.76			APLL/12	50	0.50
26.000			2 x 13	APLL/4	50	0.50
<b>30.720</b>			3 x 10.24	APLL/4	50	0.50
31.104 OC3 only			77.76	APLL/10	50	0.50
31.250	GbE ÷ 16	GbE ÷ 16	GbE ÷ 16	APLL/8	50	0.50
32.000			4 x 10	APLL/5	50	0.50
32.768	16 x E1	16 x E1	16 x E1	APLL/4	50	0.50
<b>34.368</b>			2 x E3	APLL/8	50	0.50
37.056	24 x DS1	24 x DS1	24 x DS1	APLL/4	50	0.50
<b>38.880</b>	77.76		77.76	APLL/8	50	0.50
40.000			4 x 10	APLL/4	50	0.50
<b>44.736</b>			DS3	APLL/4	50	0.50
49.152 not OC3 from T0 APLL	12 x E1	12 x E1	12 x E1	APLL/2	50	0.50
49.408 not OC3 from T0 APLL	16 x DS1	16 x DS1	16 x DS1	APLL/2	50	0.50
<b>50.000</b>		GbE ÷ 16	GbE ÷ 16	APLL/5	50	0.50
50.496 not OC3 from T0 APLL	4 x 6.312	4 x 6.312	4 x 6.312	APLL/2	50	0.50
<b>51.840</b>	77.76			APLL/6	60	0.6
52.000			2 x 13	APLL/2	50	0.50
61.440			3 x 10.24	APLL/2	50	0.50
62.208			77.76	APLL/5	50	0.50
<b>62.500</b>	GbE ÷ 16	GbE ÷ 16	GbE ÷ 16	APLL/4	50	0.50
<b>62.500</b> OC6 only from T0 APLL2				APLL/5	50	0.50
65.536 not OC3 from T0 APLL	16 x E1	16 x E1	16 x E1	APLL/2	50	0.50
68.736			2 x E3	APLL/4	50	0.50
74.112 not OC3 from T0 APLL	24 x DS1	24 x DS1	24 x DS1	APLL/2	50	0.50
<b>77.76</b>	77.76		77.76	APLL/4	50	0.50
80.000			4 x 10	APLL/2	50	0.50
89.472			DS3	APLL/2	50	0.50
98.304 OC6 only	12 x E1	12 x E1	12 x E1	APLL/1	50	0.50
98.816 OC6 only	16 x DS1	16 x DS1	16 x DS1	APLL/1	50	0.50
100.992 OC6 only	4 x 6312 kHz	4 x 6312 kHz	4 x 6312 kHz	APLL/1	50	0.50
104.000 OC6 only			2 x 13	APLL/1	50	0.50
122.880 OC6 only			3 x 10.24	APLL/1	50	0.50
<b>125.000</b> not OC3 from T0 APLL	GbE ÷ 16	GbE ÷ 16	GbE ÷ 16	APLL/2	50	0.50
131.072 OC6 only	16 x E1	16 x E1	16 x E1	APLL/1	50	0.50
137.472 OC6 only			2 x E3	APLL/2	50	0.50
148.224 OC6 only	24 x DS1	24 x DS1	24 x DS1	APLL/1	50	0.50
<b>155.520</b> not OC3 from T0 APLL	77.76		77.76	APLL/2	50	0.50
<b>156.250</b> OC6 only from T0 APLL2				APLL/2	50	0.50
160.000 OC6 only			4 x 10	APLL/1	50	0.50
178.944 OC6 only			DS3	APLL/1	50	0.50
250.000 OC6 only	GbE ÷ 16			APLL/1	50	0.50
274.944 OC6 only						
<b>311.040</b> OC6 only	77.76			APLL/1	50	0.50
<b>312.500</b> OC6 only from T0 APLL2				APLL/2	50	0.50

### 7.8.2.4 OC3 and OC6 Default Frequency Select Pins

There are two sets of frequency select pins, O3F[2:0] and O6F[2:0], that control the reset default frequencies of the OC3 and OC6 output clock pins, respectively. The SONSDH pin also selects the output frequencies for some of the pin settings. There is also an interaction between O3F[2:0] and O6F[2:0] when O6F[2:0] uses some internal resource that is needed to generate certain frequencies. After reset the O3F[2:0] and O6F[2:0] pins can be used as GPIO pins and status output pins. The default output frequencies are affected by changing the register bit values of four registers: [OCR2](#), [OCR3](#), [T0CR1](#), and [T4CR1](#). The register defaults can be changed after reset using the microprocessor interface.

**Table 7-14 T0FREQ Default Settings**

O6F[2:0]	O3F[2:0]	SONSDH	T0CR1:T0FREQ	
=001	=001	0	010	12 x E1 DFB
		1	100	24 x DS1 DFB
!=001	X	X	001	77.76 AFB
X	!=001	X	001	77.76 AFB

**Table 7-15 T4FREQ Default Settings**

O6F[2:0]	O3F[2:0]	SONSDH	T4CR1:T4FREQ	
=001	X	0	0110	E3
		1	0111	DS3
X	=010	0	0110	E3
		1	0111	DS3
!=001	!=010	0	0011	16 x E1
		1	0101	16 x DS1

**Table 7-16 OC6 Default Frequency Configuration**

O6F[2:0]	SONSDH	Freq MHz	OCR3: OFREQ6	APLL SRC
000	X	0	0000	---
001	0	34.368	1111	T4
	1	44.736	1110	T4
010	X	19.44	0110	T0
011	X	25.92	0111	T0
100*	X	38.88	1000	T0
101	X	51.84	1001	T0
110	X	77.76	1010	T0
111	X	155.52	0011	T0

\* Occurs when O6F[2:0] are left floating.

**Table 7-17 OC3 Default Frequency Configuration**

O3F[2:0]	SONSDH	Freq, MHz	O6F[2:0] =001	OCR2: OFREQ3	APLL SRC
000	X	0	X	0000	---
001	0	2.048	FALSE	1101	T4
	1	1.544		1101	T4
001	0	2.048	TRUE	0111	T0
	1	3.088		0111	T0
010	0	34.736	X	1111	T4
010	1	44.736	X	1110	T4
011*	X	19.44	X	0110	T0
100	X	25.92	X	0111	T0
101	X	38.88	X	1000	T0
110	X	51.84	X	1001	T0
111	X	77.76	X	1010	T0

\* Occurs when O3F[2:0] are left floating.

### 7.8.2.5 FSYNC and MFSYNC Configuration

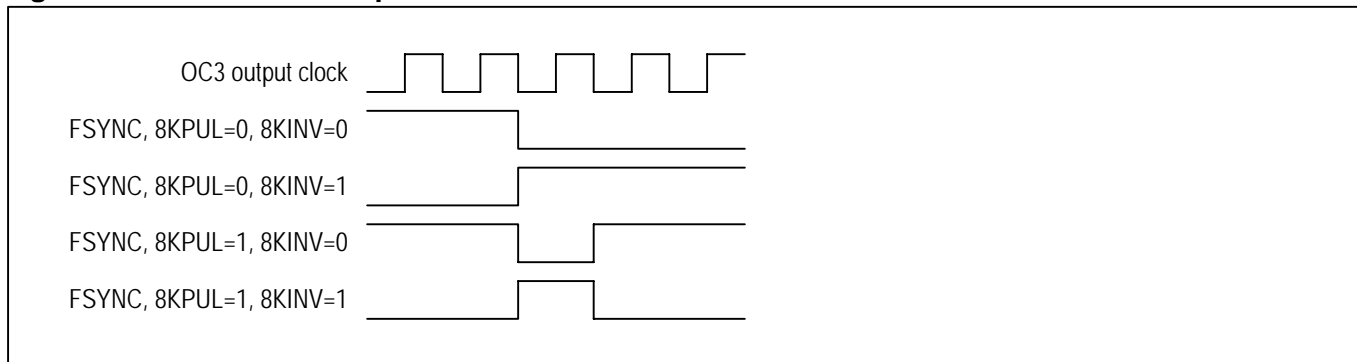
The FSYNC output is enabled by setting FSEN=1 in the [OCR4](#) register, while the MFSYNC output is enabled by setting MFSEN=1 in [OCR4](#). When disabled, these pins are driven low.

When 8KPUL=0 in [FSCR1](#), FSYNC is configured as an 8 kHz clock with 50% duty cycle. When 8KPUL=1, FSYNC is an 8 kHz frame sync that pulses low once every 125  $\mu$ s with pulse width equal to one cycle of output clock OC3. When 8KINV=1 in [FSCR1](#), the clock or pulse polarity of FSYNC is inverted.

When 2KPUL=0 in [FSCR1](#), MFSYNC is configured as an 2 kHz clock with 50% duty cycle. When 2KPUL=1, MFSYNC is a 2 kHz frame sync that pulses low once every 500  $\mu$ s with pulse width equal to one cycle of output clock OC3. When 2KINV=1 in [FSCR1](#), the clock or pulse polarity of MFSYNC is inverted.

If either 8KPUL=1 or 2KPUL=1, then output clock OC3 must be generated from the T0 DPLL and must be configured for a frequency of 1.544 MHz or higher or the FSYNC/MFSYNC pulses may not be generated correctly. [Figure 7-3](#) shows how the 8KPUL and 8KINV control bits affect the FSYNC output. The 2KPUL and 2KINV bits have an identical effect on MFSYNC.

**Figure 7-3. FSYNC 8 kHz Options**



### 7.8.2.6 Custom Output Frequencies

In addition to the many standard frequencies available in the device, any of the seven output DFS blocks can be configured to generate a custom frequency. Possible custom frequencies include any multiple of 2 kHz up to 77.76 MHz and any multiple of 8 kHz up to 311.04 MHz. (An APLL must be used to achieve frequencies above 77.76 MHz.) Any of the programmable output clocks can be configured to output the custom frequency or submultiples thereof. Contact the factory at [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com) for help with custom frequencies.

## 7.9 Microprocessor Interface

The device presents an SPI interface on the  $\overline{CS}$ , SCLK, SDI and SDO pins. SPI is a widely-used master/slave bus protocol that allows a master device and one or more slave devices to communicate over a serial bus. The DS3106 is always a slave device. Masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master device, which also generates the SCLK signal. The DS3106 receives serial data on the SDI pin and transmits serial data on the SDO pin. SDO is high-impedance except when the DS3106 is transmitting data to the bus master.

**Bit Order.** When both bit 3 and bit 4 are low at device address 3FFFh, the register address and all data bytes are transmitted MSB first on both SDI and SDO. When either bit 3 or bit 4 is set to 1 at device address 3FFFh, the register address and all data bytes are transmitted LSB first on both SDI and SDO. The reset default setting and Motorola SPI convention is MSB first.

**Clock Polarity and Phase.** SCLK is normally low and pulses high during bus transactions. The CPHA pin sets the phase (active edge) of SCLK. When CPHA = 0, data is latched in on SDI on the leading edge of the SCLK pulse and updated on SDO on the trailing edge. When CPHA = 1, data is latched in on SDI on the trailing edge of the SCLK pulse and updated on SDO on the following leading edge. SCLK does not have to toggle between accesses, i.e., when  $\overline{CS}$  is high. See [Figure 7-4](#).

**Device Selection.** Each SPI device has its own chip-select line. To select the DS3106, pull its  $\overline{CS}$  pin low.

**Control Word.** After  $\overline{CS}$  is pulled low, the bus master transmits the control word during the first sixteen SCLK cycles. In MSB-first mode the control word has the form:

$$R/\overline{W} \ A13 \ A12 \ A11 \ A10 \ A9 \ A8 \ A7 \quad A6 \ A5 \ A4 \ A3 \ A2 \ A1 \ A0 \ BURST$$

where A[13:0] is the register address,  $R/\overline{W}$  is the data direction bit (1=read, 0=write), and BURST is the burst bit (1=burst access, 0=single-byte access). In LSB-first mode the order of the fourteen address bits is reversed. In the discussion that follows, a control word with  $R/\overline{W} = 1$  is a read control word, while a control word with  $R/\overline{W} = 0$  is a write control word.

**Single-Byte Writes.** See [Figure 7-5](#). After  $\overline{CS}$  goes low, the bus master transmits a write control word with BURST=0 followed by the data byte to be written. The bus master then terminates the transaction by pulling  $\overline{CS}$  high.

**Single-Byte Reads.** See [Figure 7-5](#). After  $\overline{CS}$  goes low, the bus master transmits a read control word with BURST=0. The DS3106 then responds with the requested data byte. The bus master then terminates the transaction by pulling  $\overline{CS}$  high.

**Burst Writes.** See [Figure 7-5](#). After  $\overline{CS}$  goes low, the bus master transmits a write control word with BURST=1 followed by the first data byte to be written. The DS3106 receives the first data byte on SDI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the DS3106 continues to write the data received and increment its address counter. After the address counter reaches 3FFFh it rolls over to address 0000h and continues to increment.

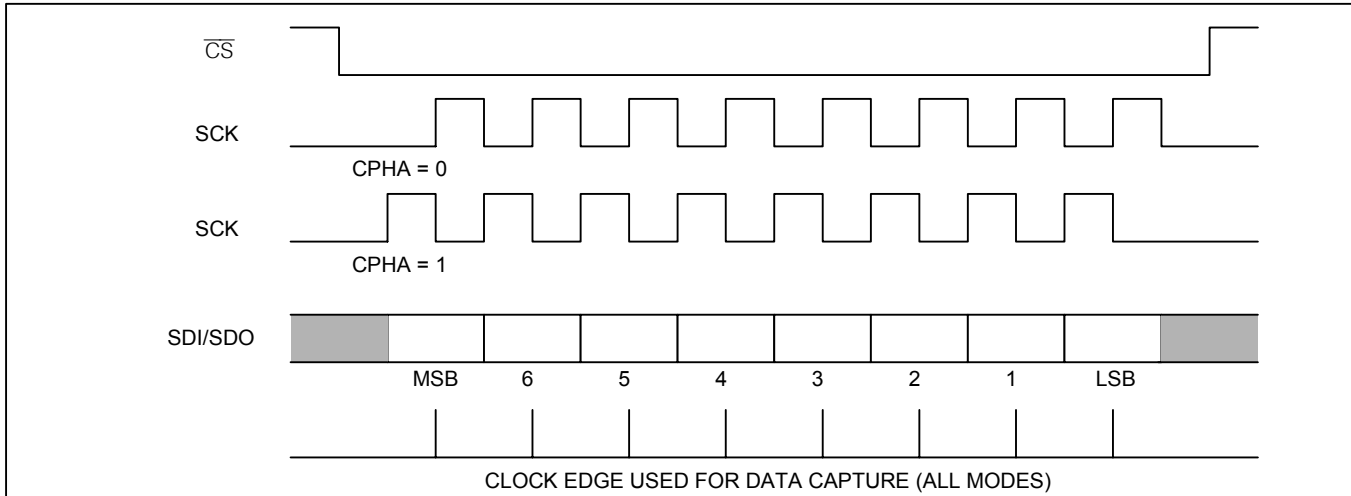
**Burst Reads.** See [Figure 7-5](#). After  $\overline{CS}$  goes low, the bus master transmits a read control word with BURST=1. The DS3106 then responds with the requested data byte on SDO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the DS3106 continues to provide the data on SDO, increment its address counter, and pre-fetch the following byte. After the address counter reaches 3FFFh it rolls over to address 0000h and continues to increment.

**Early Termination of Bus Transactions.** The bus master can terminate SPI bus transactions at any time by pulling  $\overline{CS}$  high. In response to early terminations, the DS3106 resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the LSB of a data byte, the data byte is not written.

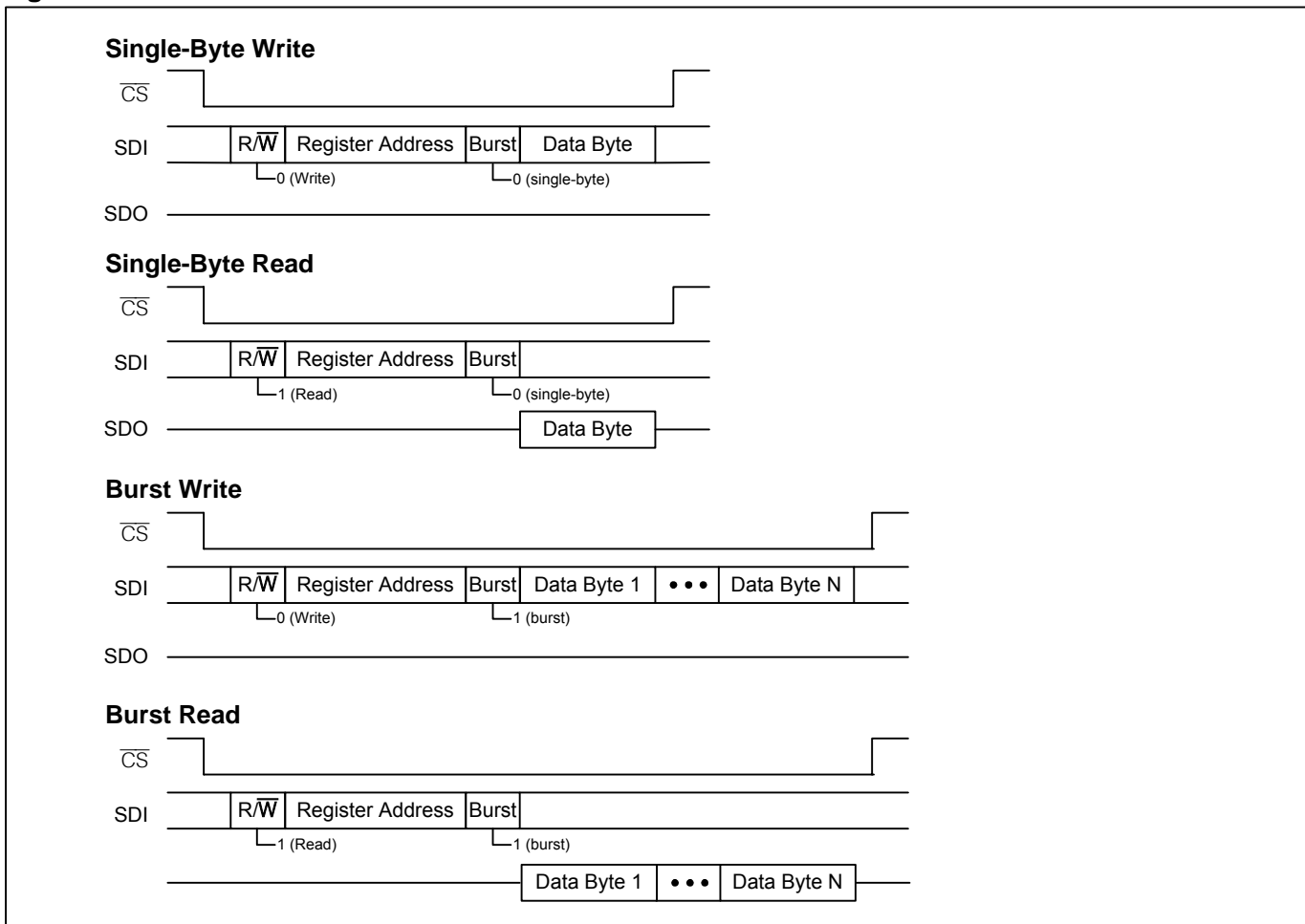
**Design Option: Wiring SDI and SDO Together.** Because communication between the bus master and the DS3106 is half-duplex, the SDI and SDO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the SDI/SDO line when the DS3106 is transmitting.

**AC Timing.** See [Table 10-9](#) and [Figure 10-3](#) for AC timing specifications for the SPI interface.

**Figure 7-4. SPI Clock Phase Options**



**Figure 7-5. SPI Bus Transactions**



## 7.10 Reset Logic

The device has three reset controls: the  $\overline{\text{RST}}$  pin, the RST bit in **MCR1**, and the JTAG reset pin  $\overline{\text{JTRST}}$ . The  $\overline{\text{RST}}$  pin asynchronously resets the entire device, except for the JTAG logic. When the  $\overline{\text{RST}}$  pin is low all internal registers are reset to their default values, including those fields which latch their default values from, or based on, the states of configuration input pins when the  $\overline{\text{RST}}$  goes high. **The  $\overline{\text{RST}}$  pin must be asserted once after power-up while the external oscillator is stabilizing.**

The **MCR1**:RST bit resets the entire device (except for the microprocessor interface, the JTAG logic, and the RST bit itself), but when RST is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead these fields are reset to the default values that were latched when the  $\overline{\text{RST}}$  pin was last active.

Dallas/Maxim recommends holding  $\overline{\text{RST}}$  low while the external oscillator starts up and stabilizes. An incorrect reset condition could result if  $\overline{\text{RST}}$  is released before the oscillator has started up completely.

**Important:** System software must wait at least 100 $\mu\text{s}$  after reset ( $\overline{\text{RST}}$  pin or RST bit) is deasserted before initializing the device as described in section 7.12.

## 7.11 Power-Supply Considerations

Due to the dual-power-supply nature of the DS3106, some I/Os have parasitic diodes between a 1.8V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the 1.8V supply and the 3.3V supply to force the 3.3V supply to be less than one parasitic diode drop below the 1.8V supply. The second method is to ramp up the 3.3V supply first and then ramp up the 1.8V supply.

## 7.12 Initialization

After power-up or reset, a series of writes must be done to the DS3106 to tune it for optimal performance. This series of writes is called the initialization script. Each die revision of the DS3106 has a different initialization script. The latest initialization scripts can be obtained by downloading from the DS3106 web page, [www.maxim-ic.com/DS3106](http://www.maxim-ic.com/DS3106), or by emailing [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com). Important: System software must wait at least 100 $\mu\text{s}$  after reset is deasserted before initializing the device

## 8 REGISTER DESCRIPTIONS

The DS3106 has an overall address range from 000h to 1FFh. [Table 8-1](#) in section [8.4](#) shows the register map. In each register, bit 7 is the MSB and bit 0 is the LSB. Register addresses not listed and bits marked “--” are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled “0” or “1” must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow [Table 8-1](#).

### 8.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request on the INTREQ pin if enabled to do so by corresponding interrupt enable bits. ISR#.LOCK# are special-case latched status bits because they cannot create an interrupt request on the INTREQ pin and a “write 0” is needed to clear them.

### 8.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked “--” are reserved and must be written with 0.

### 8.3 Multi-Register Fields

Multi-register fields—such as FREQ[18:0] in registers [FREQ1](#), [FREQ2](#) and [FREQ3](#)—must be handled carefully to ensure that the bytes of the field remain consistent. A write access to a multi-register field is accomplished by writing all the registers of the field in any order, with no other accesses to the device in between. If the write sequence is interrupted by another access, none of the bytes are written and the [MSR4:MRAA](#) latched status bit is set to indicate the write was aborted. A read access from a multi-register field is accomplished by reading the registers of the field in any order, with no other accesses to the device in between. When one register of a multi-register field is read, the other register(s) in the field are frozen until after they are all read. If the read sequence is interrupted by another access, the registers of the multi-byte field are unfrozen and the [MSR4:MRAA](#) bit is set to indicate the read was aborted. For best results, interrupt servicing should be disabled in the microprocessor before a multi-register access and then enabled again after the access is complete. The multi-register fields are:

<u>Field</u>	<u>Registers</u>	<u>Addresses</u>	<u>Type</u>
<u>FREQ[18:0]</u>	<a href="#">FREQ1</a> , <a href="#">FREQ2</a> , <a href="#">FREQ3</a>	07, 0C, 0D	read-only
<u>MCLKFREQ[15:0]</u>	<a href="#">MCLK1</a> , <a href="#">MCLK2</a>	3C, 3D	read/write
<u>HARDLIM[9:0]</u>	<a href="#">DLIMIT1</a> , <a href="#">DLIMIT2</a>	41, 42	read/write
<u>DIVN[15:0]</u>	<a href="#">DIVN1</a> , <a href="#">DIVN2</a>	46, 47	read/write
<u>PHASE[15:0]</u>	<a href="#">PHASE1</a> , <a href="#">PHASE2</a>	77, 78	read-only

## 8.4 Register Definitions

**Table 8-1. Register Map**

Register names are hyperlinks to register definitions. Underlined fields are read-only.

Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	<a href="#">ID1</a>	<u>ID[7:0]</u>							
01	<a href="#">ID2</a>	<u>ID[15:8]</u>							
02	<a href="#">REV</a>	<u>REV[7:0]</u>							
03	<a href="#">TEST1</a>	<a href="#">PALARM</a>	<a href="#">D180</a>	--	<a href="#">RA</a>	0	<a href="#">8KPOL</a>	0	0
05	<a href="#">MSR1</a>	--	--	--	--	<a href="#">IC4</a>	<a href="#">IC3</a>	--	--
06	<a href="#">MSR2</a>	<a href="#">STATE</a>	<a href="#">SRFAIL</a>	--	--	--	--	--	--
07	<a href="#">FREQ3</a>	--	--	--	--	--	<a href="#">FREQ[18:16]</a>		
09	<a href="#">OPSTATE</a>	--	--	<a href="#">T0SOFT</a>	--	--	<a href="#">T0STATE[2:0]</a>		
0A	<a href="#">PTAB1</a>	--	--	--	--	<a href="#">SELREF[3:0]</a>			
0C	<a href="#">FREQ1</a>	<a href="#">FREQ[7:0]</a>							
0D	<a href="#">FREQ2</a>	<a href="#">FREQ[15:8]</a>							
0E	<a href="#">VALSR1</a>	--	--	--	--	<a href="#">IC4</a>	<a href="#">IC3</a>	--	--
11	<a href="#">ISR2</a>	--	--	<a href="#">ACT4</a>	--	--	--	<a href="#">ACT3</a>	--
17	<a href="#">MSR4</a>	--	<a href="#">HORDY</a>	<a href="#">MRAA</a>	--	--	--	--	--
22	<a href="#">ICR3</a>	<a href="#">DIVN</a>	<a href="#">LOCK8K</a>	--	--	<a href="#">FREQ[3:0]</a>			
23	<a href="#">ICR4</a>	<a href="#">DIVN</a>	<a href="#">LOCK8K</a>	--	--	<a href="#">FREQ[3:0]</a>			
32	<a href="#">MCR1</a>	<a href="#">RST</a>	--	<a href="#">FREN</a>	<a href="#">LOCKPIN</a>	--	<a href="#">T0STATE[2:0]</a>		
34	<a href="#">MCR3</a>	--	--	<a href="#">XOEDGE</a>	<a href="#">FRUNHO</a>	--	<a href="#">SONSDH</a>	--	--
38	<a href="#">MCR6</a>	<a href="#">DIG2AF</a>	<a href="#">DIG2SS</a>	<a href="#">DIG1SS</a>	--	--	--	--	--
39	<a href="#">MCR7</a>	<a href="#">DIG2F[1:0]</a>		<a href="#">DIG1F[1:0]</a>		--	--	--	--
3A	<a href="#">MCR8</a>	--	--	--	--	--	<a href="#">OC6SF</a>		
3B	<a href="#">MCR9</a>	<a href="#">AUTOBW</a>	--	--	--	<a href="#">LIMINT</a>	--	--	--
3C	<a href="#">MCLK1</a>	<a href="#">MCLKFREQ[7:0]</a>							
3D	<a href="#">MCLK2</a>	<a href="#">MCLKFREQ[15:8]</a>							
40	<a href="#">HOCSR3</a>	<a href="#">AVG</a>	--	--	--	--	--	--	--
41	<a href="#">DLIMIT1</a>	<a href="#">HARDLIM[7:0]</a>							
42	<a href="#">DLIMIT2</a>	--	--	--	--	--	--	<a href="#">HARDLIM[9:8]</a>	
43	<a href="#">IER1</a>	--	--	--	--	<a href="#">IC4</a>	<a href="#">IC3</a>	--	--
44	<a href="#">IER2</a>	<a href="#">STATE</a>	<a href="#">SRFAIL</a>	--	--	--	--	--	--
46	<a href="#">DIVN1</a>	<a href="#">DIVN[7:0]</a>							
47	<a href="#">DIVN2</a>	<a href="#">DIVN[15:0]</a>							
48	<a href="#">MCR10</a>	--	<a href="#">SRFPIN</a>	--	--	--	--	--	--
4D	<a href="#">DLIMIT3</a>	<a href="#">FLLLOL</a>	<a href="#">SOFTLIM[6:0]</a>						
4E	<a href="#">IER4</a>	--	<a href="#">HORDY</a>	--	--	--	--	--	--
4F	<a href="#">OCR5</a>	--	--	<a href="#">AOF6</a>	--	--	<a href="#">AOF3</a>	--	--
50	<a href="#">LB0U</a>	<a href="#">LB0U[7:0]</a>							
51	<a href="#">LB0L</a>	<a href="#">LB0L[7:0]</a>							
52	<a href="#">LB0S</a>	<a href="#">LB0S[7:0]</a>							
53	<a href="#">LB0D</a>	--	--	--	--	--	--	<a href="#">LB0D[1:0]</a>	
61	<a href="#">OCR2</a>	--	--	--	--	<a href="#">OFREQ3[3:0]</a>			
62	<a href="#">OCR3</a>	<a href="#">OFREQ6[3:0]</a>				--	--	--	--
63	<a href="#">OCR4</a>	<a href="#">MFSEN</a>	<a href="#">FSEN</a>	--	--	--	--	--	--
64	<a href="#">T4CR1</a>	--	--	--	--	<a href="#">T4FREQ[3:0]</a>			
65	<a href="#">T0CR1</a>	--	<a href="#">T4APT0</a>	<a href="#">T0FT4[2:0]</a>			<a href="#">T0FREQ[2:0]</a>		
67	<a href="#">T0LBW</a>	--	--	--	<a href="#">RSV1</a>	<a href="#">RSV2</a>	<a href="#">T0LBW[2:0]</a>		
69	<a href="#">T0ABW</a>	--	--	--	<a href="#">RSV1</a>	<a href="#">RSV2</a>	<a href="#">T0ABW[2:0]</a>		

Addr	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6B	T0CR2	--	PD2G8K[2:0]			--	DAMP[2:0]		
6D	T0CR3	PD2EN	--	--	--	--	PD2G[2:0]		
6E	GPCR	GPIO4D	GPIO3D	GPIO2D	GPIO1D	GPIO4O	GPIO3O	GPIO2O	GPIO1O
6F	GPSR	--	--	--	--	GPIO4	GPIO3	GPIO2	GPIO1
73	PHLIM1	FLEN	NALOL	1	--	--	FINELIM[2:0]		
74	PHLIM2	CLEN	MCPDEN	USEMCPD	--	COARSELIM[3:0]			
76	PHMON	NW	--	--	--	--			
77	PHASE1	PHASE[7:0]							
78	PHASE2	PHASE[15:8]							
7A	FSCR1	--	--	--	--	8KINV	8KPUL	2KINV	2KPUL
7D	INTCR	--	--	--	--	LOS	GPO	OD	POL
7E	PROT	PROT[7:0]							

### Register Map Color Coding

	Device Identification and Protection
	Local Oscillator and Master Clock Configuration
	Input Clock Configuration
	Input Clock Monitoring
	Input Clock Selection
	DPLL Configuration
	DPLL State
	Output Clock Configuration
	Frame/Multiframe Sync Configuration

**Register Name:** ID1  
**Register Description:** Device Identification Register, LSB  
**Register Address:** 00h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[7:0]							
Default	0	0	1	0	0	0	0	1

**Bits 7 to 0: Device ID (ID[7:0]).** ID[15:0] = 0C22h = 3106 decimal.

**Register Name:** ID2  
**Register Description:** Device Identification Register, MSB  
**Register Address:** 01h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[15:8]							
Default	0	0	0	0	1	1	0	0

**Bits 7 to 0: Device ID (ID[15:8]).** See the [ID1](#) register description.

**Register Name:** REV  
**Register Description:** Device Revision Register  
**Register Address:** 02h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REV[7:0]							
Default	0	0	0	0	0	0	0	0

**Bits 7 to 0: Device Revision (REV[7:0]).** Contact the factory to interpret this value and determine the latest revision.

**Register Name:** TEST1  
**Register Description:** Test Register 1 (Not Normally Used)  
**Register Address:** 03h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	<u>PALARM</u>	D180	—	RA	0	8KPOL	0	0
<b>Default</b>	0	0	0	1	0	1	0	0

**Bit 7: Phase Alarm (PALARM).** This real-time status bit indicates the state of the T0 DPLL phase lock detector. See section 7.7.5. (NOTE: This is not the same as T0STATE=Locked.)

0 = T0 DPLL phase-lock parameters are met (FLEN, CLEN, NALOL, FLLOL)

1 = T0 DPLL loss of phase lock

**Bit 6: Disable 180 (D180).** When locking to a new reference, the T0 DPLL first tries nearest-edge locking ( $\pm 180^\circ$ ) for the first two seconds. If unsuccessful it then tries full phase/frequency locking ( $\pm 360^\circ$ ). Disabling the nearest-edge locking can reduce lock time by up to two seconds but may cause an unnecessary phase shift (up to  $360^\circ$ ) when the new reference is close in frequency/phase to the old reference. See section 7.7.4.

0 = normal operation: try nearest-edge locking then phase/frequency locking

1 = phase/frequency locking only

**Bit 4: Resync Analog Dividers (RA).** When this bit is set the analog output dividers are always synchronized to ensure that low-frequency outputs are in sync with the higher-frequency clock from the DPLL.

0 = synchronized for the first two seconds after power-up

1 = always synchronized

**Bit 3:** Leave set to zero (test control).

**Bit 2: 8kHz Edge Polarity (8KPOL).** Specifies the input clock edge to lock to on the selected reference when it is configured for LOCK8K mode. See section 7.4.2.

0 = Falling edge

1 = Rising edge

**Bit 1:** Leave set to zero (test control).

**Bit 0:** Leave set to zero (test control).

**Register Name:** MSR1  
**Register Description:** Master Status Register 1  
**Register Address:** 05h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	IC4	IC3	--	--
<b>Default</b>	1	0	1	1	1	1	1	1

**Bits 3 and 2: Input Clock Status Change (IC4 and IC3).** Each of these latched status bits is set to 1 when the corresponding [VALSR1](#) status bit changes state (set or cleared). Each bit is cleared when written with a 1 and not set again until the [VALSR1](#) bit changes state again. When one of these latched status bits is set it can cause an interrupt request on the INTREQ pin if the corresponding interrupt enable bit is set in the [IER1](#) register. See section [7.5](#) for input clock validation/invalidation criteria.

**Register Name:** MSR2  
**Register Description:** Master Status Register 2  
**Register Address:** 06h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	STATE	SRFAIL	--	--	--	--	--	--
<b>Default</b>	0	0	0	0	0	0	0	1

**Bit 7: T0 DPLL State Change (STATE).** This latched status bit is set to 1 when the operating state of the T0 DPLL changes. STATE is cleared when written with a 1 and not set again until the operating state changes again. When STATE is set it can cause an interrupt request on the INTREQ pin if the STATE interrupt enable bit is set in the [IER2](#) register. The current operating state can be read from the T0STATE field of the [OPSTATE](#) register. See section [7.7.1](#).

**Bit 6: Selected Reference Failed (SRFAIL).** This latched status bit is set to 1 when the selected reference to the T0 DPLL fails, (i.e. no clock edges in two UI). SRFAIL is cleared when written with a 1. When SRFAIL is set it can cause an interrupt request on the INTREQ pin if the SRFAIL interrupt enable bit is set in the [IER2](#) register. SRFAIL is not set in Free-run mode or Holdover mode. See section [7.5.3](#).

**Register Name:** [FREQ3](#)  
**Register Description:** Frequency Register 3  
**Register Address:** 07h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	--	FREQ[18:16]		
<b>Default</b>	0	0	0	0	0	0	0	0

**Bits 2 to 0: Current DPLL Frequency (FREQ[18:16]).** See the [FREQ1](#) register description.

**Register Name:** OPSTATE  
**Register Description:** Operating State Register  
**Register Address:** 09h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	T0SOFT	--	--	T0STATE[2:0]		
<b>Default</b>	1	0	0	0	0	0	0	1

**Bit 5: T0 DPLL Frequency Soft Alarm (T0SOFT).** This real-time status bit indicates whether or not the T0 DPLL is tracking its reference within the soft alarm limits specified in the SOFT[6:0] field of the DLIMIT3 register. See section 7.7.5.

0 = No alarm; frequency is within the soft alarm limits

1 = Soft alarm; frequency is outside the soft alarm limits

**Bits 2 to 0: T0 DPLL Operating State (T0STATE[2:0]).** This real-time status field indicates the current state of the T0 DPLL state machine. Values not listed below correspond to invalid (unused) states. See section 7.7.1.

001 = Free-run

010 = Holdover

100 = Locked

101 = Pre-locked 2

110 = Pre-locked

111 = Loss-of-lock

**Register Name:** PTAB1  
**Register Description:** Priority Table Register 1  
**Register Address:** 0Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	SELREF[3:0]			
<b>Default</b>	0	0	0	0	see below			

**Bits 3 to 0: Selected Reference (SELREF[3:0]).** This real-time status field indicates the current selected reference for the DPLL. The default value for this field is 0011b if the SRCSW pin is 1 during reset and 0100b if SRCSW is 0 during reset.

0000 = No valid input reference available

0001 to 0010 = {unused value}

0011 = Input IC3

0100 = Input IC4

0101 to 1111 = {unused value}

**Register Name:**                   FREQ1  
**Register Description:**        Frequency Register 1  
**Register Address:**            0Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	FREQ[7:0]							
<b>Default</b>	0	0	0	0	0	0	0	0

The FREQ1, FREQ2 and FREQ3 registers must be read consecutively. See section 8.3.

**Bits 7 to 0: Current DPLL Frequency (FREQ[7:0]).** The full 19-bit FREQ[18:0] field spans this register, FREQ2 and FREQ3. FREQ is a 2's-complement signed integer that expresses the current frequency as an offset with respect to the master clock frequency (see section 7.3). Because the value in this register field is derived from the DPLL integral path, it can be considered an average frequency with a rate of change inversely proportional to the DPLL bandwidth. If LIMINT=1 in the MCR9 register, the value of FREQ freezes when the DPLL reaches its minimum or maximum frequency. The frequency offset in ppm is equal to  $FREQ[18:0] * 0.0003068$ . See section 7.7.1.6.

Application Note: Frequency measurements are relative, i.e. they measure the frequency of the selected reference with respect to the local oscillator. As such, when a frequency difference exists, it is difficult to distinguish whether the selected reference is off frequency or the local oscillator is off frequency. In systems with timing card redundancy, the use of two timing cards, master and slave, can address this difficulty. Both master and slave have separate local oscillators, and each measures the selected reference. These two measurements provide the necessary information to distinguish which reference is off frequency, if we make the simple assumption that at most one reference has a significant frequency deviation at any given time (i.e. a single point of failure). If both master and slave indicate a significant frequency offset, then the selected reference must be off frequency. If the master indicates a frequency offset but the slave does not, then the master's local oscillator must be off frequency. Likewise, if the slave indicates a frequency offset but the master does not, then slave's local oscillator must be off frequency.

**Register Name:**                   FREQ2  
**Register Description:**        Frequency Register 2  
**Register Address:**            0Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	FREQ[15:8]							
<b>Default</b>	0	0	0	0	0	0	0	0

**Bits 7 to 0: Current DPLL Frequency (FREQ[15:8]).** See the FREQ1 register description.

**Register Name:** VALSR1  
**Register Description:** Input Clock Valid Status Register 1  
**Register Address:** 0Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	<u>IC4</u>	<u>IC3</u>	--	--
<b>Default</b>	0	0	0	0	0	0	0	0

**Bits 3 and 2: Input Clock Valid Status (IC4 and IC3).** Each of these real-time status bits is set to 1 when the corresponding input clock is valid. An input is valid if the activity alarm is not set (ACT=0 in the corresponding [ISR](#) register). See also the [MSR1](#) register and section 7.5.

0 = Invalid  
 1 = Valid

**Register Name:** ISR2  
**Register Description:** Input Status Register 2  
**Register Address:** 11h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	<u>ACT4</u>	--	--	--	<u>ACT3</u>	--
<b>Default</b>	0	0	1	0	0	0	1	0

**Bit 5: Activity Alarm for Input Clock 4 (ACT4).** This real-time status bit is set to 1 when the leaky bucket accumulator for IC4 reaches the alarm threshold specified in the [LBxU](#) register (where 'x' in 'LBxU' is specified in the BUCKET field of [ICR4](#)). An activity alarm clears the IC4 status bit in the [VALSR1](#) register, invalidating the IC4 clock. See section 7.5.2.

**Bit 1: Activity Alarm for Input Clock 3 (ACT3).** This bit has the same behavior as the ACT4 bit but for the IC3 input clock.

**Register Name:** MSR4  
**Register Description:** Master Status Register 4  
**Register Address:** 17h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	HORDY	MRAA	--	--	--	--	--
<b>Default</b>	0	0	0	0	0	0	0	0

**Bit 6: Holdover Frequency Ready (HORDY).** This latched status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the 1-second holdover averaging period. HORDY is cleared when written with a 1. When HORDY is set it can cause an interrupt request on the INTREQ pin if the HORDY interrupt enable bit is set in the [IER4](#) register. See section 7.7.1.6.

**Bit 5: Multi-Register Access Aborted (MRAA).** This latched status bit is set to 1 when a multi-byte access (read or write) is interrupted by another access to the device. MRAA is cleared when written with a 1. MRAA cannot cause an interrupt to occur. See section 8.3.

**Register Name:** ICR3, ICR4  
**Register Description:** Input Configuration Register 3, 4  
**Register Address:** 22h, 23h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	DIVN	LOCK8K	--	--		FREQ[3:0]		
<b>Default</b>	0	0	0	0		see below		

These registers are identical in function. ICRx is the control register for input clock ICx.

**Bit 7: DIVN Mode (DIVN).** When DIVN is set to 1 and LOCK8K=0, the input clock is divided down by a programmable pre-divider. The resulting output clock is then passed to the DPLL. All input clocks for which DIVN=1 are divided by the factor specified in [DIVN1](#) and [DIVN2](#). When DIVN=1 and LOCK8K=0 in an ICR register, the FREQ field of that register must be set to the input frequency divided by the divide factor. When DIVN=1 and LOCK8K=1 in an ICR register, the FREQ field of that register is decoded as the alternate frequencies. See sections [7.4.2.2](#) and [7.4.2.4](#).

0 = Disabled  
 1 = Enabled

**Bit 6: LOCK8K Mode (LOCK8K).** When LOCK8K is set to 1 and DIVN=0, the input clock is divided down by a preset pre-divider. The resulting output clock, which is always 8 kHz, is then passed to the DPLL. LOCK8K is ignored when DIVN=0 and FREQ[3:0] = 1001 (2 kHz) or 1010 (4 kHz). When DIVN=1 and LOCK8K=1 in an ICR register, the FREQ field of that register is decoded as the alternate frequencies. See sections [7.4.2.2](#) and [7.4.2.3](#)

0 = Disabled  
 1 = Enabled

**Bits 3 to 0: Input Clock Frequency (FREQ[3:0]).** When DIVN=0 and LOCK8K=0 (standard direct-lock mode), this field specifies the input clock's nominal frequency for direct-lock operation. When DIVN=0 and LOCK8K=1 (LOCK8K mode) this field specifies the input clock's nominal frequency for LOCK8K operation. When DIVN=1 and LOCK8K=0 (DIVN mode), this field specifies the frequency after the DIVN divider (i.e. input frequency divided by [DIVN](#) + 1). When DIVN=1 and LOCK8K=1 (alternate direct-lock frequencies), this field specifies the input clock's nominal frequency for direct-lock operation.

DIVN=0 or LOCK8K=0: (Standard direct-lock mode, LOCK8K mode, or DIVN mode)

0000 = 8 kHz  
 0001 = 1544 or 2048 kHz (as determined by SONS DH bit in the [MCR3](#) register)  
 0010 = 6.48 MHz  
 0011 = 19.44 MHz  
 0100 = 25.92 MHz  
 0101 = 38.88 MHz  
 0110 = 51.84 MHz  
 0111 = 77.76 MHz  
 1000 = 155.52 MHz (only valid for LVDS inputs)  
 1001 = 2 kHz  
 1010 = 4 kHz  
 1011 = 6312 kHz  
 1100 = 5 MHz  
 1101 = 31.25 MHz (not a multiple of 8 kHz and therefore not valid for LOCK8K mode)  
 1110 to 1111 = undefined

DIVN=1 and LOCK8K=1: (Alternate direct-lock frequency decode)

0000 = 10 MHz (internally divided down to 5 MHz)  
 0001 = 25 MHz (internally divided down to 5 MHz)  
 0010 = 62.5 MHz (internally down to 31.25 MHz)  
 0011 = 125 MHz (internally down to 31.25 MHz)  
 0100 to 1111 = undefined

**FREQ[3:0] Default Values:**

See [Table 7-2](#).

**Register Name:** MCR1  
**Register Description:** Master Configuration Register 1  
**Register Address:** 32h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	RST	--	FREN	LOCKPIN	--	T0STATE[2:0]		
<b>Default</b>	0	0	1	0	0	0	0	0

**Bit 7: Device Reset (RST).** When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the RST pin was last active. See section 7.10.

0 = Normal operation

1 = Reset

**Bit 5: Frequency Range Detect Enable (FREN).** When this bit is high the frequency of each input clock is measured and used to quickly declare the input inactive.

0 = Frequency Range Detect disabled

1 = Frequency Range Detect enabled

**Bit 4: T0 DPLL LOCK Pin Enable (LOCKPIN).** When this bit is high the LOCK pin indicates when the T0 DPLL state machine is in the LOCK state (OPSTATE.T0STATE=100).

0 = LOCK pin is not driven

1 = LOCK pin is driven high when the T0 DPLL is in the Lock state

**Bits 2 to 0: T0 DPLL State Control (T0STATE[2:0]).** This field allows the T0 DPLL state machine to be forced to a specified state. The state machine will remain in the forced state, and therefore cannot react to alarms and other events, as long as T0STATE is not equal to 000. See section 7.7.1.

000 = Automatic (normal state machine operation)

001 = Free-run

010 = Holdover

011 = {unused value}

100 = Locked

101 = Pre-locked 2

110 = Pre-locked

111 = Loss-of-lock

**Register Name:** MCR3  
**Register Description:** Master Configuration Register 3  
**Register Address:** 34h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	XOEDGE	FRUNHO	--	SONSDH	--	--
<b>Default</b>	1	1	0	0	0	see below	1	0

**Bit 5: Local Oscillator Edge (XOEDGE).** This bit specifies the significant clock edge of the local oscillator clock signal on the REFCLK input pin. The faster edge should be selected for best jitter performance. See section 7.3.

- 0 = Rising edge
- 1 = Falling edge

**Bit 4: Free-Run Holdover (FRUNHO).** When this bit is set to 1 the T0 DPLL holdover frequency is set to 0 ppm so the output frequency accuracy is set by the external oscillator accuracy. This effects both mini-holdover and the holdover state.

- 0 = Digital holdover
- 1 = Free-Run holdover, 0 ppm

**Bit 2: SONET or SDH Frequencies (SONSDH).** This bit specifies the clock rate for input clocks with  $FREQ=0001$  in the ICR registers (20h to 28h). During reset the default value of this bit is latched from the SONSDH pin. See section 7.4.2.

- 0 = 2048 kHz
- 1 = 1544 kHz.

**Register Name:** MCR6  
**Register Description:** Master Configuration Register 6  
**Register Address:** 38h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	DIG2AF	DIG2SS	DIG1SS	--	--	--	--	--
<b>Default</b>	0	see below	see below	1	1	1	1	1

**Bit 7: Digital Alternate Frequency (DIG2AF).** Selects alternative frequencies.

- 0 = Digital2 Nx $E1$  or Nx $DS1$  frequency specified by DIG2SS and MCR7:DIG2F.
- 1 = Digital2 6.312 MHz, 10 MHz or Nx19.44 MHz frequency specified by DIG2SS and MCR7:DIG2F.

**Bit 6: Digital2 SONET or SDH Frequencies (DIG2SS).** This bit specifies whether the clock rates generated by the Digital2 clock synthesizer are multiples of 1.544 MHz (SONET-compatible) or multiples of 2.048 MHz (SDH-compatible) or alternate frequencies. The specific multiple is set in the DIG2F field of the MCR7 register. When  $\overline{RST}=0$  the default value of this bit is latched from the SONSDH pin.

- DIG2AF=0:
  - 0 = Multiples of 2048 kHz
  - 1 = Multiples of 1544 kHz
- DIG2AF=1:
  - 6.312 MHz, 10 MHz or Nx19.44 MHz

**Bit 5: Digital1 SONET or SDH Frequencies (DIG1SS).** This bit specifies whether the clock rates generated by the Digital1 clock synthesizer are multiples of 1544 kHz (SONET-compatible) or multiples of 2048 kHz (SDH-compatible). The specific multiple is set in the DIG1F field of the MCR7 register. When  $\overline{RST}=0$  the default value of this bit is latched from the SONSDH pin.

- 0 = Multiples of 2048 kHz
- 1 = Multiples of 1544 kHz

**Register Name:** MCR7  
**Register Description:** Master Configuration Register 7  
**Register Address:** 39h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	DIG2F[1:0]		DIG1F[1:0]		--	--	--	--
<b>Default</b>	0	0	0	0	1	0	0	0

**Bits 7 to 6: Digital2 Frequency (DIG2F[1:0]).** This field, [MCR6:DIG2SS](#) and [MCR6:DIG2AF](#) configure the frequency of the Digital2 clock synthesizer.

DIG2AF=0		DIG2AF=1	
DIG2SS = 1	DIG2SS = 0	DIG2SS = 1	DIG2SS = 0
00 = 1544 kHz	00 = 2048 kHz	00 = 19.44 MHz	00 = 6.312 MHz
01 = 3088 kHz	01 = 4096 kHz	01 = 38.88 MHz	01 = undefined
10 = 6176 kHz	10 = 8192 kHz	10 = undefined	10 = 10 MHz
11 = 12352 kHz	11 = 16384 kHz	11 = undefined	11 = undefined

**Bits 5 to 4: Digital1 Frequency (DIG1F[1:0]).** This field and [MCR6:DIG1SS](#) configure the frequency of the Digital1 clock synthesizer.

DIG1SS = 1	DIG1SS = 0
00 = 1544 kHz	00 = 2048 kHz
01 = 3088 kHz	01 = 4096 kHz
10 = 6176 kHz	10 = 8192 kHz
11 = 12352 kHz	11 = 16384 kHz

**Register Name:** MCR8  
**Register Description:** Master Configuration Register 8  
**Register Address:** 3Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	--	--	OC6SF[1:0]	
<b>Default</b>	0	0	0	0	0	0	1	0

**Bits 1 to 0: Output Clock 6 Signal Format (OC6SF[1:0]).** See section [7.8.1](#).

00 = Output disabled  
01 = 3V LVPECL level compatible  
10 = 3V LVDS compatible (default)  
11 = 3V LVDS compatible

**Register Name:** MCR9  
**Register Description:** Master Configuration Register 9  
**Register Address:** 3Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	AUTOBW	--	--	--	LIMINT	--	--	--
<b>Default</b>	1	1	1	1	1	0	1	1

**Bit 7: Automatic Bandwidth Selection (AUTOBW).** See section 7.7.2.

0 = Always selects locked bandwidth from the TOLBW register

1 = Automatically selects either locked bandwidth (TOLBW register) or acquisition bandwidth (TOABW register) as appropriate

**Bit 3: Limit Integral Path (LIMINT).** When this bit is set to 1, the T0 DPLL's integral path is limited (i.e. frozen) when the DPLL reaches minimum or maximum frequency, as set by the HARDLIM field in DLIMIT1 and DLIMIT2. When the integral path is frozen, the current DPLL frequency in registers FREQ1, FREQ2 and FREQ3 is also frozen. Setting LIMINT=1 minimizes overshoot when the DPLL is pulling in. See section 7.7.2.

0 = Don't freeze integral path at min/max frequency

1 = Freeze integral path at min/max frequency

**Register Name:** MCLK1  
**Register Description:** Master Clock Frequency Adjustment Register 1  
**Register Address:** 3Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	MCLKFREQ[7:0]							
<b>Default</b>	1	0	0	1	1	0	0	1

The MCLK1 and MCLK2 registers must be read consecutively and written consecutively. See section 8.3.

**Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[7:0]).** The full 16-bit MCLKFREQ[15:0] field spans this register and MCLK2. MCLKFREQ is an unsigned integer that adjusts the frequency of the internal 204.8 MHz master clock with respect to the frequency of the local oscillator clock on the REFCLK pin by up to +514ppm and -771 ppm. The master clock adjustment has the effect of speeding up the master clock with a positive adjustment and slowing it down with a negative adjustment. For example, if the oscillator connected to REFCLK has an offset of +1 ppm then the adjustment should be -1 ppm to correct the offset.

The formulas below translate adjustments to register values and vice versa. The default register value of 39,321 corresponds to 0 ppm. See section 7.3.

$$\text{MCLKFREQ}[15:0] = \text{adjustment\_in\_ppm} / 0.0196229 + 39,321$$

$$\text{adjustment\_in\_ppm} = (\text{MCLKFREQ}[15:0] - 39,321) * 0.0196229$$

**Register Name:** MCLK2  
**Register Description:** Master Clock Frequency Adjustment Register 2  
**Register Address:** 3Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	MLCKFREQ[15:8]							
<b>Default</b>	1	0	0	1	1	0	0	1

**Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[15:8]).** See the [MCLK1](#) register description.

**Register Name:** HOCCR3  
**Register Description:** Holdover Configuration Register 3  
**Register Address:** 40h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	AVG	--	--	--	--	--	--	--
<b>Default</b>	1	0	0	0	1	0	0	0

See section [8.3](#) for important information about writing and reading this register.

**Bit 7: Averaging (AVG).** When this bit is set to 1 the T0 DPLL uses the averaged frequency value during holdover mode. When FRUNHO=1 in the [MCR3](#) register, this bit is ignored. See section [7.7.1.6](#).

0 = Not averaged frequency; holdover frequency is either freerun (FRUNHO=1) or instantaneously frozen  
 1 = Averaged frequency over the last 1 second while locked to the input

**Register Name:** DLIMIT1  
**Register Description:** DPLL Frequency Limit Register 1  
**Register Address:** 41h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	HARDLIM[7:0]							
<b>Default</b>	1	1	1	1	1	1	1	1

The DLIMIT1 and DLIMIT2 registers must be read consecutively and written consecutively. See section [8.3](#).

**Bits 7 to 0: DPLL Hard Frequency Limit (HARDLIM[7:0]).** The full 10-bit HARDLIM[9:0] field spans this register and [DLIMIT2](#). HARDLIM is an unsigned integer that specifies the hard frequency limit or pull-in/hold-in range of the T0 DPLL. When frequency limit detection is enabled by setting FLLOL=1 in the [DLIMIT3](#) register, if the DPLL frequency exceeds the hard limit then the DPLL declares loss-of-lock. The hard frequency limit in ppm is  $\pm \text{HARDLIM}[9:0] * 0.0782$ . The default value is normally  $\pm 79.794$  ppm (3FFh). See section [7.7.5](#).

**Register Name:** DLIMIT2  
**Register Description:** DPLL Frequency Limit Register 1  
**Register Address:** 42h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	--	--	HARDLIM[9:8]	
<b>Default</b>	0	0	0	0	0	0	1	1

**Bits 1 to 0: DPLL Hard Frequency Limit (HARDLIM[9:8]).** See the [DLIMIT1](#) register description.

**Register Name:** IER1  
**Register Description:** Interrupt Enable Register 1  
**Register Address:** 43h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	IC4	IC3	--	--
<b>Default</b>	0	0	0	0	0	0	0	0

**Bits 3 to 2 Interrupt Enable for Input Clock Status Change (IC4 to IC3).** Each of these bits is an interrupt enable control for the corresponding bit in the [MSR1](#) register.

0 = Mask the interrupt

1 = Enable the interrupt

**Register Name:** IER2  
**Register Description:** Interrupt Enable Register 2  
**Register Address:** 44h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	STATE	SRFAIL	--	--	--	--	--	--
<b>Default</b>	0	0	0	0	0	0	0	0

**Bit 7: Interrupt Enable for T0 DPLL State Change (STATE).** This bit is an interrupt enable for the STATE bit in the [MSR2](#) register.

0 = Mask the interrupt

1 = Enable the interrupt

**Bit 6: Interrupt Enable for Selected Reference Failed (SRFAIL).** This bit is an interrupt enable for the SRFAIL bit in the [MSR2](#) register.

0 = Mask the interrupt

1 = Enable the interrupt

**Register Name:** DIVN1  
**Register Description:** DIVN Register 1  
**Register Address:** 46h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIVN[7:0]							
Default	1	1	1	1	1	1	1	1

The DIVN1 and DIVN2 registers must be read consecutively and written consecutively. See section 8.3.

**Bits 7 to 0: DIVN Factor (DIVN[7:0]).** The full 16-bit DIVN[15:0] field spans this register and [DIVN2](#). This field contains the integer value used to divide the frequency of input clocks that are configured for DIVN mode. The frequency is divided by DIVN[15:0] + 1. See section 7.4.2.4.

**Register Name:** DIVN2  
**Register Description:** DIVN Register 2  
**Register Address:** 47h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIVN[15:8]							
Default	0	0	1	1	1	1	1	1

**Bits 7 to 0: DIVN Factor (DIVN[15:8]).** See the [DIVN1](#) register description.

**Register Name:** MCR10  
**Register Description:** Master Configuration Register 10  
**Register Address:** 48h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	--	SRFPIN	--	--	--	--	--	--
Default	1	0	0	1	0	0	0	0

**Bit 6: SRFAIL Pin Enable (SRFPIN).** When this bit is set to 1, the SRFAIL pin is enabled. When enabled the SRFAIL pin follows the state of the SRFAIL status bit in the [MSR2](#) register. This gives the system a very fast indication of the failure of the current reference. See section 7.5.3.

0 = SRFAIL pin disabled (not driven)

1 = SRFAIL pin enabled

**Register Name:** DLIMIT3  
**Register Description:** DPLL Frequency Limit Register 3  
**Register Address:** 4Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	FLLOL	SOFTLIM[6:0]						
<b>Default</b>	1	0	0	0	1	1	1	0

**Bit 7: Frequency Limit Loss of Lock (FLLOL).** When this bit is set to 1, the T0 DPLL internally declares loss-of-lock when the hard frequency limit in the [DLIMIT1](#) and [DLIMIT2](#) registers is reached. See section [7.7.5](#).

0 = DPLL declares loss-of-lock normally

1 = DPLL also declares loss-of-lock when the hard frequency limit is reached

**Bits 6 to 0: DPLL Soft Frequency Limit (SOFTLIM6:0).** This field is an unsigned integer that specifies the soft frequency limit for the T0 DPLL. The soft limit is only used for monitoring; exceeding this limit does not cause loss-of-lock. The limit in ppm is  $\pm\text{SOFTLIM}[6:0] * 0.628$ . The default value is  $\pm 8.79$  ppm. When the T0 DPLL frequency reaches the soft limit the T0SOFT status bit is set in the [OPSTATE](#) register. See section [7.7.5](#).

**Register Name:** IER4  
**Register Description:** Interrupt Enable Register 4  
**Register Address:** 4Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	HORDY	--	--	--	--	--	--
<b>Default</b>	0	0	0	0	0	0	0	0

**Bit 6: Interrupt Enable for Holdover Frequency Ready (HORDY).** This bit is an interrupt enable for the HORDY bit in the [MSR4](#) register.

0 = Mask the interrupt

1 = Enable the interrupt

**Register Name:** OCR5  
**Register Description:** Output Configuration Register 1  
**Register Address:** 4Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	AOF6	--	--	AOF3	--	--
<b>Default</b>	0	0	0	0	0	0	0	0

**Bit 5: Alternate Output Frequency Mode Select 6 (AOF6).** This bit controls the decoding of the [OCR3.OFREQ6](#) field for the OC6 pin.

0 = Standard decodes

1 = Alternate decodes

**Bit 2: Alternate Output Frequency Mode Select 3 (AOF3).** This bit controls the decoding of the [OCR2.OFREQ3](#) field for the OC3 pin.

0 = Standard decodes

1 = Alternate decodes

**Register Name:** LB0U  
**Register Description:** Leaky Bucket 0 Upper Threshold Register  
**Register Address:** 50h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	LB0U[7:0]							
<b>Default</b>	0	0	0	0	0	1	1	0

**Bits 7 to 0: Leaky Bucket 0 Upper Threshold (LB0U[7:0]).** When the leaky bucket accumulator is equal to the value stored in this field, the activity monitor declares an activity alarm by setting the input clock's ACT bit in the appropriate **ISR** register. Registers **LB0U**, **LB0L**, **LB0S** and **LB0D** together specify leaky bucket configuration 0. See section [7.5.2](#).

**Register Name:** LB0L  
**Register Description:** Leaky Bucket 0 Lower Threshold Register  
**Register Address:** 51h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	LB0L[7:0]							
<b>Default</b>	0	0	0	0	0	1	0	0

**Bits 7 to 0: Leaky Bucket 0 Lower Threshold (LB0L[7:0]).** When the leaky bucket accumulator is equal to the value stored in this field, the activity monitoring logic clears the activity alarm (if previously declared) by clearing the input clock's ACT bit in the appropriate **ISR** register. Registers **LB0U**, **LB0L**, **LB0S** and **LB0D** together specify leaky bucket configuration 0. See section [7.5.2](#).

**Register Name:** LB0S  
**Register Description:** Leaky Bucket 0 Size Register  
**Register Address:** 52h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	LB0S[7:0]							
<b>Default</b>	0	0	0	0	1	0	0	0

**Bits 7 to 0: Leaky Bucket 0 Size (LB0S[7:0]).** This field specifies the maximum value of the leaky bucket. The accumulator cannot increment past this value. Registers **LB0U**, **LB0L**, **LB0S** and **LB0D** together specify leaky bucket configuration 0. See section [7.5.2](#).

**Register Name:** LB0D  
**Register Description:** Leaky Bucket 0 Decay Rate Register  
**Register Address:** 53h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	--	--	LB0D[1:0]	
<b>Default</b>	0	0	0	0	0	0	0	1

**Bits 1 to 0: Leaky Bucket 0 Decay Rate (LB0D[1:0]).** This field specifies the decay or "leak" rate of the leaky bucket accumulator. For each period of 1, 2, 4 or 8 128-ms intervals in which no irregularities are detected on the input clock, the accumulator decrements by 1. Registers **LB0U**, **LB0L**, **LB0S** and **LB0D** together specify leaky bucket configuration 0. See section [7.5.2](#).

- 00 = decrement every 128 ms (8 units/second)
- 01 = decrement every 256 ms (4 units/second)
- 10 = decrement every 512 ms (2 units/second)
- 11 = decrement every 1024 ms (1 unit/second)

**Register Name:** OCR2  
**Register Description:** Output Configuration Register 2  
**Register Address:** 61h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	0	0	0	0	OFREQ3[3:0]			
<b>Default</b>	0	0	0	0	see below			

**Bits 3 to 0: Output Frequency of OC3 (OFREQ3[3:0]).** This field specifies the frequency of output clock OC3. The frequencies of the T0 APLL and T4 APLL are configured in the [TOCR1](#) and [T4CR1](#) registers. The Digital1 and Digital2 frequencies are configured in the [MCR7](#) register. See section [7.8.2.3](#). The default frequency is set by the O3F[2:0] bits, see [Table 7-17](#). The decode of this field is controlled by the value of the [OCR5.AOF3](#) bit.

AOF3=0: (standard decodes)

- 0000 = Output disabled (i.e. low)
- 0001 = 2 kHz
- 0010 = 8 kHz
- 0011 = Digital2 (see [Table 7-7](#))
- 0100 = Digital1 (see [Table 7-6](#))
- 0101 = T0 APLL frequency divided by 48
- 0110 = T0 APLL frequency divided by 16
- 0111 = T0 APLL frequency divided by 12
- 1000 = T0 APLL frequency divided by 8
- 1001 = T0 APLL frequency divided by 6
- 1010 = T0 APLL frequency divided by 4
- 1011 = T4 APLL frequency divided by 64
- 1100 = T4 APLL frequency divided by 48
- 1101 = T4 APLL frequency divided by 16
- 1110 = T4 APLL frequency divided by 8
- 1111 = T4 APLL frequency divided by 4

AOF3=1: (alternate decodes)

- 0000 = Output disabled (i.e. low)
- 0001 = T0 APLL frequency divided by 64
- 0010 = T4 APLL frequency divided by 20
- 0011 = T4 APLL frequency divided by 12
- 0100 = T4 APLL frequency divided by 10
- 0101 = T4 APLL frequency divided by 5
- 0110 = T4 APLL frequency divided by 2
- 0111 to 1111 = undefined

**Register Name:** OCR3  
**Register Description:** Output Configuration Register 3  
**Register Address:** 62h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	OFREQ6[3:0]				0	0	0	0
<b>Default</b>	see below				0	0	0	0

**Bits 7 to 4: Output Frequency of OC6 (OFREQ6[3:0]).** This field specifies the frequency of output clock output OC6. The frequencies of the T0 APLL and T4 APLL are configured in the [T0CR1](#) and [T4CR1](#) registers. The Digital1 and Digital2 frequencies are configured in the [MCR7](#) register. See section [7.8.2.3](#). The default frequency is set by the O6F[2:0] bits, see [Table 7-16](#). The decode of this field is controlled by the value of the [OCR5.AOF6](#) bit.

AOF6=0: (standard decodes)

- 0000 = Output disabled (i.e. low)
- 0001 = 2 kHz
- 0010 = 8 kHz
- 0011 = T0 APLL frequency divided by 2
- 0100 = Digital1 (see [Table 7-6](#))
- 0101 = T0 APLL frequency
- 0110 = T0 APLL frequency divided by 16
- 0111 = T0 APLL frequency divided by 12
- 1000 = T0 APLL frequency divided by 8
- 1001 = T0 APLL frequency divided by 6
- 1010 = T0 APLL frequency divided by 4
- 1011 = T4 APLL frequency divided by 64
- 1100 = T4 APLL frequency divided by 48
- 1101 = T4 APLL frequency divided by 16
- 1110 = T4 APLL frequency divided by 8
- 1111 = T4 APLL frequency divided by 4

AOF6=1: (alternate decodes)

- 0000 = Output disabled (i.e. low)
- 0001 = T4 APLL frequency divided by 5
- 0010 = T4 APLL frequency divided by 2
- 0011 = T4 APLL frequency
- 0100 = T0 APLL2 frequency divided by 5
- 0101 = T0 APLL2 frequency divided by 2
- 0110 = T0 APLL2 frequency
- 0111 to 1111 = undefined

**Register Name:** OCR4  
**Register Description:** Output Configuration Register 4  
**Register Address:** 63h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	MFSEN	FSEN	0	0	0	0	0	0
<b>Default</b>	1	1	0	0	0	0	0	0

**Bit 7: MFSYNC Enable (MFSEN).** This configuration bit enables the 2 kHz output on the MFSYNC pin. See section 7.8.2.5.

0 = Disabled, driven low

1 = Enabled, output is 2 kHz

**Bit 6: FSYNC Enable (FSEN).** This configuration bit enables the 8 kHz output on the FSYNC pin. See section 7.8.2.5.

0 = Disabled, driven low

1 = Enabled, output is 8 kHz

**Register Name:** T4CR1  
**Register Description:** T4 APLL Configuration Register 1  
**Register Address:** 64h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	T4FREQ[3:0]			
<b>Default</b>	0	0	0	0	see below			

**Bits 3 to 0: T4 APLL Frequency (T4FREQ[3:0]).** When `T0CR1:T4APT0=0`, this field configures the T4 APLL DFS frequency. The T4 APLL DFS frequency affects the frequency of the T4 APLL which in turn affects the available output frequencies on the output clock pins (see the registers). See section 7.8.2. The default value of this field is controlled by the `O6F[2:0]` and `O3F[2:0]` pins as described in Table 7-15.

T4FREQ[3:0]	T4 APLL DFS Frequency	T4 APLL Frequency (4 x T4 APLL DFS)
0000	APLL output disabled	Disabled, output is low
0001	77.76 MHz	311.04 MHz (4 x 77.76 MHz)
0010	24.576 MHz (12 x E1)	98.304 MHz (48 x E1)
0011	32.768 MHz (16 x E1)	131.072 MHz (64 x E1)
0100	37.056 MHz (24 x DS1)	148.224 MHz (96 x DS1)
0101	24.704 MHz (16 x DS1)	98.816 MHz (64 x DS1)
0110	68.736 MHz (2 x E3)	274.944 MHz (8 x E3)
0111	44.736 MHz (DS3)	178.944 MHz (4 x DS3)
1000	25.248 MHz (4 x 6312 kHz)	100.992 MHz (16 x 6312 kHz)
1001	62.500 MHz (GbE ÷ 16)	250.000 MHz (GbE ÷ 4)
1010	30.720 MHz (3 x 10.24)	122.880 MHz (12 x 10.24)
1011	40.000 MHz (4 x 10 MHz)	160.000 MHz (16 x 10 MHz)
1100	26.000 MHz (2 x 13 MHz)	104.000 MHz (8 x 13 MHz)
1100 - 1111	{unused values}	{unused values}

**Register Name:** T0CR1  
**Register Description:** T0 DPLL Configuration Register 1  
**Register Address:** 65h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	T4APT0	T0FT4[2:0]			T0FREQ[2:0]		
<b>Default</b>	0	0	0	0	0	see below		

**Bit 6: T4 APLL Source from T0 (T4APT0).** When this bit is set to 0, T4CR1:T4FREQ configures the T4 APLL DFS frequency. The T4 APLL DFS frequency affects the frequency of the T4 APLL which in turn affects the available output frequencies on the output clock pins (see the registers). When this bit is set to 1, the frequency of the T4 APLL DFS is configured by the T0CR1:T0FT4[2:0] field below. See section 7.8.2.

0 = T4 APLL frequency is determined by T4FREQ

1 = T4 APLL frequency is determined by T0FT4

**Bits 5 to 3: T0 Frequency to T4 APLL (T0FT4[2:0]).** When the T4APT0 bit is set to 1, this field specifies the frequency of the T4 APLL DFS. This frequency can be different than the frequency specified by T0CR1:T0FREQ. See section 7.8.2.

T0FT4	T4 APLL DFS Frequency	T4 APLL Frequency (4 x T4 APLL DFS)
000 =	24.576 MHz (12 x E1)	98.304 MHz (48 x E1)
001 =	62.500 MHz (GbE ÷ 16)	250.000 MHz (GbE ÷ 4)
010 =	32.768 MHz (16 x E1)	131.072 MHz (64 x E1)
011 =	{unused value}	{unused value}
100 =	37.056 MHz (24 x DS1)	148.224 MHz (96 x DS1)
101 =	{unused value}	{unused value}
110 =	24.704 MHz (16 x DS1)	98.816 MHz (64 x DS1)
111 =	25.248 MHz (4 x 6312 kHz)	100.992 MHz (16 x 6312 kHz)

**Bits 2 to 0: T0 DPLL Output Frequency (T0FREQ[2:0]).** This field configures the T0 APLL DFS frequency. The T0 APLL DFS frequency affects the frequency of the T0 APLL, which in turn affects the available output frequencies on the output clock pins (see the registers). See section 7.8.2. The default frequency is controlled by the O6F[2:0] and O3F[2:0] pins as described in Table 7-14.

T0FREQ	T0 APLL DFS Frequency	T0 APLL Frequency (4 x T0 APLL DFS)
000 =	77.76 MHz	311.04 MHz (4 x 77.76 MHz)
001 =	77.76 MHz	311.04 MHz (4 x 77.76 MHz)
010 =	24.576 MHz (12 x E1)	98.304 MHz (48 x E1)
011 =	32.768 MHz (16 x E1)	131.072 MHz (64 x E1)
100 =	37.056 MHz (24 x DS1)	148.224 MHz (96 x DS1)
101 =	24.704 MHz (16 x DS1)	98.816 MHz (64 x DS1)
110 =	25.248 MHz (4 x 6312 kHz)	100.992 MHz (16 x 6312 kHz)
111 =	62.500 MHz (GbE ÷ 16)	250.000 MHz (GbE ÷ 4)

**Register Name:** T0LBW  
**Register Description:** T0 DPLL Locked Bandwidth Register  
**Register Address:** 67h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	0	0	0	RSV1	RSV2	T0LBW[2:0]		
<b>Default</b>	0	0	0	0	0	0	0	0

**Bit 4: Reserved Bit 1 (RSV1).** This bit is reserved for future use, it can be written to and read back.

**Bit 3: Reserved Bit 2 (RSV2).** This bit is reserved for future use, it can be written to and read back.

**Bits 2 to 0: T0 DPLL Locked Bandwidth (T0LBW[2:0]).** This field configures the bandwidth of the T0 DPLL when locked to an input clock. When AUTOBW=0 in the [MCR9](#) register, the T0LBW bandwidth is used for acquisition and for locked operation. When AUTOBW=1, [T0ABW](#) bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See section [7.7.2](#).

111 = 18 Hz  
 000 = 35 Hz (default)  
 001 = 70 Hz  
 010 = {unused value, undefined}  
 011 = 18 Hz  
 100 = 120 Hz  
 101 = 250 Hz  
 110 = 400 Hz

**Register Name:** T0ABW  
**Register Description:** T0 DPLL Acquisition Bandwidth Register  
**Register Address:** 69h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	0	0	0	RSV1	RSV2	T0ABW[2:0]		
<b>Default</b>	0	0	0	0	0	0	0	1

**Bit 4: Reserved Bit 1 (RSV1).** This bit is reserved for future use, it can be written to and read back.

**Bit 3: Reserved Bit 2 (RSV2).** This bit is reserved for future use, it can be written to and read back.

**Bits 2 to 0: T0 DPLL Acquisition Bandwidth (T0ABW[2:0]).** This field configures the bandwidth of the T0 DPLL when acquiring lock. When AUTOBW=0 in the [MCR9](#) register, the T0LBW bandwidth is used for acquisition and for locked operation. When AUTOBW=1, [T0ABW](#) bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See section [7.7.2](#).

111 = 18 Hz  
 000 = 35 Hz  
 001 = 70 Hz (default)  
 010 = {unused value, undefined}  
 011 = 18 Hz  
 100 = 120 Hz  
 101 = 250 Hz  
 110 = 400 Hz

**Register Name:** T0CR2  
**Register Description:** T0 Configuration Register 2  
**Register Address:** 6Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	PD2G8K[2:0]			--	DAMP[2:0]		
<b>Default</b>	0	0	0	1	0	1	0	0

**Bits 6 to 4: Phase Detector 2 Gain, 8 kHz (PD2G8K[2:0]).** This field specifies the gain of the T0 phase detector 2 with an input clock of 8 kHz or less. This value is only used if automatic gain selection is enabled by setting PD2EN=1 in the [T0CR3](#) register. See section [7.7.4](#).

**Bits 2 to 0: Damping Factor (DAMP[2:0]).** This field configures the damping factor of the T0 DPLL. Damping factor is a function of both DAMP[2:0] and the T0 DPLL bandwidth ([T0ABW](#) and [T0LBW](#)). The default value corresponds to a damping factor of 5. See section [7.7.3](#).

	18 Hz	35 Hz	≥ 70 Hz
001 =	1.2	1.2	1.2
010 =	2.5	2.5	2.5
011 =	5	5	5
100 =	5	10	10
101 =	5	10	20
000, 110 and 111 =	{unused values}		

The gain peak for each damping factor is shown below:

Damping Factor	Gain Peak
1.2	0.4 dB
2.5	0.2 dB
5	0.1 dB
10	0.06 dB
20	0.03 dB

**Register Name:** T0CR3  
**Register Description:** T0 Configuration Register 3  
**Register Address:** 6Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	PD2EN	--			PD2G[2:0]			
<b>Default</b>	1	1	0	0	0	0	1	0

**Bit 7: Phase Detector 2 Gain Enable (PD2EN).** When this bit is set to 1, the T0 phase detector 2 is enabled and the gain is determined by the input locking frequency. If the frequency is greater than 8 kHz, the gain is set by the PD2G field. If the frequency is less or equal to 8 kHz, the gain is set by the PD2G8K field in the [T0CR2](#) register. See section [7.7.4](#).

0 = Disable  
 1 = Enable

**Bits 2 to 0: Phase Detector 2 Gain (PD2G[2:0]).** This field specifies the gain of the T0 phase detector 2 when the input frequency is greater than 8 kHz. This value is only used if automatic gain selection is enabled by setting PD2EN=1. See section [7.7.4](#).

**Register Name:** GPCR  
**Register Description:** GPIO Configuration Register  
**Register Address:** 6Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	GPIO4D	GPIO3D	GPIO2D	GPIO1D	GPIO4O	GPIO3O	GPIO2O	GPIO1O
<b>Default</b>	0	0	0	0	0	0	0	0

**Bit 7: GPIO4 Direction (GPIO4D).** This bit configures the data direction for the GPIO4 pin. When GPIO4 is an input its current state can be read from [GPSR:GPIO4](#). When GPIO4 is an output, its value is controlled by the GPIO4O configuration bit.

0 = Input  
 1 = Output

**Bit 6: GPIO3 Direction (GPIO3D).** This bit configures the data direction for the GPIO3 pin. When GPIO3 is an input its current state can be read from [GPSR:GPIO3](#). When GPIO3 is an output, its value is controlled by the GPIO3O configuration bit.

0 = Input  
 1 = Output

**Bit 5: GPIO2 Direction (GPIO2D).** This bit configures the data direction for the GPIO2 pin. When GPIO2 is an input its current state can be read from [GPSR:GPIO2](#). When GPIO2 is an output, its value is controlled by the GPIO2O configuration bit.

0 = Input  
 1 = Output

**Bit 4: GPIO1 Direction (GPIO1D).** This bit configures the data direction for the GPIO1 pin. When GPIO1 is an input its current state can be read from [GPSR:GPIO1](#). When GPIO1 is an output, its value is controlled by the GPIO1O configuration bit.

0 = Input  
 1 = Output

**Bit 3: GPIO4 Output Value (GPIO4O).** When GPIO4 is configured as an output (GPIO4D=1) then this bit specifies the output value.

0 = Low  
 1 = High

**Bit 2: GPIO3 Output Value (GPIO3O).** When GPIO3 is configured as an output (GPIO3D=1) then this bit specifies the output value.

0 = Low  
 1 = High

**Bit 1: GPIO2 Output Value (GPIO2O).** When GPIO2 is configured as an output (GPIO2D=1) then this bit specifies the output value.

0 = Low  
 1 = High

**Bit 0: GPIO1 Output Value (GPIO1O).** When GPIO1 is configured as an output (GPIO1D=1) then this bit specifies the output value.

0 = Low  
 1 = High

**Register Name:** GPSR  
**Register Description:** GPIO Status Register  
**Register Address:** 6Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	GPIO4	GPIO3	GPIO2	GPIO1
<b>Default</b>	0	0	0	0	0	1	0	0

**Bit 3: GPIO4 State (GPIO4).** This bit indicates the current state of the GPIO4 pin.

0 = low

1 = high

**Bit 2: GPIO3 State (GPIO3).** This bit indicates the current state of the GPIO3 pin.

0 = low

1 = high

**Bit 2: GPIO2 State (GPIO2).** This bit indicates the current state of the GPIO2 pin.

0 = low

1 = high

**Bit 1: GPIO1 State (GPIO1).** This bit indicates the current state of the GPIO1 pin.

0 = low

1 = high

**Register Name:** PHLIM1  
**Register Description:** Phase Limit Register 1  
**Register Address:** 73h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	FLEN	NALOL	1	--	--	FINELIM[2:0]		
<b>Default</b>	1	0	1	0	0	0	1	0

**Bit 7: Fine Phase Limit Enable (FLEN).** This configuration bit enables the fine phase limit specified in the FINELIM[2:0] field. The fine limit must be disabled for multi-UI jitter tolerance (see [PHLIM2](#) fields). See section [7.7.5](#).

0 = Disabled

1 = Enabled

**Bit 6: No-Activity Loss of Lock (NALOL).** The T0 DPLL can detect that an input clock has no activity very quickly (within two clock cycles). When NALOL=0, loss-of-lock is not declared when clock cycles are missing, and nearest edge locking ( $\pm 180^\circ$ ) is used when the clock recovers. This gives tolerance to missing cycles. When NALOL=1, loss-of-lock is indicated as soon as no activity is detected, and the device switches to phase/frequency locking ( $\pm 360^\circ$ ). See sections [7.5.3](#) and [7.7.5](#).

0 = No activity does not trigger loss-of-lock

1 = No activity does trigger loss-of-lock

**Bit 5:** Leave set to 1 (test control).

**Bits 2 to 0: Fine Phase Limit (FINELIM[2:0]).** This field specifies the fine phase limit window, outside of which loss-of-lock is declared. The FLEN bit enables this feature. The phase of the input clock has to be inside the fine limit window for two seconds before phase lock is declared. Loss-of-lock is declared immediately if the phase of the input clock is outside the phase limit window. The default value of 010 is appropriate for most situations. See section [7.7.5](#).

000 = Always indicates loss of phase lock—do not use

001 = Small phase limit window,  $\pm 45$  to  $\pm 90^\circ$

010 = Normal phase limit window,  $\pm 90$  to  $\pm 180^\circ$  (default)

100, 101, 110, 111 = Proportionately larger phase limit window

**Register Name:** PHLIM2  
**Register Description:** Phase Limit Register 2  
**Register Address:** 74h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	CLEN	MCPDEN	USEMCPD	--	COARSELIM[3:0]			
<b>Default</b>	1	1	1	0	0	1	0	1

**Bit 7: Coarse Phase Limit Enable (CLEN).** This configuration bit enables the coarse phase limit specified in the COARSELIM[3:0] field. See section 7.7.5.

0 = Disabled  
 1 = Enabled

**Bit 6: Multi-Cycle Phase Detector Enable (MCPDEN).** This configuration bit enables the multi-cycle phase detector and allows the DPLL to tolerate large-amplitude jitter and wander. The range of this phase detector is the same as the coarse phase limit specified in the COARSELIM[3:0] field. See section 7.7.4.

0 = Disabled  
 1 = Enabled

**Bit 5: Use Multi-Cycle Phase Detector in the DPLL Algorithm (USEMCPD).** This configuration bit enables the DPLL algorithm to use the multi-cycle phase detector so that a large phase measurement drives faster DPLL pull-in. When USEMCPD=0, phase measurement is limited to  $\pm 360^\circ$ , giving slower pull-in at higher frequencies but with less overshoot. When USEMCPD=1, phase measurement is set as specified in the COARSELIM[3:0] field, giving faster pull-in. MCPDEN should be set to 1 when USEMCPD=1. See section 7.7.4.

0 = Disabled  
 1 = Enabled

**Bits 3 to 0: Coarse Phase Limit (COARSELIM[3:0]).** This field specifies the coarse phase limit and the tracking range of the multi-cycle phase detector. The CLEN bit enables this feature. If jitter tolerance greater than 0.5 UI is required and the input clock is a high frequency signal then the DPLL can be configured to track phase errors over many UI using the multi-cycle phase detector. See section 7.7.4 and 7.7.5.

0000 =  $\pm 1$  UI  
 0001 =  $\pm 3$  UI  
 0010 =  $\pm 7$  UI  
 0011 =  $\pm 15$  UI  
 0100 =  $\pm 31$  UI  
 0101 =  $\pm 63$  UI  
 0110 =  $\pm 127$  UI  
 0111 =  $\pm 255$  UI  
 1000 =  $\pm 511$  UI  
 1001 =  $\pm 1023$  UI  
 1010 =  $\pm 2047$  UI  
 1011 =  $\pm 4095$  UI  
 1100 to 1111 =  $\pm 8191$  UI

**Register Name:** PHMON  
**Register Description:** Phase Monitor Register  
**Register Address:** 76h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	NW	--	--	--	--			
<b>Default</b>	0	0	0	0	0	1	1	0

**Bit 7: Low-Frequency Input Clock Noise Window (NW).** For 2 kHz, 4 kHz or 8 kHz input clocks, this configuration bit enables a  $\pm 5\%$  tolerance noise window centered around the expected clock edge location. Noise-induced edges outside this window are ignored, reducing the possibility of phase hits on the output clocks. This bit should be enabled only when the T0 DPLL is locked to an input and the 180 phase detector is being used.

0 = All edges are recognized by the T0 DPLL

1 = Only edges within the  $\pm 5\%$  tolerance window are recognized by the T0 DPLL

**Register Name:** PHASE1  
**Register Description:** Phase Register 1  
**Register Address:** 77h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	PHASE[7:0]							
<b>Default</b>	0	0	0	0	0	0	0	0

The PHASE1 and PHASE2 registers must be read consecutively. See section [8.3](#).

**Bits 7 to 0: Current DPLL Phase (PHASE[7:0]).** The full 16-bit PHASE[15:0] field spans this register and the [PHASE2](#) register. PHASE is a 2's-complement signed integer that indicates the current value of the phase detector. The value is the output of the phase averager. The averaged phase difference in degrees is equal to PHASE \* 0.707. See section [7.7.6](#).

**Register Name:** PHASE2  
**Register Description:** Phase Register 2  
**Register Address:** 78h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	PHASE[15:8]							
<b>Default</b>	0	0	0	0	0	0	0	0

**Bits 7 to 0: Current DPLL Phase (PHASE[15:8]).** See the [PHASE1](#) register description.

**Register Name:** FSCR1  
**Register Description:** Frame Sync Configuration Register 1  
**Register Address:** 7Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	8KINV	8KPUL	2KINV	2KPUL
<b>Default</b>	0	0	0	0	0	0	0	0

**Bit 3: 8 kHz Invert (8KINV).** When this bit is set to 1 the 8 kHz signal on clock output FSYNC is inverted. See section [7.8.2.5](#).

- 0 = FSYNC not inverted
- 1 = FSYNC inverted

**Bit 2: 8 kHz Pulse (8KPUL).** When this bit is set to 1, the 8 kHz signal on clock output FSYNC is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of FSYNC is equal to the clock period of OC3. See section [7.8.2.5](#).

- 0 = FSYNC not pulsed; 50% duty cycle
- 1 = FSYNC pulsed, with pulse width equal to OC3 period

**Bit 1: 2 kHz Invert (2KINV).** When this bit is set to 1 the 2 kHz signal on clock output MFSYNC is inverted. See section [7.8.2.5](#).

- 0 = MFSYNC not inverted
- 1 = MFSYNC inverted

**Bit 0: 2 kHz Pulse (2KPUL).** When this bit is set to 1, the 2 kHz signal on clock output MFSYNC is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of MFSYNC is equal to the clock period of OC3. See section [7.8.2.5](#).

- 0 = MFSYNC not pulsed; 50% duty cycle
- 1 = MFSYNC pulsed, with pulse width equal to OC3 period

**Register Name:** INTCR  
**Register Description:** Interrupt Configuration Register  
**Register Address:** 7Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	--	--	--	--	LOS	GPO	OD	POL
<b>Default</b>	0	0	0	0	1	0	1	0

**Bit 3: INTREQ Pin Mode (LOS).** When GPO=0 this bit selects the function of the INTREQ pin.  
 0 = The INTREQ/LOS pin indicates interrupt requests  
 1 = The INTREQ/LOS pin indicates the real-time state of the selected reference activity monitor (see section 7.5.3).

**Bit 2: INTREQ Pin General Purpose Output Enable (GPO).** When set to 1 this bit configures the interrupt request pin to be a general purpose output whose value is set by the POL bit.  
 0 = INTREQ is function determined by the LOS bit  
 1 = INTREQ is a general purpose output

**Bit 1: INTREQ Pin Open Drain Enable (OD).**  
 When GPO = 0:  
 0 = INTREQ is driven in both inactive and active states  
 1 = INTREQ is driven high or low in the active state but is high impedance in the inactive state  
 When GPO = 1:  
 0 = INTREQ is driven as specified by POL  
 1 = INTREQ is high impedance and POL has no effect

**Bit 0: INTREQ Pin Polarity (POL).**  
 When GPO = 0:  
 0 = INTREQ goes low to signal an interrupt request or LOS (active low)  
 1 = INTREQ goes high to signal interrupt request or LOS (active high)  
 When GPO = 1:  
 0 = INTREQ driven low  
 1 = INTREQ driven high

**Register Name:** PROT  
**Register Description:** Protection Register  
**Register Address:** 7Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<b>Name</b>	PROT[7:0]							
<b>Default</b>	1	0	0	0	0	1	0	1

**Bits 7 to 0: Protection Control (PROT[7:0]).** This field can be used to protect the rest of the register set from inadvertent writes. In protected mode writes to all other registers are ignored. In single unprotected mode, one register (other than PROT) can be written, but after that write the device reverts to protected mode (and the value of PROT is internally changed to 00h). In fully unprotected mode all register can be written without limitation. See section 7.2.  
 1000 0101 = Fully unprotected mode  
 1000 0110 = Single unprotected mode  
 all other values = Protected mode

## 9 JTAG TEST ACCESS PORT AND BOUNDARY SCAN

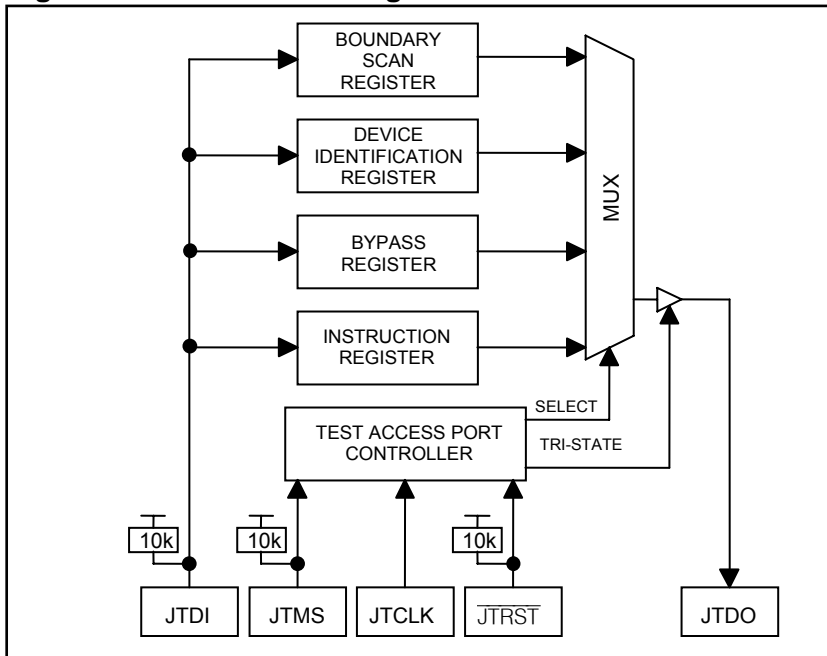
### 9.1 JTAG Description

The DS3106 supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. Figure 9-1 shows a block diagram. The DS3106 contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

Test Access Port (TAP)	Bypass Register
TAP Controller	Boundary Scan Register
Instruction Register	Device Identification Register

The TAP has the necessary interface pins, namely JTCLK,  $\overline{\text{JTRST}}$ , JTDI, JTDO, and JTMS. Details on these pins can be found in Table 6-5. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

Figure 9-1. JTAG Block Diagram



### 9.2 JTAG TAP Controller State Machine Description

This section discusses the operation of the TAP controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. Each of the states denoted in Figure 9-2 are described in the following paragraphs.

**Test-Logic-Reset.** Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

**Run-Test-Idle.** Run-Test-Idle is used between scan operations or during specific tests. The instruction register and all test registers remain idle.

**Select-DR-Scan.** All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

**Capture-DR.** Data can be parallel-loaded into the test register selected by the current instruction. If the instruction does not call for a parallel load or the selected test register does not allow parallel loads, the register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

**Shift-DR.** The test register selected by the current instruction is connected between JTDI and JTDO and data is shifted one stage toward the serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

**Exit1-DR.** While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

**Pause-DR.** Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

**Exit2-DR.** While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

**Update-DR.** A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

**Select-IR-Scan.** All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

**Capture-IR.** The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

**Shift-IR.** In this state, the instruction register's shift register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and the test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state, while moving data one stage through the instruction shift register.

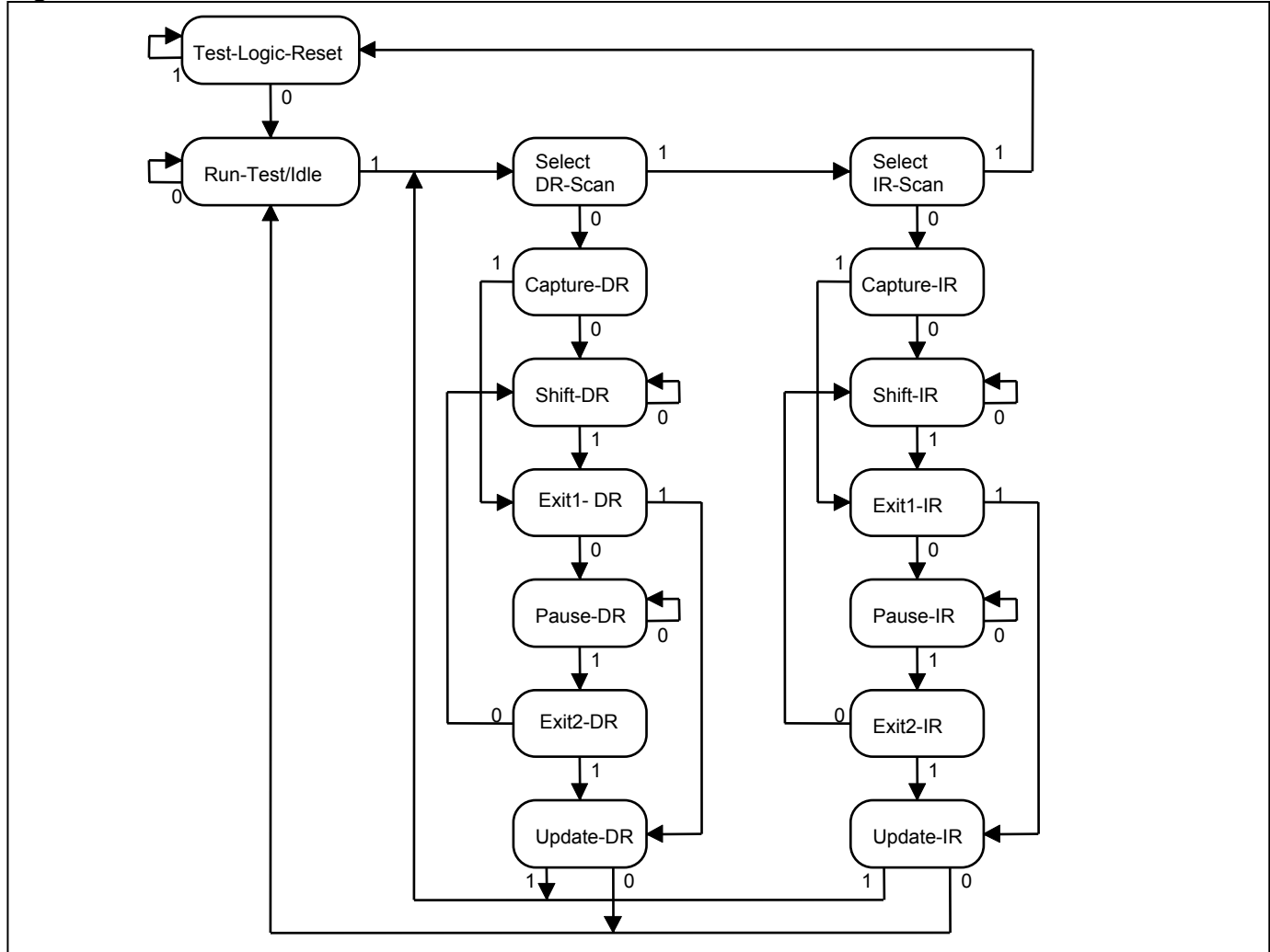
**Exit1-IR.** A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

**Pause-IR.** Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

**Exit2-IR.** A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

**Update-IR.** The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

**Figure 9-2. JTAG TAP Controller State Machine**



**9.3 JTAG Instruction Register and Instructions**

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 9-1 shows the instructions supported by the DS3106 and their respective operational binary codes.

**Table 9-1. JTAG Instruction Codes**

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

**SAMPLE/PRELOAD.** SAMPLE/RELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. First, the digital I/Os of the device can be sampled at the boundary scan register, using the Capture-DR state, without interfering with the device’s normal operation. Second, data can be shifted into the boundary scan register through JTDI using the Shift-DR state.

**EXTEST.** EXTEST allows testing of the interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur: (1) Once the EXTEST instruction is enabled through the Update-IR state, the parallel outputs of the digital output pins are driven. (2) The boundary scan register is connected between JTDI and JTDO. (3) The Capture-DR state samples all digital inputs into the boundary scan register.

**BYPASS.** When the BYPASS instruction is latched into the parallel instruction register, JTDI is connected to JTDO through the 1-bit bypass register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

**IDCODE.** When the IDCODE instruction is latched into the parallel instruction register, the device identification register is selected. The device ID code is loaded into the device identification register on the rising edge of JTCLK, following entry into the Capture-DR state. Shift-DR can be used to shift the ID code out serially through JTDO. During Test-Logic-Reset, the ID code is forced into the instruction register's parallel output.

**HIGHZ.** All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

**CLAMP.** All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

## 9.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the device design. It is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

**Bypass Register.** This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO.

**Boundary Scan Register.** This register contains a shift register path and a latched parallel output for control cells and digital I/O cells. BSDL files are available at [www.maxim-ic.com/TechSupport/telecom/bsdl.htm](http://www.maxim-ic.com/TechSupport/telecom/bsdl.htm).

**Identification Register.** This register contains a 32-bit shift register and a 32-bit latched parallel output. It is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device identification code for the DS3106 is shown in Table 9-2.

**Table 9-2. JTAG ID Code**

DEVICE	REVISION	DEVICE CODE	MANUFACTURER CODE	REQUIRED
DS3106	Consult factory	0000000010100100	00010100001	1

## 10 ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin with Respect to $V_{SS}$ (except $V_{DD}$ )	-0.3V to +5.5V
Supply Voltage Range ( $V_{DD}$ ) with Respect to $V_{SS}$	-0.3V to +1.98V
Supply Voltage Range ( $V_{DDIO}$ ) with Respect to $V_{SS}$	-0.3V to +3.63V
Ambient Operating Temperature Range	-40°C to +85°C
Junction Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.

**Note:** The typical values listed in the tables of section 10 are not production tested.

### 10.1 DC Characteristics

**Table 10-1. Recommended DC Operating Conditions**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, Core	VDD		1.62	1.8	1.98	V
Supply Voltage, I/O	VDDIO		3.135	3.3	3.465	V
Ambient Temperature Range	$T_A$		-40		+85	°C
Junction Temperature Range	$T_J$		-40		+125	°C

**Table 10-2. DC Characteristics**

(VDD = 1.8V ± 10%; VDDIO = 3.3V ± 5%,  $T_A$  = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Core	$I_{DD}$	Note 1, 2		TBD	TBD	mA
Supply Current, I/O	$I_{DDIO}$	Note 1, 2		TBD	TBD	mA
Supply Current from VDD_OC6 When Output OC6 Enabled	$I_{DDOC6}$	Note 3		16		mA
Input Capacitance	$C_{IN}$			5		pF
Output Capacitance	$C_{OUT}$			7		pF

**Note 1:** 12.800 MHz clock applied to REFCLK and 19.44 MHz clock applied to one CMOS/TTL input clock pin. Output clock pin OC3 at 19.44 MHz driving 100 pF load; all other inputs at VDDIO or grounded; all other outputs disabled and open.

**Note 2:** TYP current measured at VDD=1.8V and VDDIO=3.3V, MAX current measured at VDD=1.98V and VDDIO=3.465V

**Note 3:** 19.44MHz output clock frequency, driving the load shown in [Figure 10-1](#).

**Table 10-3. CMOS/TTL Pins**(VDD = 1.8V ± 10%; VDDIO = 3.3V ± 5%, T<sub>A</sub> = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V <sub>IH</sub>		2.0		5.5	V
Input Low Voltage	V <sub>IL</sub>		-0.3		+0.8	V
Input Leakage	I <sub>IL</sub>	Note 1	-10		+10	μA
Input Leakage, pins with internal pull-up resistor (50kΩ typical)	I <sub>ILPU</sub>	Note 1	-85		+10	μA
Input Leakage, pins with internal pull-down resistor (50kΩ typical)	I <sub>ILPD</sub>	Note 1	-10		+85	μA
Output Leakage (when High-Z)	I <sub>LO</sub>	Note 1	-10		+10	μA
Output High Voltage (I <sub>O</sub> = -4.0mA)	V <sub>OH</sub>		2.4		VDDIO	V
Output High Voltage (I <sub>O</sub> = -4.0mA)	V <sub>OH</sub>	Note 2	2.0		VDDIOB	V
Output Low Voltage (I <sub>O</sub> = +4.0mA)	V <sub>OL</sub>		0		0.4	V

**Note 1:** 0V < V<sub>IN</sub> < VDDIO for all other digital inputs.**Note 2:** For OC1B through OC5B when VDDIOB=2.5V.**Table 10-4. LVDS Output Pins**(VDD = 1.8V ± 10%; VDDIO = 3.3V ± 5%, T<sub>A</sub> = -40°C to +85°C)

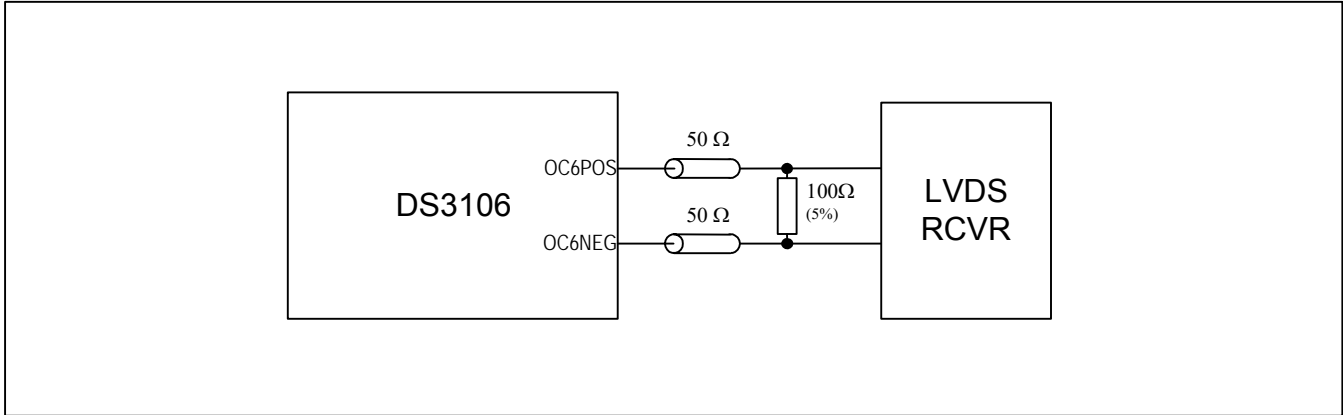
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OHLVDS</sub>	Note 1			1.6	V
Output Low Voltage	V <sub>OLLVDS</sub>	Note 1	0.9			V
Differential Output Voltage	V <sub>ODLVDS</sub>		247	350	454	mV
Output Offset (Common Mode) Voltage	V <sub>OSLVDS</sub>	25°C, Note 1	1.125	1.25	1.375	V
Difference in Magnitude of Output Differential Voltage for Complementary States	V <sub>DOSLVDS</sub>				25	mV

**Note 1:** With 100Ω load across the differential outputs.**Note 2:** The differential output can easily be interfaced to an LVDS, LVPECL or CML input on a neighboring IC using a few external passive components. See [Maxim App Note HFAN-1.0](#) for details.**Table 10-5. LVPECL Level-Compatible Output Pins**(VDD = 1.8V ± 10%; VDDIO = 3.3V ± 5%, T<sub>A</sub> = -40°C to +85°C)

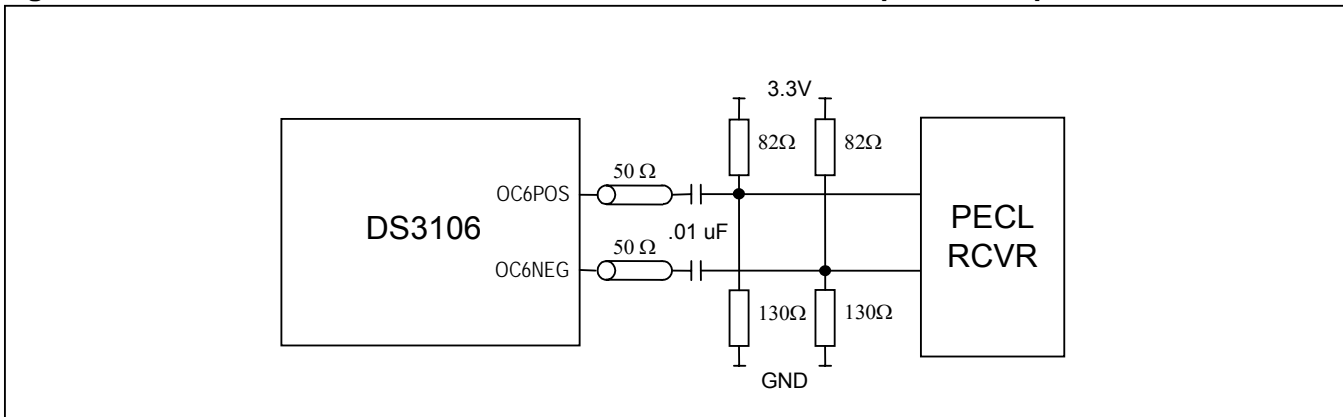
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Voltage	V <sub>ODPECL</sub>		595	700	930	mV
Output Offset (Common Mode) Voltage	V <sub>OSPECL</sub>	25°C, Note 1		0.8		V
Difference in Magnitude of Output Differential Voltage for Complementary States	V <sub>DOSPECL</sub>				50	mV

**Note 1:** With 100Ω load across the differential outputs.**Note 2:** The differential output can easily be interfaced to an LVDS, LVPECL or CML input on a neighboring IC using a few external passive components. See [Maxim App Note HFAN-1.0](#) for details.

**Figure 10-1. Recommended Termination for LVDS Output Pins**



**Figure 10-2 Recommended Termination for LVPECL Level-Compatible Output Pins**



## 10.2 Input Clock Timing

**Table 10-6. Input Clock Timing**

(VDD = 1.8V ± 10%; VDDIO = 3.3V ± 5%, T<sub>A</sub> = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Duty Cycle			30		70	%

## 10.3 Output Clock Timing

**Table 10-7. Input Clock to Output Clock Delay**

INPUT FREQUENCY	OUTPUT FREQUENCY	DELAY, INPUT CLOCK EDGE TO OUTPUT CLOCK EDGE
8 kHz	8 kHz	0.0 ± 1.5ns
6.48 MHz	6.48 MHz	-12 ± 1.5ns
19.44 MHz	19.44 MHz	0.0 ± 1.5ns
25.92 MHz	25.92 MHz	0.0 ± 1.5ns
38.88 MHz	38.88 MHz	0.0 ± 1.5ns
51.84 MHz	51.84 MHz	0.0 ± 1.5ns
77.76 MHz	77.76 MHz	0.0 ± 1.5ns
155.52 MHz	155.52 MHz	0.0 ± 1.5ns

**Table 10-8. Output Clock Phase Alignment, Frame Sync Alignment Mode**

OUTPUT FREQUENCY	DELAY, MFSYNC FALLING EDGE TO OUTPUT CLOCK FALLING EDGE
8 kHz (FSYNC)	0.0 ± 0.5ns
2 kHz	0.0 ± 0.5ns
8 kHz	0.0 ± 0.5ns
1.544 MHz	0.0 ± 1.25ns
2.048 MHz	0.0 ± 1.25ns
44.736 MHz	-2.0 ± 1.25ns
34.368 MHz	-2.0 ± 1.25ns
6.48 MHz	-2.0 ± 1.25ns
19.44 MHz	-2.0 ± 1.25ns
25.92 MHz	-2.0 ± 1.25ns
38.88 MHz	-2.0 ± 1.25ns
51.84 MHz	-2.0 ± 1.25ns
77.76 MHz	-2.0 ± 1.25ns
155.52 MHz	-2.0 ± 1.25ns
311.04 MHz	-2.0 ± 1.25ns

### 10.4 SPI Interface Timing

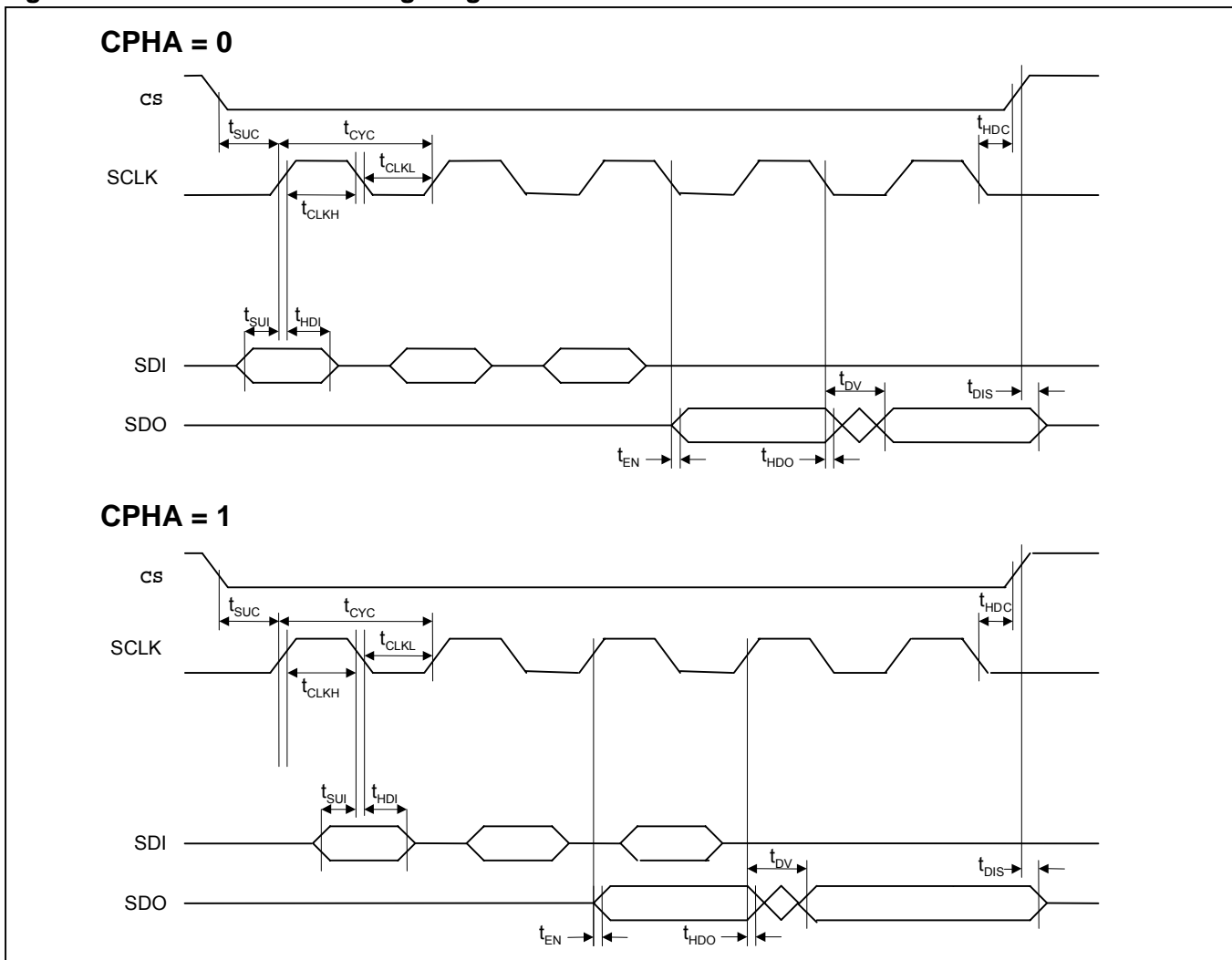
**Table 10-9. SPI Interface Timing**

(VDD = 1.8V ± 10%; VDDIO = 3.3V ± 5%, T<sub>A</sub> = -40°C to +85°C) (Figure 10-3)

PARAMETER (Note 1)	SYMBOL	MIN	TYP	MAX	UNITS
SCLK Frequency	f <sub>BUS</sub>			6	MHz
SCLK Cycle Time	t <sub>CYC</sub>	100			ns
CS Setup to First SCLK Edge	t <sub>SUC</sub>	15			ns
CS Hold time After Last SCLK Edge	t <sub>HDC</sub>	15			ns
SCLK High Time	t <sub>CLKH</sub>	50			ns
SCLK Low Time	t <sub>CLKL</sub>	50			ns
SDI Data Setup Time	t <sub>SUI</sub>	5			ns
SDI Data Hold Time	t <sub>HDI</sub>	15			ns
SDO Enable Time (High-Impedance to Output Active)	t <sub>EN</sub>	0			ns
SDO Disable Time (Output Active to High-Impedance)	t <sub>DIS</sub>			25	ns
SDO Data Valid Time	t <sub>DV</sub>			50	ns
SDO Data Hold Time After Update SCLK Edge	t <sub>HDO</sub>	5			ns

**Note 1:** All timing is specified with 100 pF load on all SPI pins.

**Figure 10-3. SPI Interface Timing Diagram**



### 10.5 JTAG Interface Timing

**Table 10-10. JTAG Interface Timing**

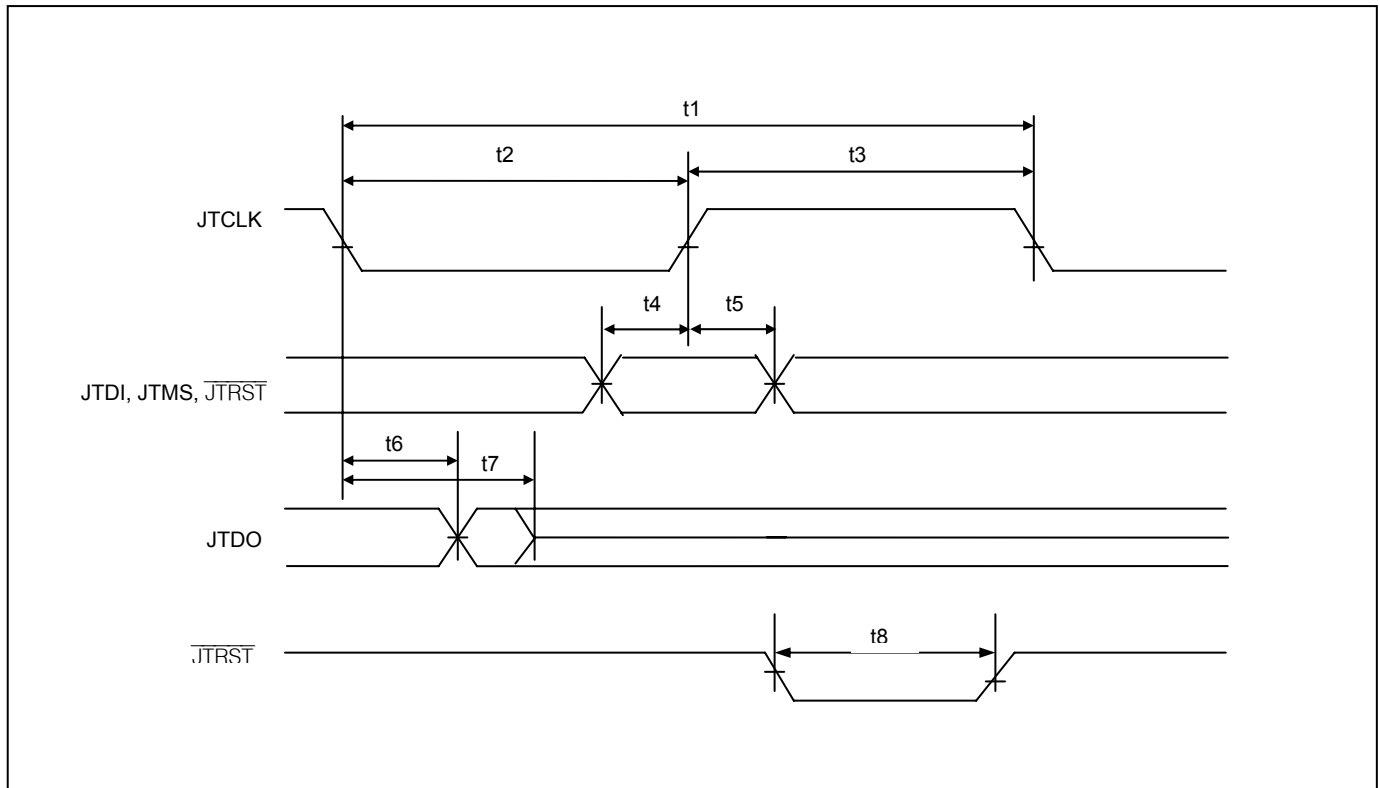
(VDD = 1.8V ± 10%; VDDIO = 3.3V ± 5%, T<sub>A</sub> = -40°C to +85°C) (Figure 10-4)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1		1000		ns
JTCLK Clock High/Low Time (Note 1)	t2/t3	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4	50			ns
JTCLK to JTDI, JTMS Hold Time	t5	50			ns
JTCLK to JTDO Delay	t6	2		50	ns
JTCLK to JTDO High-Z Delay (Note 2)	t7	2		50	ns
JTRST Width Low Time	t8	100			ns

**Note 1:** Clock can be stopped high or low.

**Note 2:** Not tested during production test.

**Figure 10-4. JTAG Timing Diagram**



## 10.6 Reset Pin Timing

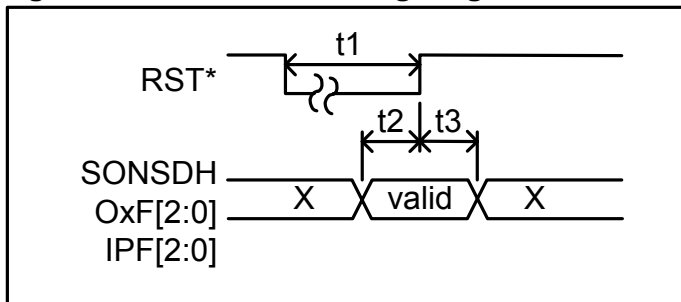
**Table 10-11. Reset Pin Timing**

(VDD = 1.8V ± 10%; VDDIO = 3.3V ± 5%, T<sub>A</sub> = -40°C to +85°C) (Figure 10-5)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
$\overline{\text{RST}}$ low time (Note 1)	t1	1000			ns
SONSDH, IFP[2:0], O3F[2:0], O6F[2:0] Setup Time to $\overline{\text{RST}}$	t2	0			ns
SONSDH, IFP[2:0], O3F[2:0], O6F[2:0] Hold Time from $\overline{\text{RST}}$	t3	50			ns

**Note 1:**  $\overline{\text{RST}}$  should be held low while the REFCLK oscillator stabilizes. It is recommended to force  $\overline{\text{RST}}$  low during power up. The 1000 ns minimum time applies if the  $\overline{\text{RST}}$  pulse is applied any time after the device has powered up and the oscillator has stabilized.

**Figure 10-5. Reset Pin Timing Diagram**



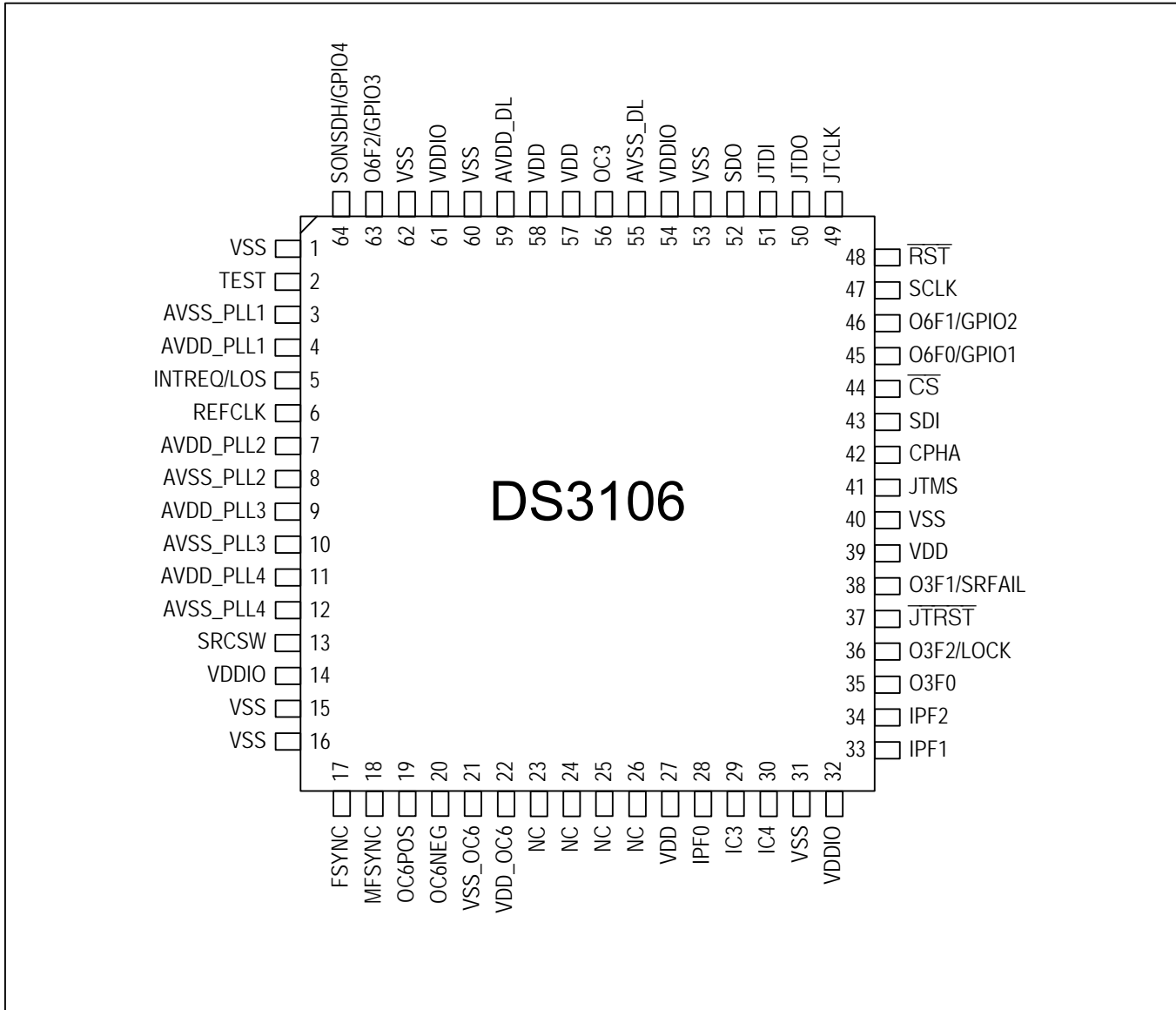
## 11 PIN ASSIGNMENTS

Table 11-1 below lists pin assignments sorted in alphabetical order by pin name. Figure 11-1 show pin assignments arranged by pin number.

**Table 11-1. Pin Assignments Sorted by Signal Name**

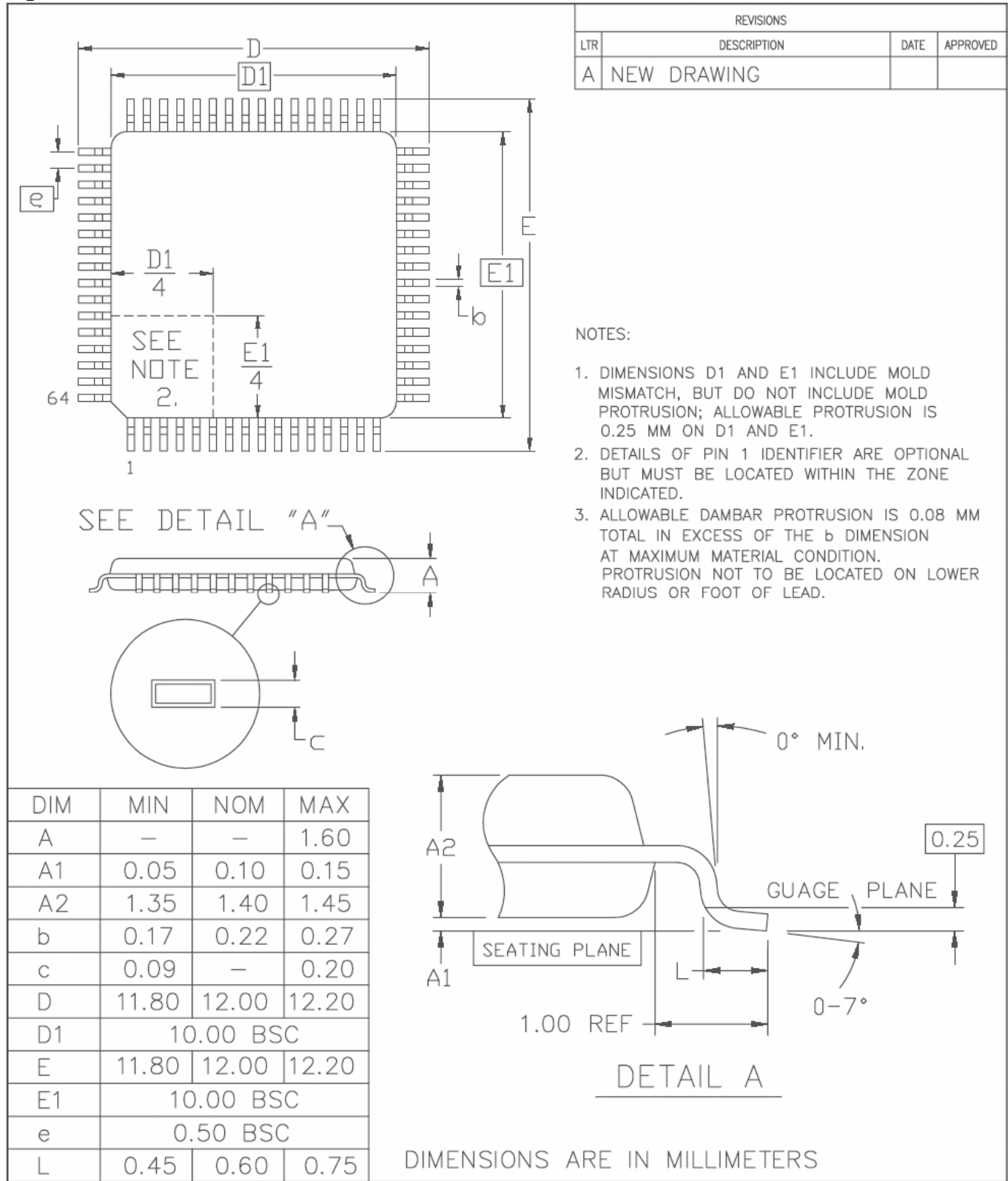
PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER
AVDD_DL	59	MFSYNC	18
AVDD_PLL1	4	NC	23, 24, 25, 26
AVDD_PLL2	7	O3F0	35
AVDD_PLL3	9	O3F1 / SRFAIL	38
AVDD_PLL4	11	O3F2 / LOCK	36
AVSS_DL	55	O6F0 / GPIO1	45
AVSS_PLL1	3	O6F1 / GPIO2	46
AVSS_PLL2	8	O6F2 / GPIO3	63
AVSS_PLL3	10	OC3	56
AVSS_PLL4	12	OC6NEG	19
CPHA	42	OC6POS	20
$\overline{\text{CS}}$	44	REFCLK	6
FSYNC	17	$\overline{\text{RST}}$	48
IC3	29	SCLK	47
IC4	30	SDI	43
INTREQ / LOS	5	SDO	52
IPF0	28	SONSDH / GPIO4	64
IPF1	33	SRCSW	13
IPF2	34	TEST	2
JTCLK	49	VDD	27, 39, 57, 58
JTDI	51	VDDIO	14, 32, 54, 61
JTDO	50	VDD_OC6	22
JTMS	41	VSS	1, 15, 16, 31, 40, 53, 60, 62
$\overline{\text{JTRST}}$	37	VSS_OC6	21

Figure 11-1. Pin Assignment Diagram



## 12 MECHANICAL INFORMATION

Figure 12-1. LQFP Mechanical Dimensions



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING		

NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM ON D1 AND E1.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.

**Table 12-1. LQFP Thermal Properties, Natural Convection**

PARAMETER	MIN	TYP	MAX
Ambient Temperature (Note 1)	-40°C	—	+85°C
Junction Temperature	-40°C	—	+125°C
Theta-JA ( $\theta_{JA}$ ), Still Air (Note 2)		TBD °C/W	
Psi-JB		TBD °C/W	
Psi-JT		TBD °C/W	

**Note 1:** The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

**Note 2:** Theta-JA ( $\theta_{JA}$ ) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

**Table 12-2. LQFP Theta-JA ( $\theta_{JA}$ ) vs. Airflow**

FORCED AIR (METERS PER SECOND)	THETA-JA ( $\theta_{JA}$ )
0	TBD °C/W
1	TBD °C/W
2.5	TBD °C/W

## 13 ACRONYMS AND ABBREVIATIONS

AIS	alarm indication signal
AMI	alternate mark inversion
APLL	analog phase locked loop
BITS	building integrated timing supply
BPV	bipolar violation
DFS	digital frequency synthesis
DPLL	digital phase locked loop
ESF	extended superframe
EXZ	excessive zeros
GbE	gigabit ethernet
I/O	input/output
LOS	loss of signal
LVDS	low voltage differential signal
LVPECL	low voltage positive emitter-coupled logic
MTIE	Maximum Time Interval Error
OCXO	oven controlled crystal oscillator
OOF	out of frame alignment
PBO	phase build-out
PFD	phase/frequency detector
PLL	phase locked loop
ppb	parts per billion
ppm	parts per million
pk-pk	peak-to-peak
rms	root-mean-square
RAI	remote alarm indication
RO	read-only
R/W	read/write
SDH	synchronous digital hierarchy
SEC	SDH equipment clock
SETS	synchronous equipment timing source
SF	superframe
SONET	synchronous Optical Network
SSM	synchronization status message
SSU	synchronization supply unit
STM	synchronous Transport Module
TDEV	time deviation
TCXO	temperature compensated crystal oscillator
UI	unit interval
UIpp	unit interval, peak to peak
XO	crystal oscillator

## TRADEMARK ACKNOWLEDGEMENTS

Motorola is a registered trademark of Motorola, Inc.

Semtech and Semtech Corp. are registered trademarks of Semtech Corporation.

SPI is a trademark of Motorola, Inc.

Telcordia is a registered trademark of Telcordia Technologies

## 14 DATA SHEET REVISION HISTORY

REVISION	DESCRIPTION
02/28/07	First version released to customers.
3/1/07	In the <b>ICR</b> register description, updated the <b>FREQ</b> field description explicitly mention its use in <b>LOCK8K</b> mode and to indicate that 31.25 MHz is not a valid setting for <b>LOCK8K</b> mode.
3/5/07	Updated section 7.4 to indicate minimum high time or low time is 3ns or 30% of clock period, whichever is smaller. In section 7.8.1 added hyperlink to Maxim app note HFAN-1.0. Added Note 2 to Table 10-4. Added Note 2 to Table 10-5. Updated Table 10-6 to clarify minimum high time and low time (and therefore duty cycle) for input clocks.
3/9/07	Deleted reference to IEEE1596.3 standard from Table 1-1.
4/3/07	Added section 7.12.
4/4/07	Deleted mention of slave mode from <b>MCR9:AUTOBW</b> bit description. In the <b>OPSTATE</b> register description, changed the default value of bit 6 to 0.
4/17/07	In Table 10-5 deleted <b>VOHPECL</b> and <b>VOLPECL</b> specs and changed <b>VOSPECL</b> spec to 0.8V typical. Added information about custom clock rates to page 1 bullets and section 5 bullets, and added a new section 7.8.2.6. Changed caption for Table 7-13 from “Possible Frequencies” to “Standard Frequencies”.
4/30/07	In section 7.5.3, second paragraph, first sentence, deleted “frequency range error” as a criteria for entering mini holdover. Changed pin name <b>INTREQ/SRFAIL</b> to <b>INTREQ/LOS</b> and changed register bit <b>INTCR:SRFAIL</b> to <b>LOS</b> . This affected the pin description in Table 6-3, the name of <b>INTCR</b> bit 3 in Table 8-1, the <b>MSR2:SRFAIL</b> register description, and the bit descriptions for <b>INTCR</b> . Also changed the pin name from <b>INTREQ/SRFAIL</b> to <b>INTREQ/LOS</b> in Figure 11-1 and Table 11-1.
5/10/07	Edited register <b>T4BW</b> to not have bit 2. Updated the data sheet in several places to indicate <b>CMOS/TTL</b> input clock pins can accept any multiple of 2kHz up to 125MHz. In Table 7-8, added frequencies 45.824, 22.912, 29.824 and 14.912 MHz. In the <b>DLIMIT1</b> register description, corrected the default value to FFh. In the <b>T0LBW</b> register definition, changed the default value to 00h. In the <b>T0ABW</b> register definition, changed the default value to 01h.
5/18/07	Updated page 1 feature bullet, section 5 feature bullet and section 7.8.2.6 text to indicate maximum custom frequency is 311.04MHz. In Figure 7-1, changed <b>OC10</b> to <b>FSYNC</b> , <b>OC11</b> to <b>MFSYNC</b> , <b>OCnEN</b> to <b>FSEN</b> and <b>MFSEN</b> , <b>OCnINV</b> to <b>8KINV</b> and <b>2KINV</b> , and <b>OCnPOL</b> to <b>8KPOL</b> and <b>2KPOL</b> . In Table 10-3, changed max from <b>VDD</b> to <b>VDDIO</b> and added separate <b>V<sub>OH</sub></b> spec for <b>OC1B</b> through <b>OC5B</b> when <b>VDDIOB</b> is 2.5V. In Table 10-9, changed <b>t<sub>DV</sub></b> max to 50ns.
06/04/07	In Table 6-6, changed which <b>AVDD_PLLx</b> and <b>AVSS_PLLx</b> goes with which <b>APLL</b> to match how the device is actually arranged.
06/15/07	In Table 1-1, added references to G.8261 and G.8262 (pre-published). In sections 7.10 and 7.12, added notes to indicate that system software must wait at least 100µs after reset is deasserted before initializing the device