KMM5402000C/CG/CM Fast Page Mode
2Mx40 DRAM SIMM, 5V

GENERAL DESCRIPTION

The Samsung KMM5402000C is a 2M bit x 40 Dynamic RAM high density memory module. The Samsung KMM5402000C consists of twenty CMOS 1Mx4bit DRAMs in 20-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5402000C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

• Performance Range:

	tRAC	tCAC	tRC
KMM5402000C - 5	50ns	15ns	90ns
KMM5402000C - 6	60ns	15ns	110ns
KMM5402000C - 7	70ns	20ns	130ns
KMM5402000C - 8	80ns	20ns	150ns

• Fast Page Mode Operation
• $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
• $\overline{RAS}$-only and Hidden refresh capability
• TTL compatible inputs and outputs
• Single +5V±10% power supply
• 1024 cycles/16 ms refresh
• JEDEC standard PDPin & pinout
• **PCB : Height (1000 mil), double sided component**

2

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ19
2	DQ0	38	DQ20
3	DQ1	39	Vss
4	DQ2	40	$\overline{CAS0}$
5	DQ3	41	NC
6	DQ4	42	NC
7	DQ5	43	$\overline{CAS1}$
8	DQ6	44	$\overline{RAS0}$
9	DQ7	45	$\overline{RAS1}$
10	Vcc	46	DQ21
11	NC	47	W
12	A0	48	Vss
13	A1	49	DQ22
14	A2	50	DQ23
15	A3	51	DQ24
16	A4	52	DQ25
17	A5	53	DQ26
18	A6	54	DQ27
19	$\overline{OE}$	55	DQ28
20	DQ8	56	DQ29
21	DQ9	57	DQ30
22	DQ10	58	DQ31
23	DQ11	59	Vcc
24	DQ12	60	DQ32
25	DQ13	61	DQ33
26	DQ14	62	DQ34
27	DQ15	63	DQ35
28	A7	64	DQ36
29	DQ16	65	DQ37
30	Vcc	66	DQ38
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	NC	70	PD4
35	DQ17	71	DQ39
36	DQ18	72	Vss

PIN NAMES

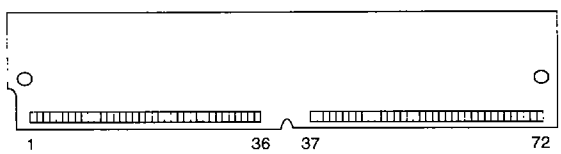
A0 - A9	Address Inputs
DQ0 - DQ39	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS0}$, $\overline{RAS1}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS1}$	Column Address Strobe
PD1 - PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
$\overline{OE}$	Output Enable

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS	70NS	80NS
PD1	NC	NC	NC	NC
PD2	NC	NC	NC	NC
PD3	Vss	NC	Vss	NC
PD4	Vss	NC	NC	Vss

*Pin Connection Changing Available

PIN CONNECTIONS (Front View)



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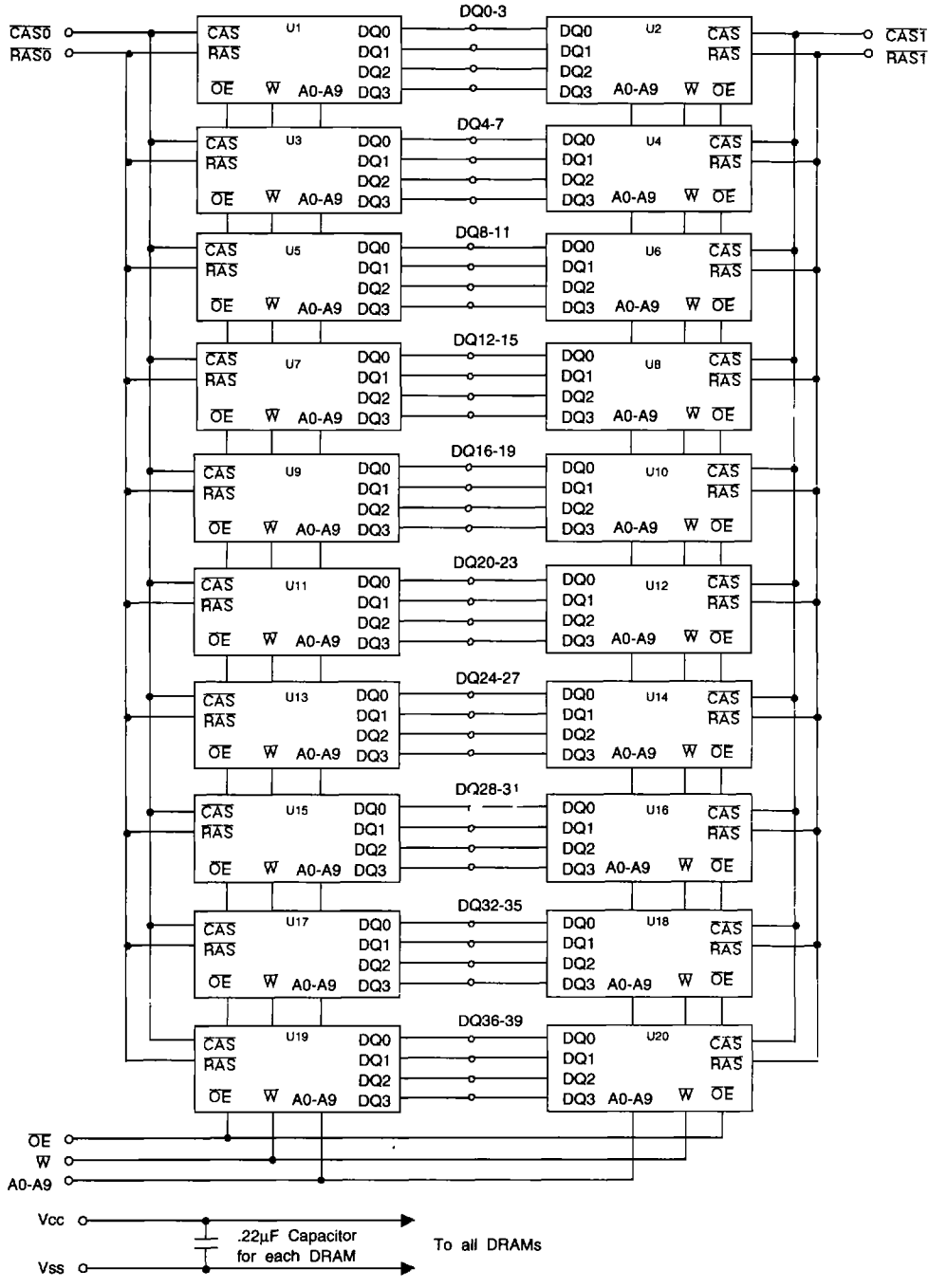
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	12	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as deteiled in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Part No	Symbol	Min	Max	Unit
Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)	KMM5402000C - 5	I_{CC1}	-	870	mA
	KMM5402000C - 6		-	770	mA
	KMM5402000C - 7		-	670	mA
	KMM5402000C - 8		-	570	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	40	mA
$\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$= V_{IH}, $\overline{RAS}$ cycling @tRC =min.)	KMM5402000C - 5	I_{CC3}	-	870	mA
	KMM5402000C - 6		-	770	mA
	KMM5402000C - 7		-	670	mA
	KMM5402000C - 8		-	570	mA
Fast Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : tPC=min.)	KMM5402000C - 5	I_{CC4}	-	670	mA
	KMM5402000C - 6		-	570	mA
	KMM5402000C - 7		-	470	mA
	KMM5402000C - 8		-	370	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)		I_{CC5}	-	20	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC =min.)	KMM5402000C - 5	I_{CC6}	-	870	mA
	KMM5402000C - 6		-	770	mA
	KMM5402000C - 7		-	670	mA
	KMM5402000C - 8		-	570	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ Vcc+0.5V, all other pins not under test = 0 V.)		$I_{I(L)}$	-200	200	µA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)		$I_{O(L)}$	-20	20	µA
Output High Voltage Level (I_{OH} = - 5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	-	0.4	V

* NOTE : ICC1,ICC3,ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum two times while $\overline{RAS}$=VIL. In ICC4, address can be changed maximum once within one page mode cycle .

CAPACITANCE (Ta = 25 °C, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A9]	C_{IN1}	-	130	pF
Input capacitance [$\overline{W}$, $\overline{OE}$]	C_{IN2}	-	150	pF
Input capacitance [$\overline{RAS0}$, $\overline{RAS1}$]	C_{IN3}	-	80	pF
Input capacitance [$\overline{CAS0}$, $\overline{CAS1}$]	C_{IN4}	-	80	pF
Input/Output capacitance [DQ0-39]	C_{DQ1}	-	29	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%. See notes 1,2.)

STANDARD OPERATION	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		15		15		15		ns	
Column address hold referenced to $\overline{RAS}$	tAR	40		50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		15		15		15		ns	10
Data-in hold referenced to $\overline{RAS}$	tDHR	40		50		55		60		ns	6
Refresh period	tREF		16		16		16		16	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		100		110		ns	
Column address to $\overline{W}$ delay time	tAWD	50		55		65		70		ns	
$\overline{CAS}$ setup time (C-B-R refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		5		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	tWRH	10		10		10		10		ns	
$\overline{CAS}$ precharge(C-B-R counter test)	tCPT	20		20		25		30		ns	

NOTES

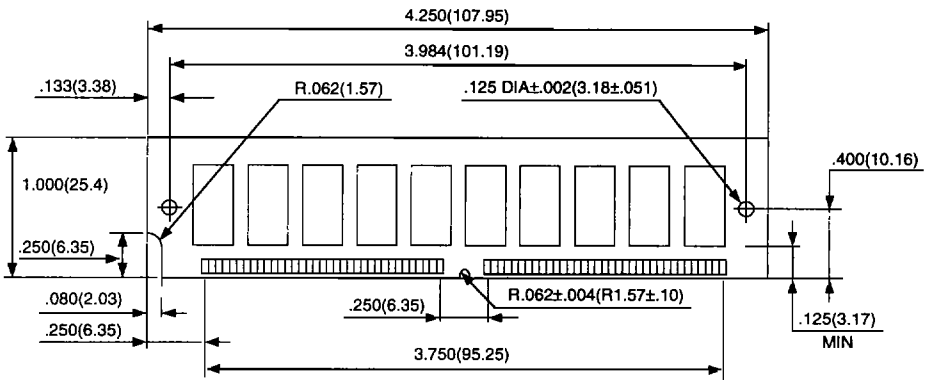
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(MAX)
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenc -ed to VOH or VOL.
8. tWCS is non restrictive operating parameter. It included in the data sheet as electrical characteristic only. If tWCS≥tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
11. Operation within the tRAD(max) limit insures that tRAC (max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.

TIMING DIAGRAM

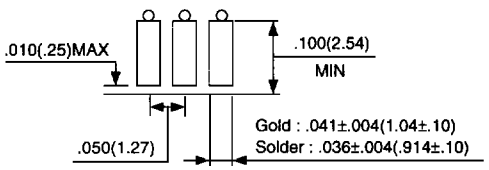
Please refer to attached timing chart (II) !!!

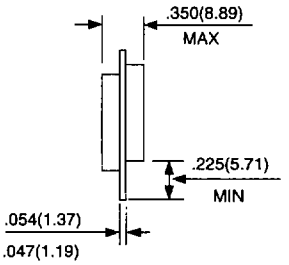
PACKAGE DIMENSIONS (Front View)

Units : Inches (millimeters)



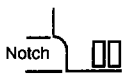
Gold & Solder Plating Lead





Tolerances : ±.005(.13) unless otherwise specified

Notch Height of KMM5401000CM : 125 MIL



NOTE : The used device is 1Mx4 DRAM , SOJ .
DRAM Part No. : KM44C1000CJ

Revision History
Rev 0.0 : 22 Dec. '93