

8-Bit Shift Register

SN54/74LS498

Features/Benefits

- 8-bit shift register for serial-to-parallel and parallel-to-serial applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading
- Expandable in 8-bit increments

Description

The 'LS498 is an 8-bit synchronous shift register with parallel load and hold capability. Two function select inputs (I0, I1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the input (D7-D0) into the output register (Q7-Q0). the HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register, Q, one bit to the left; Q0 is replaced by LIRO. RILO outputs Q7.

The SHIFT right operation shifts the output register, Q, one bit to the right; Q7 is replaced by RILO. LIRO outputs Q0.

The data output pins are enabled when \overline{OE} is LOW, and disabled (HI-Z) when \overline{OE} is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more 'LS498 8-bit shift registers may be cascaded to provide larger shift registers as shown in the application section.

Function Table

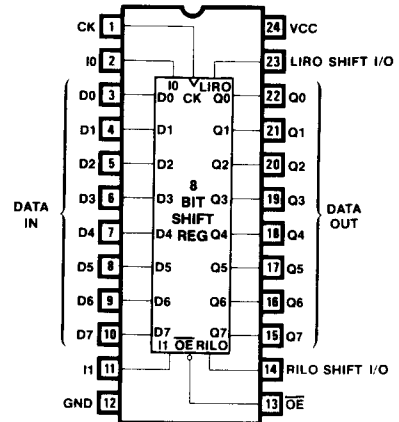
\overline{OE}	CK	I1	I0	D7-D0	Q7-Q0	OPERATION
H	*	*	*	*	Z	HI-Z*
L	↑	L	L	X	L	HOLD
L	↑	L	H	X	SR(Q)	SHIFT RIGHT
L	↑	H	L	X	SL(Q)	SHIFT LEFT
L	↑	H	H	D	D	LOAD

* When \overline{OE} is HIGH, the three-state outputs are disabled to the high-impedance state; however, sequential operation of the register is not affected.

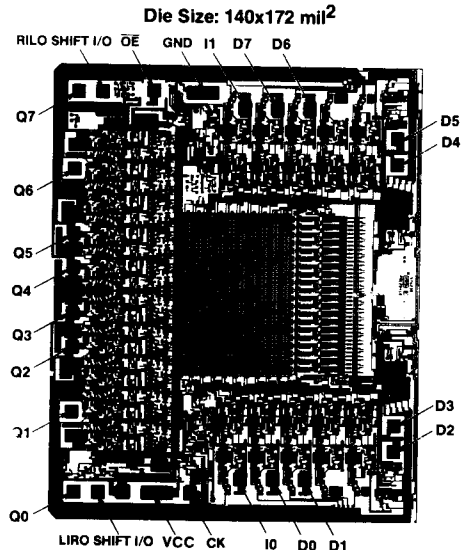
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54LS498	JS, F	28L MIL COM
SN74LS498	NS, JS	

Logic Symbol



Die Configuration



SKINNYDIP® is a registered trademark of Monolithic Memories.

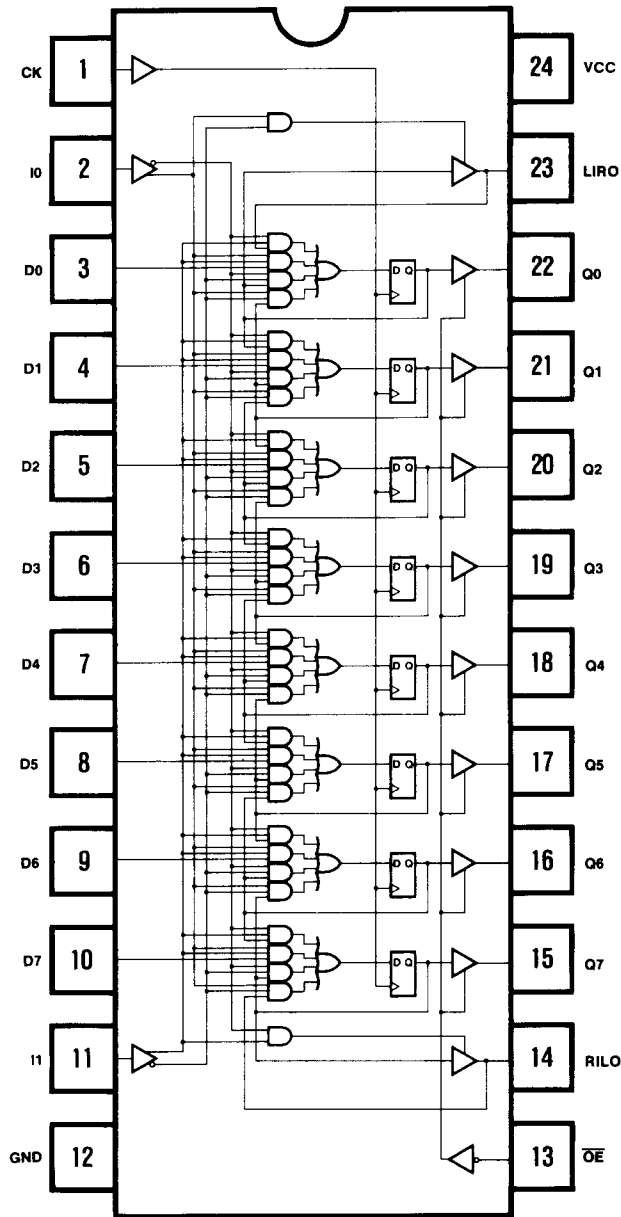
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TWX: 910-338-2376

Monolithic Memories

Logic Diagram

8-Bit Shift Register



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Absolute Maximum Ratings

Supply voltage V_{CC}	7.0 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature	-65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125*	0		75	°C
t_w	Width of clock	Low		40			35	ns
		High		30			25	
t_{su}	Setup time	60					50	ns
t_h	Hold time	0	-15		0	-15		

* Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN TYP† MAX			UNIT	
			MIN	TYP	MAX		
V_{IL}	Low-level input voltage				0.8	V	
V_{IH}	High-level input voltage		2			V	
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}$ $I_I = -18\text{mA}$			-1.5	V	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$ $V_I = 0.4\text{V}$			0.25	mA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$ $V_I = 2.4\text{V}$			25	μA	
I_I	Maximum input current	$V_{CC} = \text{MAX}$ $V_I = 5.5\text{V}$			1	mA	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$ $V_{IL} = 0.8\text{V}$ $V_{IH} = 2\text{V}$	MIL	$I_{OL} = 12\text{mA}$		0.5	V
			COM	$I_{OL} = 24\text{mA}$			
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$ $V_{IL} = 0.8\text{V}$ $V_{IH} = 2\text{V}$	MIL	$I_{OH} = -2\text{mA}$		2.4	V
			COM	$I_{OH} = -3.2\text{mA}$			
I_{OZL}	Off-state output current	$V_{CC} = \text{MAX}$ $V_{IL} = 0.8\text{V}$ $V_{IH} = 2\text{V}$	$V_O = 0.4\text{V}$		-100	μA	
I_{OZH}			$V_O = 2.4\text{V}$		100	μA	
I_{OS}	Output short-circuit current*	$V_{CC} = 5.0\text{V}$	$V_O = 0\text{V}$		-30	-130	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$			120	180	mA

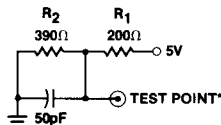
* No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

† All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum clock frequency	$C_L = 50\text{pF}$ $R_1 = 200\Omega$ $R_2 = 390\Omega$	10.5			12.5			MHz
t_{PD}	I0, I1 to LIRO, RILO			35	60		35	50	ns
t_{CLK}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to LIRO, RILO			55	95		55	80	ns
t_{PZX}	Output enable delay			35	55		35	45	ns
t_{PXZ}	Output disable delay			35	55		35	45	ns

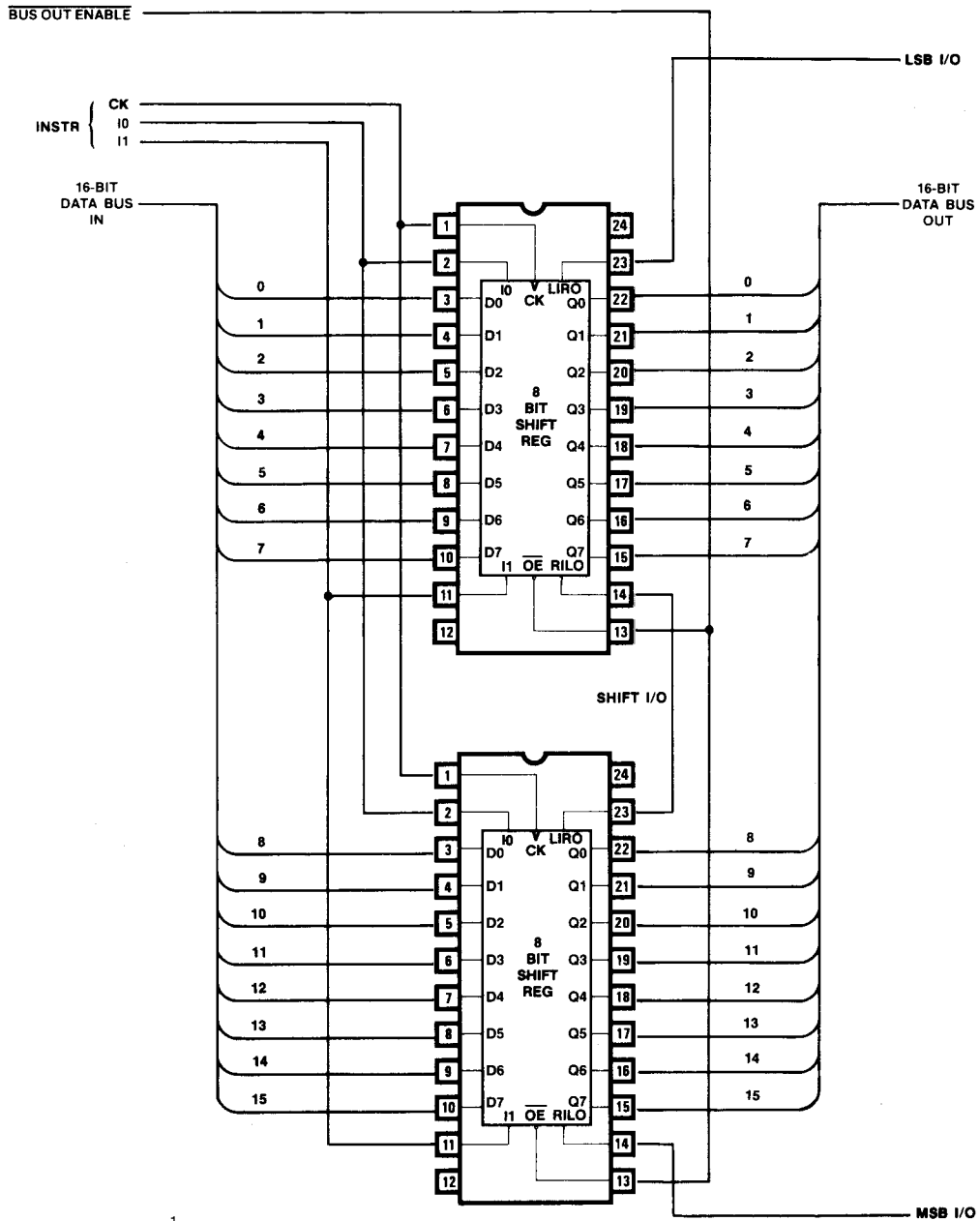
Test Load



* The "Test Point" is driven by the outputs under test, and observed by instrumentation.

Application

16-Bit Shift Register



NOTE: $t_{MAX} = \frac{1}{f_{PD CLK TO CO} + t_{SU}}$

* Assuming bit 15 is the MSB in the input stage

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