CMOS Digital Output Correlator

64-Bit, 30MHz

The TMC2023 is a monolithic 64-bit correlator with a 7-bit three-state buffered digital output. This device consists of three 64-bit independently clocked shift registers, one 64-bit reference holding latch, and a 64-bit independently clocked digital summing network. The device is capable of a 30MHz parallel correlation rate.

The 7-bit threshold register allows the user to preload a binary number from 0 to 64. Whenever the correlation is equal to or greater than the number in the threshold register, the threshold flag goes HIGH.

The 64-bit shift mask register (M register) allows the user to mask or selectively choose "no compare" bit positions enabling total word length flexibility.

The reference word is serially shifted into the B register. By clocking the R latch, the data is parallel-loaded into the R reference latch. This allows the user to serially load a new reference word into to the B register while correlation is taking place between the A register and the R latch. The two words are continually compared bit-by-bit by exclusive-OR circuits. Each exclusive-OR provides one bit to the digital summer. The output is a 7-bit word representing the sum of positions which agree at any one time between the A register and R latch. A control provides either true or inverted binary output formats.

Built with TRW's one-micron double level metal OMICRON-C™ low power CMOS process, the TMC2023 is available in a 24 pin CERDIP package and 28 contact chip carrier. The CMOS TMC2023 is pin compatible with the bipolar TDC1023.

Features

- 30MHz Correlation Rate (Worst Case Commercial)
- All Inputs And Outputs TTL Compatible
- Serial Data Input, Parallel Correlation Output
- Programmable Word Length
- Independently Clocked Registers
- Programmable Threshold Detection And Flag Output
- Available In 24 Pin CERDIP And 28 Contact Chip Carrier
- Available To Standard Military Drawing (SMD)
- Pin Compatible With TDC1023
- Output Format Flexibility
- Three-State Outputs
- Low Power CMOS

Applications

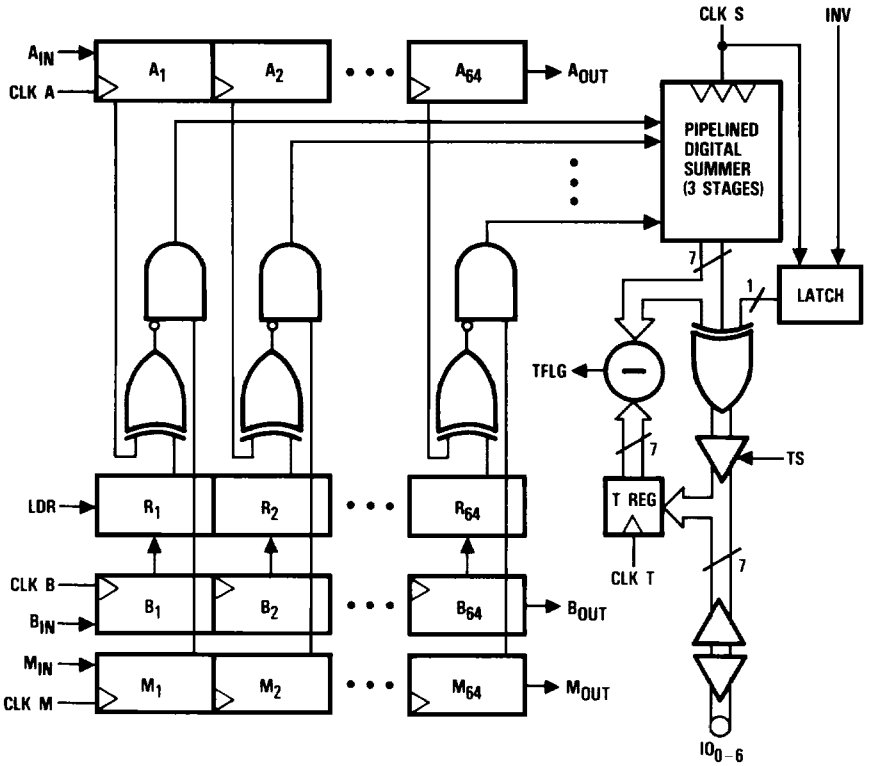
- Check Sorting Equipment
- High Density Recording
- Bar Code Identification
- Radar Signature Recognition
- Video Frame Synchronization
- Electro-Optical Navigation
- Pattern And Character Recognition
- Cross-Correlation Control Systems
- Error Correction Coding
- Asynchronous Communication
- Matched Filtering

TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

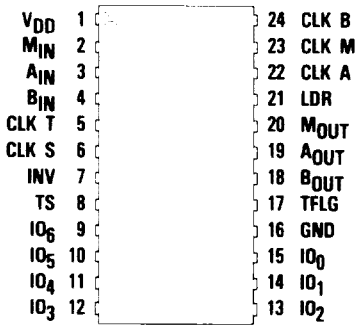
Phone: (619) 457-1000
FAX: (619) 455-6314

40G05746 Rev. C–11/90
Printed in the U.S.A.

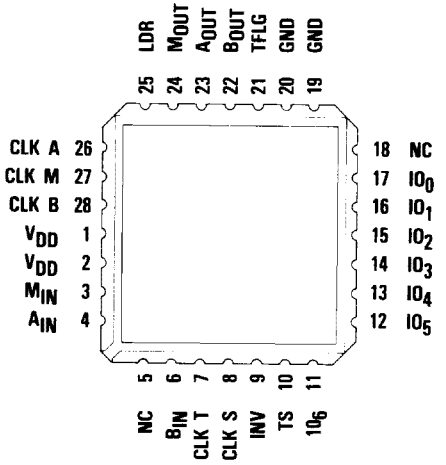
Functional Block Diagram



Pin Assigments



24 Pin CERDIP – B2, B7 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TMC2023 consists of an input section and an output section. The input section contains the A, B, and M registers, an R latch, XOR/AND logic and a pipelined summer network. The output section consists of threshold, inversion and three-state logic.

Signal Definitions

Power

V_{DD}, GND — The TMC2023 operates from a single +5V supply. All V_{DD} and GND pins must be connected.

Control

INV — Control that inverts the 7-bit digital output. When a HIGH level is applied to this pin, the outputs IO_{0-6} are logically inverted. See the *Timing Diagrams* for setup and hold requirements.

TS — The three-state control enables and disables the output buffers. A HIGH level applied to this pin forces outputs into the high-impedance state. This control also allows loading of the internal threshold register.

LDR — Control that allows parallel data to be loaded from the B register into the reference latch for correlation. If LDR is held HIGH, the R latch is transparent.

Clocks

CLK A, CLK M, CLK B — Input clocks. Clock input pins for the A, M, and B registers, respectively. Each register may be independently clocked.

CLK T — Threshold register clock. Clock input used to load the T register.

CLK S — Digital summer clock. Clock input that allows independent clocking of the pipelined summer network.

Data Inputs

M_{IN} — Mask Register Input. Allows the user to choose "no-compare" bit positions. A "0" in any bit location will result in a no-compare state for that location (bit position masked).

A_{IN}, B_{IN} — Shift register inputs to the A and B 64-bit serial registers.

Data Outputs

IO_{0-6} — Bi-directional data pins. When Outputs are enabled (TS LOW), data is a 7-bit binary representation of the correlation between the unmasked portions of the R latch and the A register. IO_6 is the MSB. These pins also serve as parallel inputs to load the threshold register. Data present one setup time before CLK T goes HIGH will be latched into the threshold register.

TFLG — The TFLG output goes HIGH whenever the correlation score is equal to or greater than the number loaded into the T register (0 to 64).

B_{OUT}, A_{OUT}, M_{OUT} — Shift register outputs of the three 64-bit shisft registers: B, A, and M, respectively. These outputs may be used to cascade multiple devices.

No Connect

NC — These pins are not functional and should be left unconnected.

G

Package Interconnections

Signal Type	Signal Name	Function	B2, B7 Package Pins	C3 Package Pins
Power	GND	Ground	16	19, 20
	V_{DD}	Supply Voltage	1	1, 2
Control	INV	Invert Output	7	9
	TS	Three-State Enable	8	10
	LDR	Load Reference	21	25
Clocks	CLK A	A Register Clock	22	26
	CLK M	M Register Clock	23	27
	CLK B	B Register Clock	24	28
	CLK T	Threshold Register Clock	5	7
	CLK S	Digital Summer Clock	6	8
Data Inputs	M_{IN}	Mask Register Input	2	3
	A_{IN}	Shift Register Input	3	4
	B_{IN}	Shift Register Input	4	6
Data Outputs	IO_{6-0}	Correlation Score	9, 10, 11, 12, 13, 14, 15	11, 12, 13, 14, 15, 16, 17
	TFLG	Threshold Flag	17	21
	B_{OUT}	Shift Register B	18	22
	A_{OUT}	Shift Register A	19	23
	M_{OUT}	Shift Register M	20	24
No Connects	NC	No Connect	None	5, 18

Timing Diagrams

Continuous Correlation

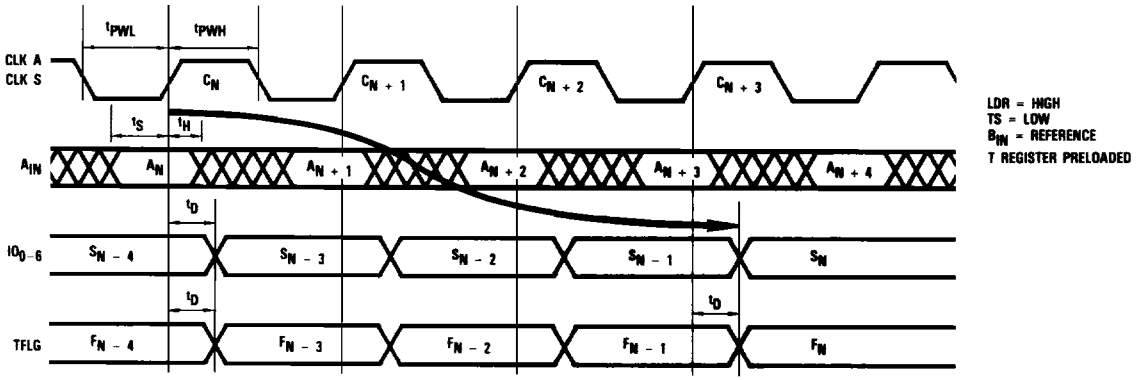
The TMC2023 contains three 1 x 64 serial shift registers (A, B, and M). The operation of these registers is identical and each has its own input, output, and clock. As shown in the timing diagram (*Figure 1*), valid data is loaded into register A (B, M) on the rising edge of CLK A (CLK B, CLK M). Data is valid if present at the input for a setup time of at least t_S before and a hold time of t_H after the rising clock edge.

The summing process is initiated when the comparison result between the A register and R latch is clocked into the summing network by a rising edge of CLK S. Typically, CLK A and CLK S are tied together so that a new correlation score is computed for each new alignment of the A register and R latch. When LDR goes HIGH, the contents of register B are copied into the R latch. With LDR LOW, a new template may be entered serially into register B, while parallel correlation takes place between register A and the R latch. In the case of continuous correlation, LDR is held HIGH so that the R latch contents continuously track those of the B register.

The summing network consists of three pipelined stages. Therefore, the total correlation score for a given set of A and B register contents appears at the summer output three CLK S cycles later. Data on the output pins IO_{0-6} is available after an additional propagation delay, denoted t_D on the timing diagram (*Figure 1*).

The correlation result is compared with the contents of the threshold register. TFLG goes HIGH if the correlation equals or exceeds the threshold value. TFLG is valid after a delay of t_D (ns) from the third CLK S rising edge.

Figure 1. Continuous Correlation

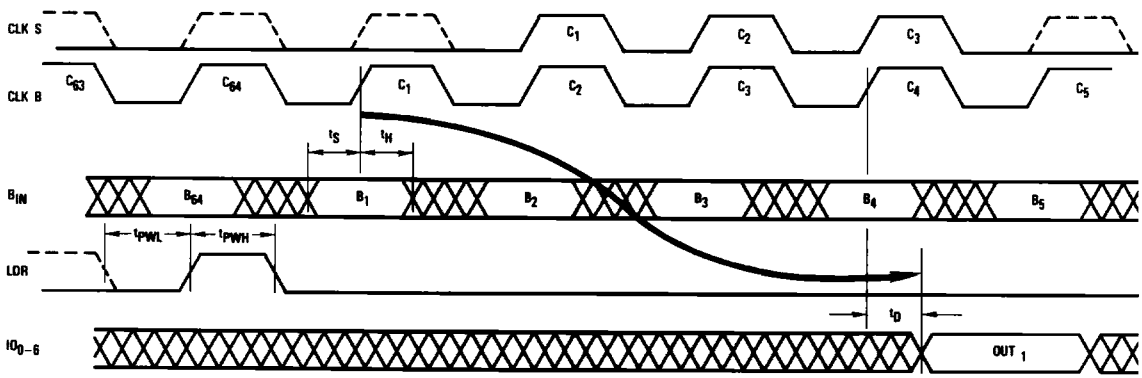


Cross Correlation

When LDR goes HIGH, the B register contents are copied into the reference latch (R latch). This useful feature allows correlation to take place between data in the R latch and the A register while a new reference is being serially clocked into the B register. If the new reference is n bits long, it requires n rising edges of CLK to load this data into the B register. For the timing diagram (see ***Figure 2***), n=64. LDR is set HIGH during the final (n^{th}) CLK B cycle, so that the new reference word is copied into the R latch. The minimum LOW and HIGH level pulse widths for LDR are shown as t_{PWL} (ns) and t_{PWH} (ns), respectively.

After the new reference is loaded, the data to be correlated is clocked through the A register. Typically, CLK A and CLK S can be tied together. This allows a new correlation score to be computed for each shift of the A register data relative to the fixed reference word in the R latch. The digital summer is internally partitioned into three pipelined stages. Therefore, a correlation score for a particular alignment of the A register data and the R latch reference appears at the summer output three CLK S cycles later. After an additional output delay of t_D (ns), the correlation data is valid at the output pins (IO_{0-6}). If this correlation result is equal to or exceeds the value in the threshold register, then TFLG goes HIGH. TFLG is valid t_D (ns) after the third rising edge of CLK S.

Figure 2. Cross-Correlation



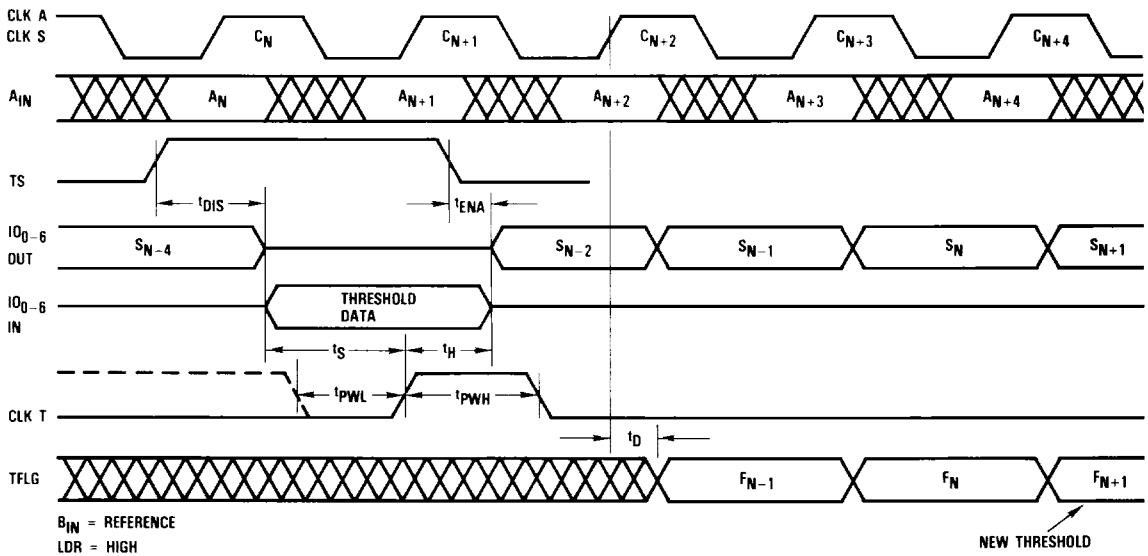
Threshold Register Load

The timing sequence for loading the threshold (T) register is shown in *Figure 3*. The T register holds the 7-bit threshold value to be compared with each correlation result. The rising edge of CLK T loads the data present on the IO_{0-6} pins into the T register. T flag logic is pipelined 3 stages, with the summer. The new value loaded into the threshold register will affect the TFLG on the third CLK S (plus an output delay t_D) following the T register load.

The output buffers must be in a high-impedance state (disabled) when the T register is programmed from an external source. After a delay of t_{DIS} (ns) from the time TS goes HIGH, the output buffers are disabled. The data pins IO_{0-6} may then be driven externally with the new threshold data. The data must be present for a setup time of t_S (ns) before and t_H (ns) after the rising edge of CLK T for correct operation. The minimum LOW and HIGH level pulse widths for CLK T are shown below as t_{PWL} (ns) and t_{PWH} (ns), respectively.

After TS is set LOW, there is an enable delay of t_{ENA} (ns) before the internal correlation data is available at pins IO_{0-6}.

Figure 3. Threshold Register Load



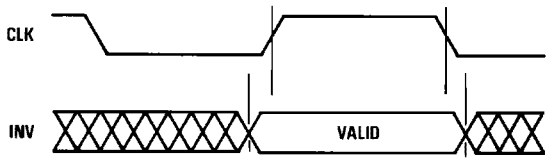
Invert Control Timing

Most applications will hardwire the INVert control HIGH or LOW depending on system requirements. In the few situations in which the control is used dynamically, the user must observe special timing constraints.

Because INVERT governs logic located between the master and slave latches of the data output register, its setup and hold requirements differ from those of the data and other controls. The device will respond to changes on INV whenever CLOCK is HIGH and will ignore it when CLOCK is LOW. To minimize the data output delay and to avoid inducing errors, the user should observe the following timing constraints:

1) Set INVERT to the desired state for the next output on or before the rising edge of CLOCK (*Figure 4*). If INVERT is asserted a few nano-seconds after the rising edge, the data output may be correspondingly delayed.
2) More importantly, keep INVERT in the desired state until after the falling edge of CLOCK, to avoid corrupting the output data. If INVERT is changed several nanoseconds before the falling edge of CLOCK, the data will likewise change. If it is changed just before the falling edge, an indeterminate output may result.

Figure 4. Invert Control Timing



Mask Register

In addition to the A and B shift references, the TMC2023 has another independently clocked register: the M, or mask register. The M register functions identically to the A and B register, except that its parallel outputs are ANDed with the exclusive-ORed outputs from the A register and R latch.

Many uses of the TMC2023 digital correlator require disabling the correlation between certain bit positions (A_i and R_i) of input words A and R. While correlation data is being clocked into the A and/or B register, a mask word may be entered into the M register. Where no comparison is to be made, zeroes are entered in those M register positions. The exclusive-OR result between each bit position is ANDed with a bit from the M register. Thus, if a particular mask bit (M_i) is zero, the output correlation between A and B for that bit position will be disabled. Consequently, a zero correlation is presented to the digital summer for each masked bit position.

The Mask register is useful for changing correlation word length and location within the registers. Where a word is undefined or no correlation is to take place, the M register should contain zeroes.

The M register is useful for building logic functions. Note that for each bit A_i and R_i, the correlation logic is:

$$A_i + R_i \qquad A_i\overline{R}_i + \overline{A}_iR_i \ (A_i \text{ exclusive-OR } R_i)$$

This result is complemented at the input of the AND gates and ANDed with the mask bit (M_i) resulting in:

$$\overline{[A_i\,\overline{R}_i + \overline{A}_iR_i]} \cdot M_i$$

The last step, performed in the digital summer, is to sum the above result over all bit positions simultaneously for a correlation at time K:

$$C(K) = \sum_{i=1}^{n} \overline{[A_i\overline{R}_i + \overline{A}_iR_i]} \cdot M_i$$

where:

i = 1, 2, 3...
n = correlation word length

Figure 5. Equivalent Input Circuit

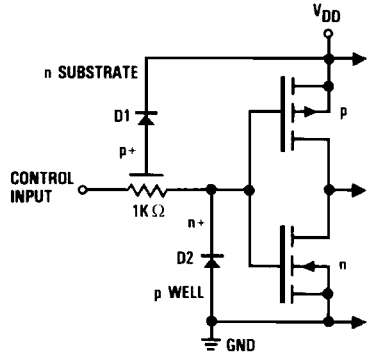


Figure 6. Equivalent Output Circuit

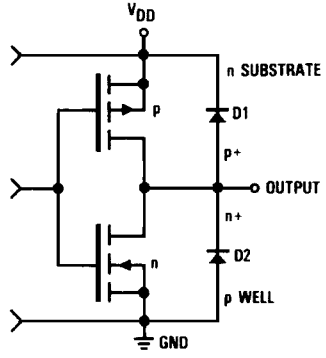
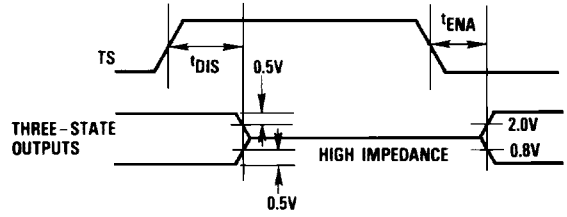


Figure 7. Threshold Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD}+0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD}+0.5)V
Forced current [3,4]	−3.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard −1 Min	Standard −1 Nom	Standard −1 Max	Standard Min	Standard Nom	Standard Max	Extended −1 Min	Extended −1 Nom	Extended −1 Max	Extended Min	Extended Nom	Extended Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.5	5.0	5.5	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW CLK A, B, M, S, T, LDR	12			15			14			15			ns
t_{PWH}	Clock Pulse Width, HIGH CLK A, B, M, S, T, LDR	12			15			14			15			ns
t_S	Data Input Setup Time	8			12			10			14			ns
t_H	Data Input Hold Time	0			0			0			0			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			2.0			2.0			V
V_{IHC}	Input Voltage, Logic HIGH A, B, M, S CLKs	2.0			2.0			2.4			2.4			V
I_{OL}	Output Current, Logic LOW			4.0			4.0			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70	0		70							°C
T_C	Case Temperature							−55		125	−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, TS = 5V		5		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 30MHz, TS = 5V		30		35	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10		−10		μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+10		+10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW [2]	V_{DD} = Max, V_{IN} = 0V [1]	−40		−40		μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH [2]	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−100		−100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Due to the IO_{0-6} and T register interconnections, these values are the I_{IH} and I_{IL} of the T register.

Switching characteristics within specified operating conditions [1]

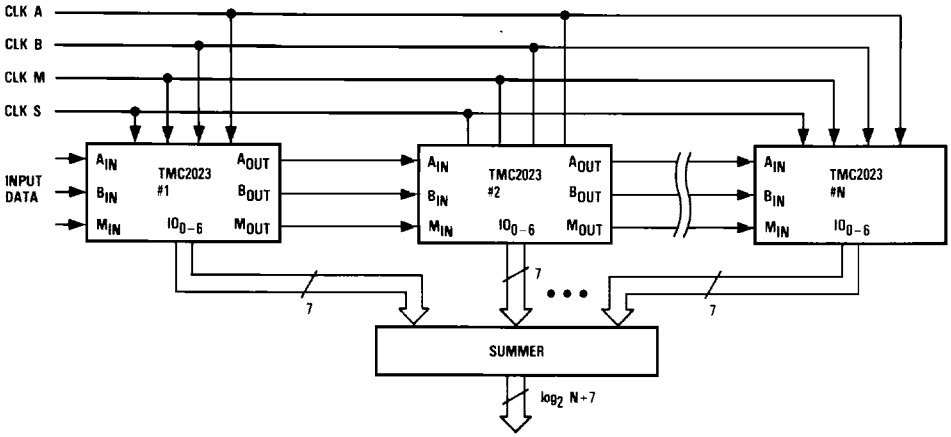
Parameter		Test Conditions	Temperature Range								Units
			Standard				Extended				
			−1				−1				
			Min	Max	Min	Max	Min	Max	Min	Max	
F_{SH}	Shift-In Clock Rate	V_{DD} = Min	30		25		30		25		MHz
F_C	Correlation Rate	V_{DD} = Min [2]	30		25		30		25		MHz
t_D	Digital Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		20		24		23		25	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF		16		20		20		25	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		16		20		18		24	ns

Notes:
1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 7.
2. Synchronous clocking: CLK A = CLK B = CLK M = CLK S.

Application Notes

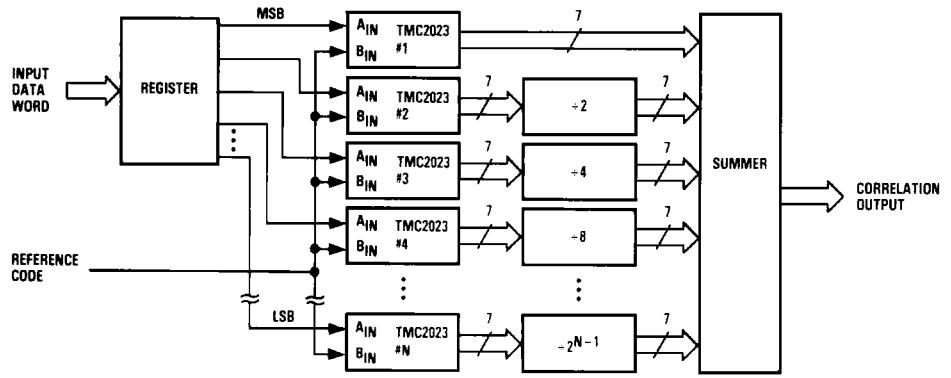
The TMC2023 can be cascaded to implement correlations of more than 64 bits. Typically, all clocks are tied together and the A, B, and M outputs of preceding stages are connected to the respective inputs of subsequent stages. An external summer is required to generate the composite correlation score. Use of the T register and TFLG require additional hardware for this configuration.

Figure 8. Cascading for Extended-Length Correlation



When comparing a multi-bit word to a single-bit reference, the outputs from the individual correlators must be appropriately weighted. This weighting reflects the relative importance of the different bit positions. Normally simple shifts (division by 2, 4, 8,...) provide the required weighting.

Figure 9. Multi-Bit x 1-Bit Correlation

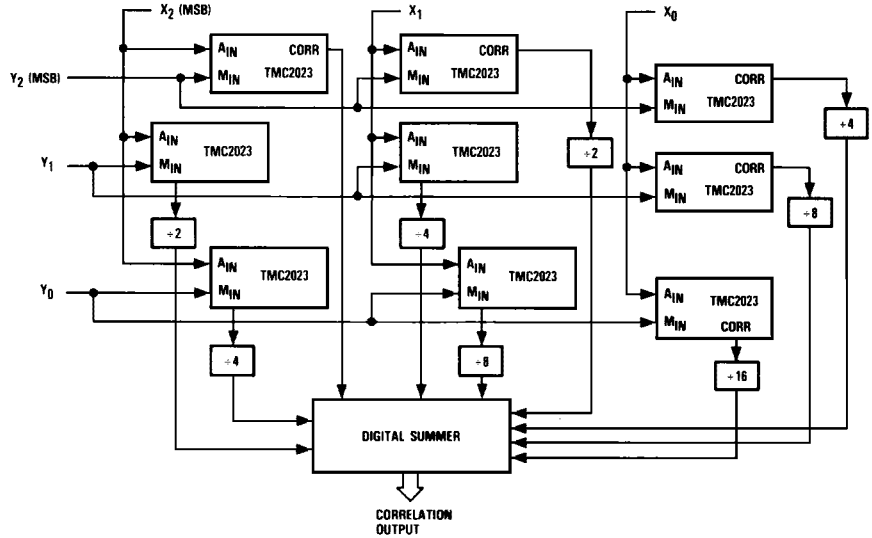


The correlation of two multi-bit words requires evaluating the term:

$$R(M) = \sum_{n=1}^{N} h(n) \cdot (M+n)$$

An example of two 3-bit words is shown in *Figure 10.*

Figure 10. Multi-Bit Correlation



Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

SMD	Nearest Equiv. TRW Product	Speed	Package
5962-89711-01JA	TMC2023B7V	25MHz	24 Pin CERDIP 0.6" Wide
5962-89711-02JA	TMC2023B7V1	30MHz	24 Pin CERDIP 0.6" Wide
5962-89711-01LA	TMC2023B2V	25MHz	24 Pin CERDIP 0.3" Wide
5962-89711-02LA	TMC2023B2V1	30MHz	24 Pin CERDIP 0.3" Wide
5962-89711-013A	TMC2023C3V	25MHz	28 Contact Chip Carrier
5962-89711-023A	TMC2023C3V1	30MHz	28 Contact Chip Carrier

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2023B2C	STD–T_A=0°C to 70°C	Commercial, 25MHz	24 Pin CERDIP	2023B2C
TMC2023B2V	EXT–T_C=–55°C to 125°C	MIL-STD-883, 25MHz	24 Pin CERDIP	2023B2V
TMC2023B2C1	STD–T_A=0°C to 70°C	Commercial, 30MHz	24 Pin CERDIP	2023B2C1
TMC2023B2V1	EXT–T_C=–55°C to 125°C	MIL-STD-883, 30MHz	24 Pin CERDIP	2023B2V1
TMC2023B7C	STD–T_A=0°C to 70°C	Commercial, 25MHz	24 Pin CERDIP	2023B7C
TMC2023B7V	EXT–T_C=–55°C to 125°C	MIL-STD-883, 25MHz	24 Pin CERDIP	2023B7V
TMC2023B7C1	STD–T_A=0°C to 70°C	Commercial, 30MHz	24 Pin CERDIP	2023B7C1
TMC2023B7V1	EXT–T_C=–55°C to 125°C	MIL-STD-883, 30MHz	24 Pin CERDIP	2023B7V1
TMC2023C3V	EXT–T_C=–55°C to 125°C	MIL-STD-883, 25MHz	28 Contact Hermetic Ceramic Chip Carrier	2023C3V
TMC2023C3V1	EXT–T_C=–55°C to 125°C	MIL-STD-883, 30MHz	28 Contact Hermetic Ceramic Chip Carrier	2023C3V1