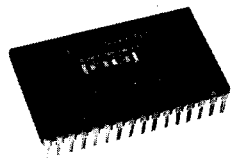
BURR-BROWN®



ADC84
ADC85H
ADC87H

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- INDUSTRY STANDARD 12-BIT A/D CONVERTERS
- COMPLETE WITH CLOCK AND INPUT BUFFER
- HIGH SPEED CONVERSION: 10μs (max)
- REDUCED CHIP COUNT—HIGH RELIABILITY
- LOWER POWER DISSIPATION: 450mW (typ)
- ±0.012% MAX LINEARITY
- THREE TEMPERATURE RANGES:
  0°C to +70°C
  −25°C to +85°C
  −55°C to +125°C
- NO MISSING CODES OVER FULL TEMPERATURE RANGE
- PARALLEL AND SERIAL OUTPUTS
- ±12V or ±15V POWER SUPPLY OPERATION
- HERMETIC 32-PIN CERAMIC SIDE-BRAZED DIP

DESCRIPTION

The ADC85H Series of analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a 32-pin hermetic side-brazed package.

Complete with internal reference and input buffer amplifier, they offer versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast 10μs conversion speed for 12-bit resolution makes these ADCs excellent for a wide range of applications where system throughput sampling rates of 100kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are CMOS/TTL-compatible. Power supply voltages are ±12VDC or ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-714A

SPECIFICATIONS

ELECTRICAL

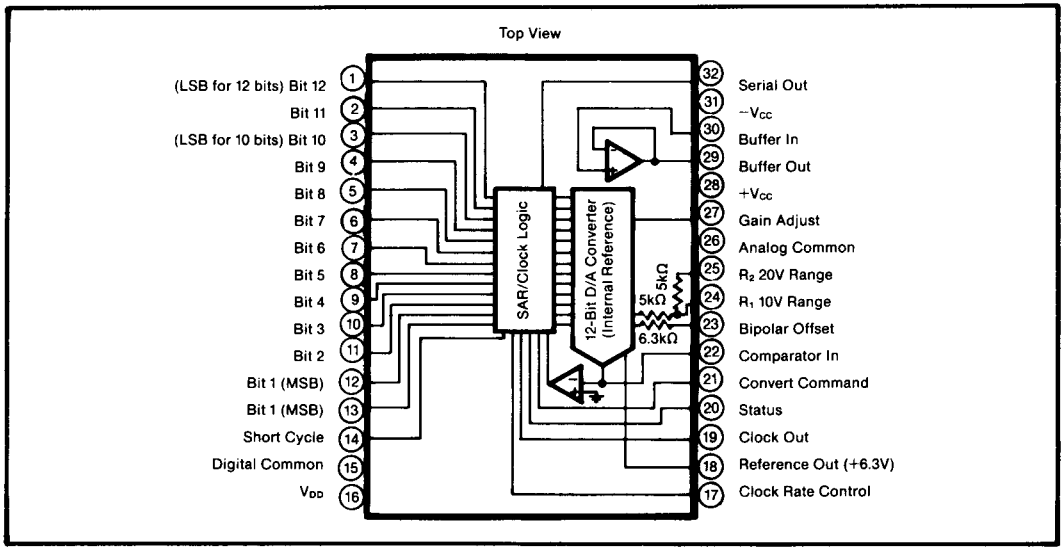
Specified at +25°C and rated supplies unless otherwise noted.

MODEL	ADC84KG-12[1]			ADC85H-12			ADC87H-12			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			*			*	Bits
INPUTS										
ANALOG										
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*			*		V
Unipolar		0 to +5, 0 to +10			*			*		V
Impedance (Direct Input): 0 to +5V, ±2.5V	2.45	2.5	2.55	*	*	*	*	*	*	kΩ
0 to +10V, ±5V	4.9	5	5.1	*	*	*	*	*	*	kΩ
±10V	9.8	10	10.2	*	*	*	*	*	*	kΩ
Buffer Amplifier: Impedance	100			*			*			MΩ
Bias Current		50			*			*		nA
Settling Time to 0.01% for 20V step[2]		2			*			*		µs
DIGITAL[3]										
Convert Command		Positive pulse 50ns (min), trailing edge initiates conversion								
Logic Loading		1			*			*		TTL Load
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error[4]		±0.1	±0.25		*	*		*	*	%
Offset Error[4]: Unipolar		±0.05	±0.2		*	*		*	*	% of FSR[5]
Bipolar		±0.1	±0.25		*	*		*	*	% of FSR
Linearity Error[6]			±0.012			*			*	% of FSR
Inherent Quantization Error		±0.5			*			*		LSB
Differential Linearity Error		±0.5			*			*		LSB
No Missing Codes Temperature Range	0		+70	−25		+85	−55		+125	°C
POWER SUPPLY SENSITIVITY										
Gain and Offset: ±15V		±0.004			*			*		% of FSR/%V_S
+5V		±0.001			*			*		% of FSR/%V_S
DRIFT										
Gain			±30			±15			±15	ppm/°C
Offset: Unipolar		±3			±3				±5	ppm of FSR/°C
Bipolar			±15			±7			±10	ppm of FSR/°C
Linearity			±3			±2			±2	ppm of FSR/°C
Monotonicity		Guaranteed			*			*		
CONVERSION TIME			10			*			*	µs
DIGITAL OUTPUT[3]										
(All Codes Complementary)										
Parallel Output Codes: Unipolar		CSB			*			*		
Bipolar		COB, CTC			*			*		
Output Drive		2			*			*		TTL Loads
Serial Data Codes (NRZ)		CSB, COB			*			*		
Output Drive		2			*			*		TTL Loads
Status		Logic "1" during conversion			*			*		
Output Drive		2			*			*		TTL Loads
Internal Clock: Output Drive		2			*			*		TTL Loads
Frequency[7]		1.35			*			*		MHz
INTERNAL REFERENCE VOLTAGE										
Reference Output	+6.2	+6.3	+6.4	*	*	*	*	*	*	V
Max. External Current With No Degradation			200			*			*	µA
Tempco of Drift			±20		±5	±10		±5	±10	ppm/°C
POWER SUPPLY REQUIREMENTS										
Rated Supply Voltages		+5, ±12 or ±15			*			*		V
Supply Ranges: V_{DD}	+4.75		+5.25	*		*	*		*	V
$\pm V_{CC}$	±11.4		±16.5	*		*	*		*	V
Supply Drain: $+I_{CC}$			20			*			*	mA
$-I_{CC}$			25			*			*	mA
I_{DD}			10			*			*	mA
Total Power Dissipation		450	725		*	*		*	*	mW
TEMPERATURE RANGE										
Specification	0		+70	−25		+85	−55		+125	°C
Operating (with Derated Specs)	−25		+85	−55		+125				°C
Storage	−65		+150	*		*	*		*	°C
PACKAGE	Hermetic Ceramic			*			*			

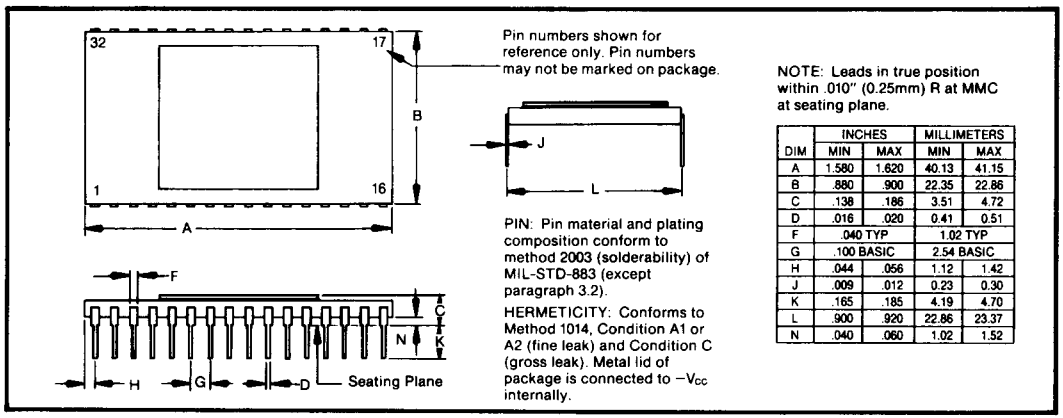
*Specification is the same as ADC84KG-12.

NOTES: (1) Model ADC84KG-10 is the same as model ADC84KG-12 except for the following: (a) Resolution: 10 bits (max), (b) Linearity Error: ±0.048% of FSR (max), (c) Conversion Time: 6μs (max), (d) Internal Clock Frequency: 1.9MHz (typ). (2) If the buffer is used, delay Convert Command until amplifier settles. (3) DTL/TTL compatible. For digital inputs Logic "0" = 0.8V (max) and Logic "1" = 2.0V min. For digital outputs Logic "0" = 0.4V (max) and Logic "1" = 2.4V (min). (4) Adjustable to zero. (5) FSR means Full Scale Range. (6) The error shown is the same as ±1/2LSB max linearity error in % of FSR. (7) Internal clock is externally adjustable.

CONNECTION DIAGRAM—ADC85H SERIES



MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.186	3.51	4.72
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.165	.185	4.19	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

ORDERING INFORMATION

Model	Resolution (Bits)	Temperature Range
ADC84KG-10	10	0°C to +70°C
ADC84KG-12	12	0°C to +70°C
ADC85H-12	12	-25°C to +85°C
ADC85HQ-12*	12	-25°C to +85°C
ADC87H-12	12	-55°C to +125°C
ADC87HQ-12*	12	-55°C to +125°C

* Environmental screening. See Table II.

ORDERING INFORMATION

BURN-IN SCREENING OPTION

See text.

Model	Burn-In Temp. (160h)(1)
ADC84KG-12-BI	+125°C
ADC85H-12-BI	+125°C
ADC87H-12-BI	+125°C

NOTE: (1) Or equivalent combination. See text.

THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC84, ADC85H and ADC87H are also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperature range. Figure 2 is the timing diagram.

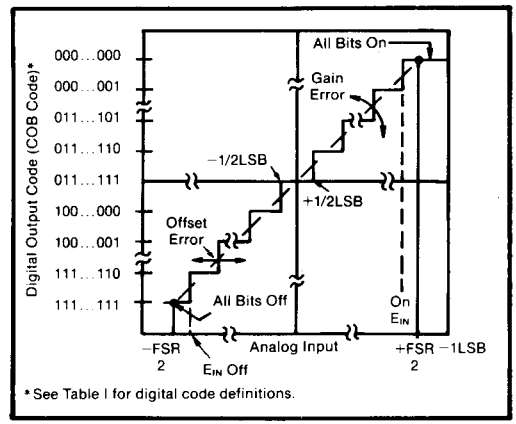
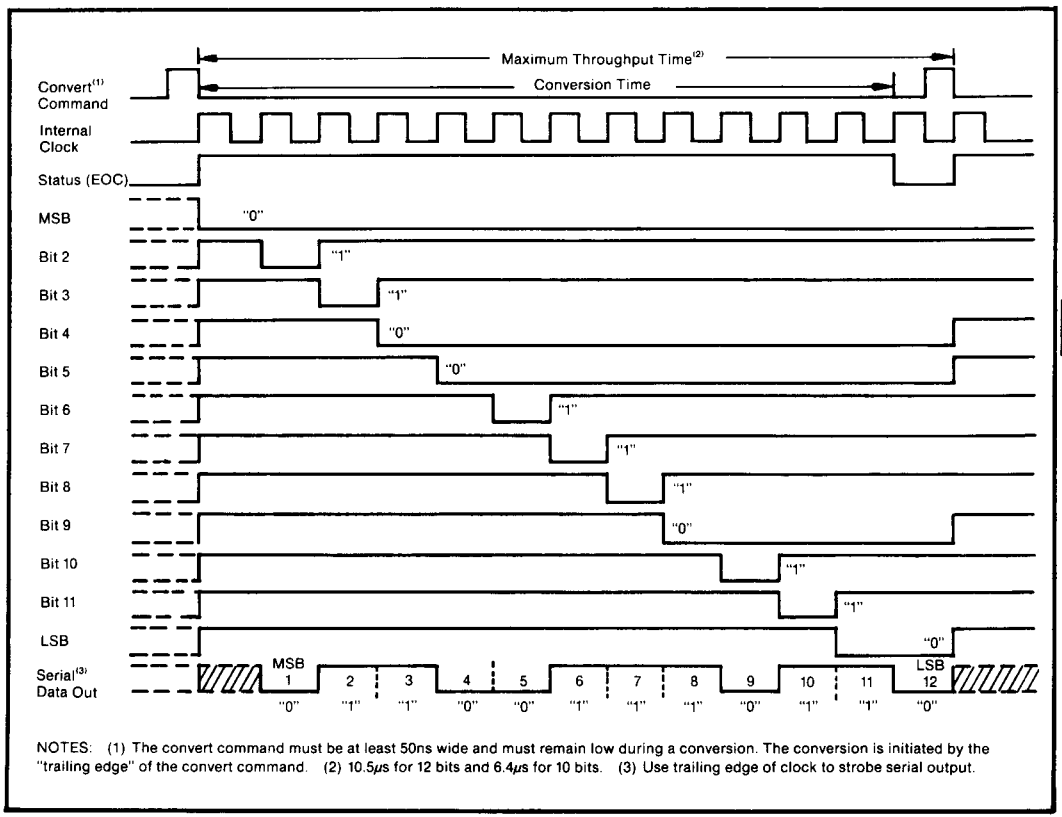


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.



NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 10.5μs for 12 bits and 6.4μs for 10 bits. (3) Use trailing edge of clock to strobe serial output.

FIGURE 2. Timing Diagram.

DIGITAL CODES

Parallel Data

Three binary codes are available on the ADC85H series parallel output:

- complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges;
- complementary two's complement (CTC) for bipolar input signal ranges;
- complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible analog input signal range for 8-, 10-, and 12-bit resolutions.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary Output	Input Voltage Range and LSB Values					
Analog Input Voltage Ranges	Defined As	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	FSR/2^n	20V/2^n	10V/2^n	5V/2^n	10V/2^n	5V/2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values						
MSB LSB						
000...000[4]	+Full Scale	+10V − 3/2LSB	+5V − 3/2LSB	+2.5V − 3/2LSB	+10V − 3/2LSB	+5V − 3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V
111...110	−Full Scale	−10V + 1/2LSB	−5V + 1/2LSB	−2.5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) CTC = Complementary Two's Complement—obtained by using the complement of the most-significant bit (MSB). MSB is available on pin 13. (3) Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table II is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.

TABLE II. Screening for ADC85HQ-12 and ADC87HQ-12.

Screen	MIL-STD-883 Method, Condition	Screening Level
Internal Visual	Burr-Brown QC4118*	
High Temperature Storage (Stabilization Bake)	1008, C	24 hour, +150°C
Temperature Cycling	1010, C	10 cycles, −65°C to +150°C
Constant Acceleration	2001, A	5000 G
Burn-in	1015, B	160 hour, +125°C steady-state
Electrical Test	Burr-Brown test procedure	
Hermeticity: Fine Leak Gross Leak	1014, A1 or A2 1014, C	5×10^{-7} atm cc/s bubble test only, preconditioning omitted
Final Electrical	Burr-Brown test procedure	
Final Drift	Burr-Brown test procedure	
External Visual	QC5150*	

* Available upon request.

DISCUSSION OF SPECIFICATIONS

The ADC85H series is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. These ADCs are factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature: gain, offset and linearity drift. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or Iσ errors as follows:

$$RSS = \sqrt{\epsilon g^2 + \epsilon o^2 + \epsilon e^2}$$

where ϵg = gain drift error (ppm /°C)
ϵo = offset drift error (ppm of FSR/°C)
ϵe = linearity error (ppm of FSR/°C)

For the ADC85H-12 operating in the unipolar mode, the total RSS drift is ±15.42ppm/°C and for bipolar operation the total RSS drift is ±16.7ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. The power supply sensitivity specification is a measure of how much the plus full-scale value will change from the initial value for independent changes in each power supply. This change results in a proportional change in all code transition values (i.e., a gain error).

The conversion speeds are specified for a maximum linearity error of ±1/2LSB with the internal clock. Faster conversion speeds are possible but at a sacrifice in linearity (see Clock Rate Control Alternate Connections).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with these ADCs. See Layout Precautions and Power Supply Decoupling.

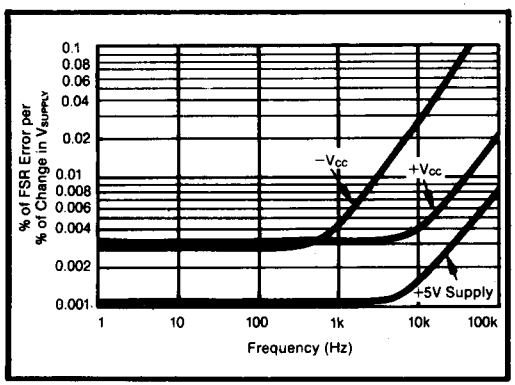


FIGURE 3. Power Supply Rejection vs Power Supply Ripple Frequency.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC85H series, but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. If these grounds must be run separately, use a wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 4 to reduce noise during operation. These capacitors should be located close to the ADC. 1μF electrolytic type capacitors should by bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

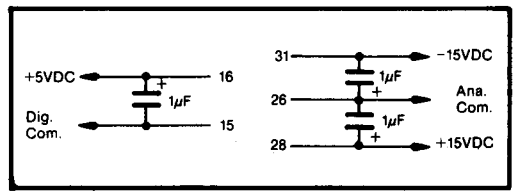


FIGURE 4. Recommended Power Supply Decoupling.

ANALOG SIGNAL SOURCE IMPEDANCE

The output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier or a sample/hold. For instance, a 741 operational amplifier will not be fast enough to accurately drive this ADC. Recommended amplifiers include the Burr-Brown models OPA602 and OPA111.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table III. See Figure 5 for circuit details.

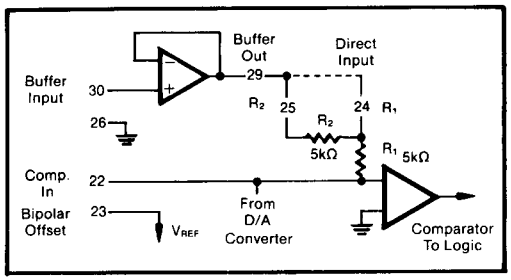


FIGURE 5. Input Scaling Circuit.

TABLE III. Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Buffered Input[1] Connect Pin 29 To Pin	For Direct Input[2] Connect Input Signal To Pin
±10V	COB or CTC	22	Input Signal[3]	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0 to +5V	CSB	26	Pin 22	24	24
0 to +10V	CSB	26	Open	24	24

NOTES: (1) Connect to pin 29 or input signal as shown in next two columns. (2) **If the buffer amplifier is not used, pin 30 must be connected to ground (pin 26).** (3) The input signal is connected to pin 30 if the buffer amplifier is used.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 27 (Gain Adjust) should be bypassed with 0.01μF to reduce noise pickup and Pin 22 (Offset Adjust) may be left open if no external adjustment is required.

Adjustment Procedure

OFFSET—Connect the Offset potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

GAIN—Connect the Gain adjust potentiometers as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition voltage to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

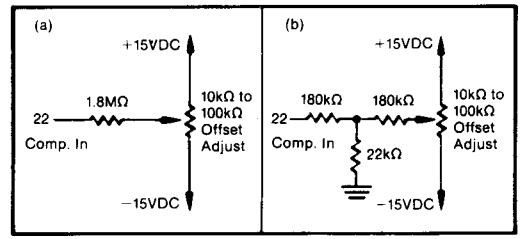


FIGURE 6. Two Methods of Connecting Optional Offset Adjust.

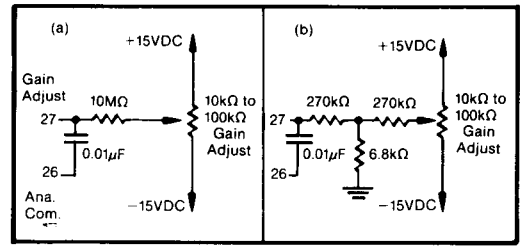


FIGURE 7. Two Methods of Connecting Optional Gain Adjust.

Clock Rate Control Alternate Connections

If adjustment of the Clock Rate is desired for faster conversion speeds, the Clock Rate Control may be connected to an external multiturn trim potentiometer with TCR of ±100ppm/°C or less as shown in Figure 8. If the potentiometer is connected to −15VDC, conversion time can be increased as shown in Figure 8. If these adjustments are used, delete the connections shown in Table IV for pin 17. See Typical Performance Curves for nonlinearity error vs. clock frequency, and Figure 9 for the effect of the control voltage on clock speed. Operation with clock rate control voltage of less than −1VDC is not recommended.

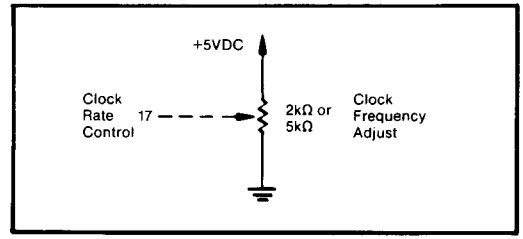


FIGURE 8. 12-Bit Clock Rate Control Optional Fine Adjust.

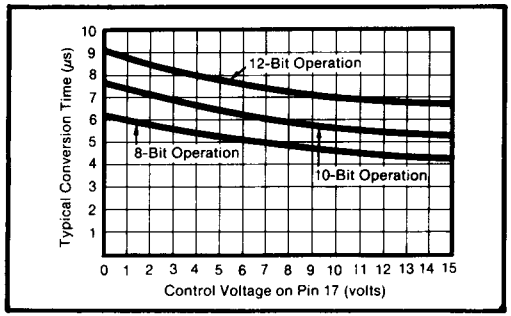


FIGURE 9. Conversion Time vs Clock Speed Control.

Additional Connections Required

The ADC85H series may be operated at faster speeds for resolutions less than 12 bits by connecting the Short Cycle input, pin 14, as shown in Table IV. Conversion speeds, linearity and resolution are shown for reference. Specifications for 10-bit units assume connections as shown below.

Converter Initialization

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

TABLE IV. Short Cycle Connections and Specifications for 8- to 12-Bit Resolution.

Resolution (Bits)	12	10	8
Connect Pin 17 to [1]	Pin 15	Pin 28	Pin 28
Connect Pin 14 to	Pin 16	Pin 2	Pin 4
Maximum Conversion Speed (μs)[2]	10	6	4.5
Maximum Nonlinearity at 25°C (% of FSR)	0.012[3]	0.048[4]	0.20[4]

NOTES: (1) Connect only if clock rate control is not used. (2) Maximum conversion speeds to maintain ±1/2LSB nonlinearity error. (3) 12-bit models only. (4) 10- or 12-bit models.

Output Drive

Normally all ADC84, ADC85H, and ADC87H logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information detail. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.