HEWLETT PACKARD

IAM-81000
MagIC™ Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amplifer Chip

Features

- **8 dB RF-IF Conversion Gain From 0.05 to 5 GHz**
- **IF Output From DC to 1 GHz with Gain**
- **Low Power Dissipation: 60 mW at V_{CC} = 5 V typ.**
- **Single Polarity Bias Supply: V_{CC} = 4 to 8 V**
- **Load-insensitive Performance**
- **Conversion Gain Flat Over Temperature**
- **Low LO Power Requirements: -5 dBm typical**
- **Low RF to IF Feedthrough, Low LO Leakage**

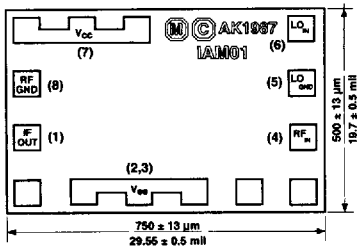
Description

The IAM-81000 is a complete low power consumption, double balanced active mixer chip. It is designed for narrow or wide bandwidth commercial, industrial, and military applications. It has RF inputs to 5 GHz and IF outputs to 1 GHz with conversion gain or above 1 GHz with conversion loss. Low frequency operation is determined by values of the external capacitors used. IAM-81000 mixers are particularly well suited for applications that require load insensitive conversion gain and good spurious signal suppression with minimum LO and bias power consumption. Typical applications include frequency down conversion, modulation, demodulation and frequency doubling, GPS satellite navigation, mobile radio, and battery powered communications receivers.

The IAM series of Gilbert multiplier based mixers is fabricated using HP's 10 GHz, f_T, 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Recommended die attach procedure is either conductive epoxy or eutectic die attach with gold preform at 400°C. Wedge or ball bonding using 0.7 mil goldwire may be used.[1]

IAM-81000 Chip Outline



Electrical specifications and associated graphs provided in this data sheet are obtained by packaging and testing IAM-81000 dice in a 180 mil package with three internal 105 pF capacitors.

Operating Frequency Range

The lower frequency limit of the IAM-81000 mixer chip at which the RF and LO ports will work is set by the AC grounding provided to these ports external to the chip. MOS capacitors are used in packaged IAM mixers to provide these grounds; package dimensions limit the values of these capacitors from 50 to 200 pF, which sets a lower frequency of operation for the RF and LO ports of approximately 50 MHz. The low frequency limit of operation for the IF is set solely by the value of the DC blocking capacitor and the lead impedance (50 Ω) at this port. Low frequency cutoff can be decreased by using high value capacitors.

Differential Use

IAM-81000 can be driven in differential mode at the RF and/or LO port. This is done by using an external balun at the port and omitting AC bypassing capacitors. To maintain DC level across the port, input blocking capacitors are used. Differential operation of either RF or LO port improves mixer LO to IF isolation.

Electrical Specifications[2,3], T_A = 25°C

Symbol	Parameters and Test Conditions:[4] V_{cc} = 5 V, V_{ee} = 0 V, Z_L = 50 Ω		Units	Min.	Typ.	Max.
G_C	Conversion Gain	RF = 2 GHz, LO = 1.75 GHz	dB		8.5	
$F_{3\,dB}RF$	RF Bandwidth (G_C 3 dB Down)	IF = 250 MHz	GHz		4.5	
$F_{3\,dB}IF$	IF Bandwidth (G_C 3 dB Down)	LO = 2 GHz	GHz		0.6	
$P_{1\,dB}$	IF Output Power at 1 dB Gain Compression	RF=2 GHz, LO =1.75 GHz	dBm		-6	
IP_3	IF Output Third Order Intercept Point	RF = 2 GHz, LO = 1.75 GHz	dBm		3	
NF	SSB Noise Figure	RF = 2 GHz, LO = 1.75 GHz	dB		15	
VSWR	RF Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	LO Port VSWR	f = 0.05 to 5 GHz			1.5:1	
	IF Port VSWR	f < 1 GHz			1.5:1	
RF_{if}	RF Feedthrough at IF Port	RF = 2 GHz, LO=1.75 GHz	dBc		-25	
LO_{if}	LO Leakage at IF Port	LO = 1.75 GHz	dBm		-25	
LO_{rf}	LO Leakage at RF Port	LO = 1.75 GHz	dBm		-35	
I_{CC}	Supply Current		mA	10	12.5	16

NOTES:
1. See Application Note, "AN-005: Transistor Chip Use" for additional information.
2. The recommended operating voltage range for this device is 4 to 8 V. Typical performance as function of voltage is on the following page.
3. Tested in a 180 mil package with three interal 150 pF capacitors.
4. RF performance of the chip is determined by packaging and testing 10 devices per wafer.

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Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	10 V
Power Dissipation[2, 3]	300 mW
RF Input Power	+14 dBm
LO Input Power	+14 dBm
Junction Temperature	200°C
Storage Temperature	-65 to 200°C

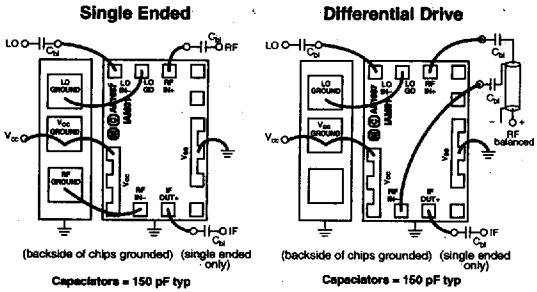
Thermal Resistance: θ_{jc} = 25°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{mounting\ surface}$ (T_{ms}) = 25°C
3. Derate at 40 mW/°C for T_{ms} > 182°C

Part Number Ordering Information

Part Number	Devices Per Tray
IAM-81000-GP2	10
IAM-81000-GP4	100
IAM-81000-GP6	up to 300

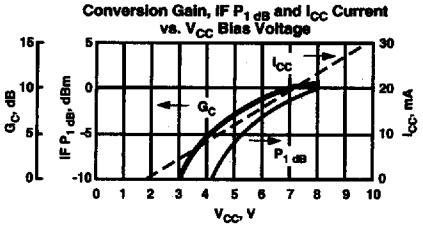
Bonding Diagrams

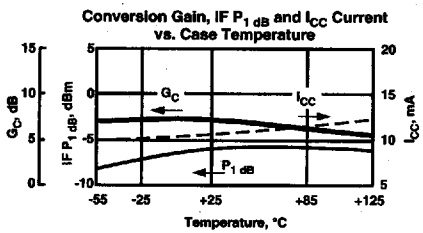


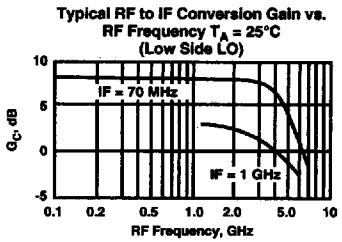
Typical Performance, T_A = 25°C, V_{CC} = 5 V

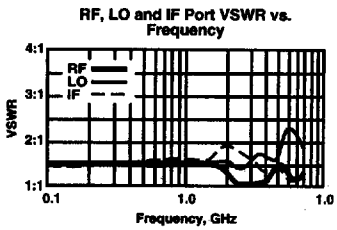
RF: -20 dBm at 2 GHz, LO: -5 dBm at 1.75 GHz

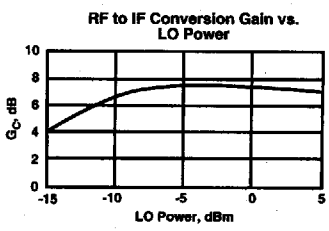
(Unless otherwise noted)

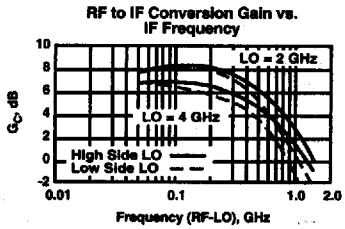


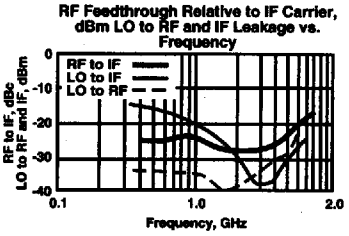












Harmonic Intermodulation Suppression (dB Below Desired Output)
RF at 1 GHz, LO at 0.752 GHz, IF at 0.248 GHz

Harmonic LO Order \ Harmonic RF Order	0	1	2	3	4	5
0	—	21	35	>75	>75	>75
1	12	0	48	48	>75	>75
2	13	41	39	71	>75	>75
3	36	28	53	57	>75	>75
4	27	49	49	72	>75	>75
5	45	35	63	62	>75	>75

Harmonic LO Order

Harmonic RF Order

Xmn = PIF-P(m*rf-n*lo)