# 8-bit, 40 Msps 2.7 to 5.5 V universal analog-to-digital converter

# TDA8790

## FEATURES

- 8-bit resolution
- Operation between 2.7 and 5.5 V
- Sampling rate up to 40 MHz
- DC sampling allowed
- High signal-to-noise ratio over a large analog input frequency range (7.3 effective bits at 4.43 MHz full-scale input at $f_{clk}$ = 40 MHz)
- CMOS/TTL compatible digital inputs and outputs
- External reference voltage regulator
- Power dissipation only 30 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- Sleep mode (4 mW)
- No sample-and-hold circuit required.

## APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Camera
- Camcorder
- Radio communication.

## GENERAL DESCRIPTION

The TDA8790 is an 8-bit universal analog-to-digital converter (ADC) for video and general purpose applications. It converts the analog input signal from 2.7 to 5.5 V into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are CMOS/TTL compatible. A sleep mode allows reduction of the device power consumption down to 4 mW.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | analog supply voltage | | 2.7 | 3.3 | 5.5 | V |
| $V_{DDD}$ | digital supply voltage | | 2.7 | 3.3 | 5.5 | V |
| $V_{DDO}$ | output stages supply voltage | | 2.5 | 3.3 | 5.5 | V |
| $\Delta V_{DD}$ | supply voltage difference | | | | | |
| | $V_{DDA} - V_{DDD}$ | | −0.2 | – | +0.2 | V |
| | $V_{DDD} - V_{DDO}$ | | −0.2 | – | +2.25 | V |
| $I_{DDA}$ | analog supply current | | – | 4 | 6 | mA |
| $I_{DDD}$ | digital supply current | | – | 5 | 8 | mA |
| $I_{DDO}$ | output stages supply current | $f_{clk}$ = 40 MHz; $C_L$ = 20 pF; ramp input | – | 1 | 2 | mA |
| INL | integral non-linearity | $f_{clk}$ = 40 MHz; ramp input | – | ±0.5 | ±0.75 | LSB |
| DNL | differential non-linearity | $f_{clk}$ = 40 MHz; ramp input | – | ±0.25 | ±0.5 | LSB |
| $f_{clk(max)}$ | maximum clock frequency | | 40 | – | – | MHz |
| $P_{tot}$ | total power dissipation | $V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V | – | 30 | 53 | mW |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA8790M | SSOP20 | plastic shrink small outline package; 20 leads; body width 4.4 mm | SOT266-1 |

## BLOCK DIAGRAM

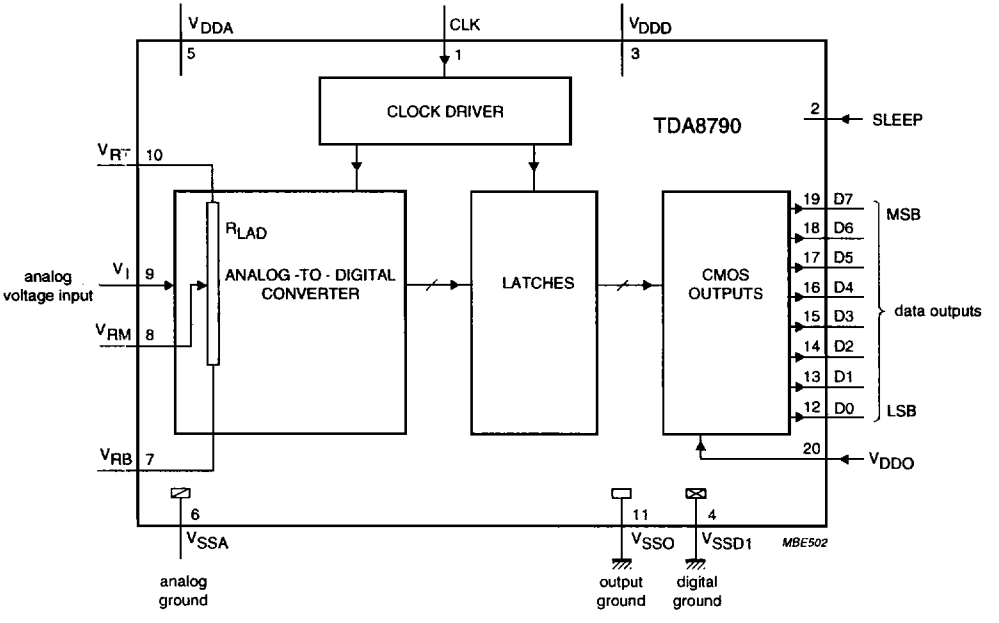



Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| CLK | 1 | clock input |
| SLEEP | 2 | sleep mode input |
| $V_{DDD}$ | 3 | digital supply voltage (2.7 to 5.5 V) |
| $V_{SSD}$ | 4 | digital ground |
| $V_{DDA}$ | 5 | analog supply voltage (2.7 to 5.5 V) |
| $V_{SSA}$ | 6 | analog ground |
| $V_{RB}$ | 7 | reference voltage BOTTOM input |
| $V_{RM}$ | 8 | reference voltage MIDDLE |
| $V_I$ | 9 | analog input voltage |
| $V_{RT}$ | 10 | reference voltage TOP input |
| $V_{SSO}$ | 11 | digital output ground |
| D0 | 12 | data output; bit 0 (LSB) |
| D1 | 13 | data output; bit 1 |
| D2 | 14 | data output; bit 2 |
| D3 | 15 | data output; bit 3 |
| D4 | 16 | data output; bit 4 |
| D5 | 17 | data output; bit 5 |
| D6 | 18 | data output; bit 6 |
| D7 | 19 | data output; bit 7 (MSB) |
| $V_{DDO}$ | 20 | positive supply voltage for output stage (2.7 to 5.5 V) |

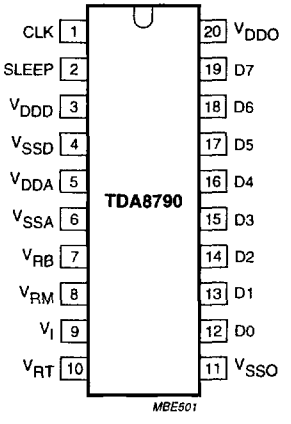



Fig.2 Pin configuration.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DDA}$ | analog supply voltage | note 1 | −0.3 | +7.0 | V |
| $V_{DDD}$ | digital supply voltage | note 1 | −0.3 | +7.0 | V |
| $V_{DDO}$ | output stages supply voltage | note 1 | −0.3 | +7.0 | V |
| $\Delta V_{DD}$ | supply voltage difference | | | | |
| | $V_{DDA} - V_{DDD}$ | | −1.0 | +4.0 | V |
| | $V_{DDA} - V_{DDO}$ | | −1.0 | +4.0 | V |
| | $V_{DDD} - V_{DDO}$ | | −1.0 | +4.0 | V |
| $V_I$ | input voltage | referenced to $V_{SSA}$ | −0.3 | +7.0 | V |
| $V_{clk(p-p)}$ | AC input voltage for switching (peak-to-peak value) | referenced to $V_{SSD}$ | − | $V_{DDD}$ | V |
| $I_O$ | output current | | − | 10 | mA |
| $T_{stg}$ | storage temperature | | −55 | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | −20 | +75 | °C |
| $T_j$ | junction temperature | | − | +150 | °C |

**Note**

1. The supply voltages $V_{DDA}$, $V_{DDD}$ and $V_{DDO}$ may have any value between −0.3 V and +7.0 V provided that the supply voltage $\Delta V_{DD}$ remains as indicated.

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient in free air | 120 | K/W |

## CHARACTERISTICS

$V_{DDA} = V_5$ to $V_6 = 3.3$ V; $V_{DDD} = V_3$ to $V_4 = 3.3$ V; $V_{DDO} = V_{20}$ to $V_{11} = 3.3$ V; $V_{SSA}$, $V_{SSD}$ and $V_{SSO}$ shorted together; $V_{i(p-p)} = 1.84$ V; $C_L = 20$ pF; $T_{amb} = 0$ to +70 °C; typical values measured at $T_{amb} = 25$ °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{DDA}$ | analog supply voltage | | 2.7 | 3.3 | 5.5 | V |
| $V_{DDD}$ | digital supply voltage | | 2.7 | 3.3 | 5.5 | V |
| $V_{DDO}$ | output stages supply voltage | | 2.5 | 3.3 | 5.5 | V |
| $\Delta V_{DD}$ | supply voltage difference | | | | | |
| | $V_{DDA} - V_{DDD}$ | | −0.2 | − | +0.2 | V |
| | $V_{DDD} - V_{DDO}$ | | −0.2 | − | +2.25 | V |
| $I_{DDA}$ | analog supply current | | − | 4 | 6 | mA |
| $I_{DDD}$ | digital supply current | | − | 5 | 8 | mA |
| $I_{DDO}$ | output stages supply current | $f_{clk}$ = 40 MHz; ramp input; $C_L$ = 20 pF | − | 1 | 2 | mA |
| **Inputs** | | | | | | |
| CLOCK INPUT CLK (REFERENCED TO $V_{SSD}$); see note 1 | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | − | $0.3V_{DDD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | $0.7V_{DDD}$ | − | $V_{DDD}$ | V |
| | | $V_{DDD} \leq 3.6$ V | $0.6V_{DDD}$ | − | $V_{DDD}$ | V |
| $I_{IL}$ | LOW level input current | $V_{clk} = 0.3V_{DDD}$ | −1 | 0 | +1 | µA |
| $I_{IH}$ | HIGH level input current | $V_{clk} = 0.7V_{DDD}$ | − | − | 5 | µA |
| $Z_I$ | input impedance | $f_{clk}$ = 40 MHz | − | 4 | − | kΩ |
| $C_I$ | input capacitance | $f_{clk}$ = 40 MHz | − | 3 | − | pF |
| INPUT SLEEP (REFERENCED TO $V_{SSD}$); see Table 2 | | | | | | |
| $V_{IL}$ | LOW level input voltage | | 0 | − | $0.3V_{DDD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | $0.7V_{DDD}$ | − | $V_{DDD}$ | V |
| | | $V_{DDD} \leq 3.6$ V | $0.6V_{DDD}$ | − | $V_{DDD}$ | V |
| $I_{IL}$ | LOW level input current | $V_{IL} = 0.3V_{DDD}$ | −1 | − | − | µA |
| $I_{IH}$ | HIGH level input current | $V_{IH} = 0.7V_{DDD}$ | − | − | +1 | µA |
| $V_I$ (ANALOG INPUT VOLTAGE REFERENCED TO $V_{SSA}$) | | | | | | |
| $I_{IL}$ | LOW level input current | $V_I = V_{RB}$ | − | 0 | − | µA |
| $I_{IH}$ | HIGH level input current | $V_I = V_{RT}$ | − | 9 | − | µA |
| $Z_I$ | input impedance | $f_i$ = 1 MHz | − | 20 | − | kΩ |
| $C_I$ | input capacitance | $f_i$ = 1 MHz | − | 2 | − | pF |
| **Reference voltages for the resistor ladder;** see Table 1 | | | | | | |
| $V_{RB}$ | reference voltage BOTTOM | | 1.1 | 1.2 | − | V |
| $V_{RT}$ | reference voltage TOP | $V_{TOP} \leq V_{DDA}$ | 2.7 | 3.3 | $V_{DDA}$ | V |
| $V_{diff}$ | differential reference voltage $V_{RT} - V_{RB}$ | | 1.5 | 2.1 | 2.7 | V |
| $I_{ref}$ | reference current | | − | 0.95 | − | mA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{LAD}$ | resistor ladder | | – | 2.2 | – | kΩ |
| $TC_{RLAD}$ | temperature coefficient of the resistor ladder | | – | 1860 | – | ppm |
| | | | – | 4092 | – | mΩ/K |
| $V_{osB}$ | offset voltage BOTTOM | note 2 | – | 170 | – | mV |
| $V_{osT}$ | offset voltage TOP | note 2 | – | 170 | – | mV |
| $V_{i(p-p)}$ | analog input voltage (peak-to-peak value) | note 3 | 1.4 | 1.76 | 2.4 | V |
| **Outputs** | | | | | | |
| DIGITAL OUTPUTS D7 TO D0 (REFERENCED TO $V_{SSD}$) | | | | | | |
| $V_{OL}$ | LOW level output voltage | $I_O$ = 1 mA | 0 | – | 0.5 | V |
| $V_{OH}$ | HIGH level output voltage | $I_O$ = −1 mA | $V_{DDO}$ − 0.5 | – | $V_{DDO}$ | V |
| $I_{OZ}$ | output current in 3-state mode | 0.4 V < $V_O$ < $V_{DDO}$ | −20 | – | +20 | µA |
| **Switching characteristics** | | | | | | |
| CLOCK INPUT CLK; see Fig.4; note 1 | | | | | | |
| $f_{clk(max)}$ | maximum clock frequency | | 40 | – | – | MHz |
| $t_{CPH}$ | clock pulse width HIGH | | 9 | – | – | ns |
| $t_{CPL}$ | clock pulse width LOW | | 9 | – | – | ns |
| **Analog signal processing** | | | | | | |
| LINEARITY | | | | | | |
| INL | integral non-linearity | $f_{clk}$ = 40 MHz; ramp input; see Fig.6 | – | ±0.5 | ±0.75 | LSB |
| DNL | differential non-linearity | $f_{clk}$ = 40 MHz; ramp input; see Fig.7 | – | ±0.25 | ±0.5 | LSB |
| BANDWIDTH ($f_{clk}$ = 40 MHz) | | | | | | |
| B | analog bandwidth | full-scale sine wave; note 4 | – | 10 | – | MHz |
| | | 75% full-scale sine wave; note 4 | – | 13 | – | MHz |
| | | 50% full-scale sine wave; note 4 | – | 20 | – | MHz |
| | | small signal at mid scale; $V_i$ = ±10 LSB at code 128; note 4 | – | 350 | – | MHz |
| INPUT SET RESPONSE ($f_{clk}$ = 40 MHz; see Fig.8; note 5) | | | | | | |
| $t_{STLH}$ | analog input settling time LOW-to-HIGH | full-scale square wave | – | 3 | 5 | ns |
| $t_{STHL}$ | analog input settling time HIGH-to-LOW | full-scale square wave | – | 3 | 5 | ns |
| HARMONICS; ($f_{clk}$ = 40 MHz; see Fig.9; note 6) | | | | | | |
| THD | total harmonic distortion | $f_i$ = 4.43 MHz | – | −50 | – | dB |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| SIGNAL-TO-NOISE RATIO; see Fig.9; note 6 | | | | | | |
| S/N | signal-to-noise ratio (full scale) | without harmonics; $f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz | – | 47 | – | dB |
| EFFECTIVE BITS; see Fig.9; note 6 | | | | | | |
| EB | effective bits | $f_{clk}$ = 40 MHz | | | | |
| | | $f_i$ = 300 kHz | – | 7.8 | – | bits |
| | | $f_i$ = 4.43 MHz | – | 7.3 | – | bits |
| DIFFERENTIAL GAIN see note 7 | | | | | | |
| $G_{diff}$ | differential gain | $f_{clk}$ = 40 MHz; PAL modulated ramp | – | 1.5 | – | % |
| DIFFERENTIAL PHASE; see note 7 | | | | | | |
| $\varphi_{diff}$ | differential phase | $f_{clk}$ = 40 MHz; PAL modulated ramp | – | 0.25 | – | deg |
| **Timing ($f_{clk}$ = 40 MHz; $C_L$ = 20 pF);** see Fig.4; note 8 | | | | | | |
| $t_{ds}$ | sampling delay time | | – | – | 5 | ns |
| $t_h$ | output hold time | | 5 | – | – | ns |
| $t_d$ | output delay time | $V_{DDO}$ = 4.75 V | 8 | 12 | 15 | ns |
| | | $V_{DDO}$ = 3.15 V | 8 | 17 | 20 | ns |
| | | $V_{DDO}$ = 2.7 V | 8 | 18 | 21 | ns |
| **3-state sleep mode delay times;** see Fig.5 | | | | | | |
| $t_{dZH}$ | enable HIGH | | – | 14 | 18 | ns |
| $t_{dZL}$ | enable LOW | | – | 16 | 20 | ns |
| $t_{dHZ}$ | disable HIGH | | – | 16 | 20 | ns |
| $t_{dLZ}$ | disable LOW | | – | 14 | 18 | ns |

**Notes**

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 0 up to and including 256:
   a) $V_{osB}$ (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM ($V_{RB}$) at $T_{amb}$ = 25 °C.
   b) $V_{osT}$ (voltage offset TOP) is the difference between $V_{RT}$ (reference voltage TOP) and the analog input which produces data outputs equal to 256 at $T_{amb}$ = 25 °C.

3. In order to ensure the optimum linearity performance of such converter architecture the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 255 respectively) are connected to pins $V_{RB}$ and $V_{RT}$ via offset resistors $R_{OB}$ and $R_{OT}$ as shown in Fig.3.

   a) The current flowing into the resistor ladder is $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter, to cover code 0 to code 255, is $V_i = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = 0.838 \times (V_{RT} - V_{RB})$

   b) Since $R_L$, $R_{OB}$ and $R_{OT}$ have similar behaviour with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from part to part. Consequently variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is then optimized.

4. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, nor any significant attenuation is observed in the reconstructed signal.
5. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
6. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8 K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
7. Measurement carried out using video analyser VM700A, where video analog signal is reconstructed through a DAC.
8. Output data acquisition: the output data is available after the maximum delay time of $t_d$.

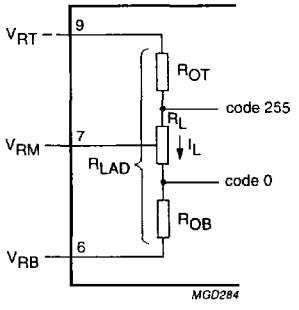



Fig.3 Explanation of note 3.

**Table 1** Output coding and input voltage (typical values; referenced to $V_{SSA}$)

| STEP | $V_{I(p-p)}$ (V) | BINARY OUTPUT BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Underflow | <1.37 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1.37 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | . | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . |
| 254 | . | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 255 | 3.13 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Overflow | >3.13 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Table 2** Sleep mode selection

| SLEEP | D7 TO D0 | $I_{DDA} + I_{DDD}$ (typ.) |
|---|---|---|
| 1 | high impedance | 1.2 mA |
| 0 | active | 9 mA |

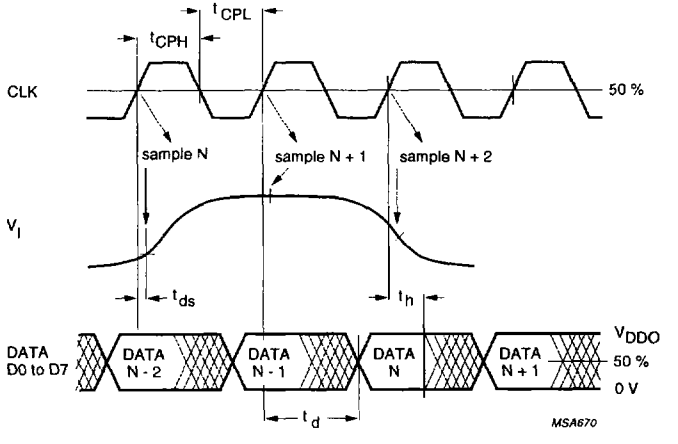
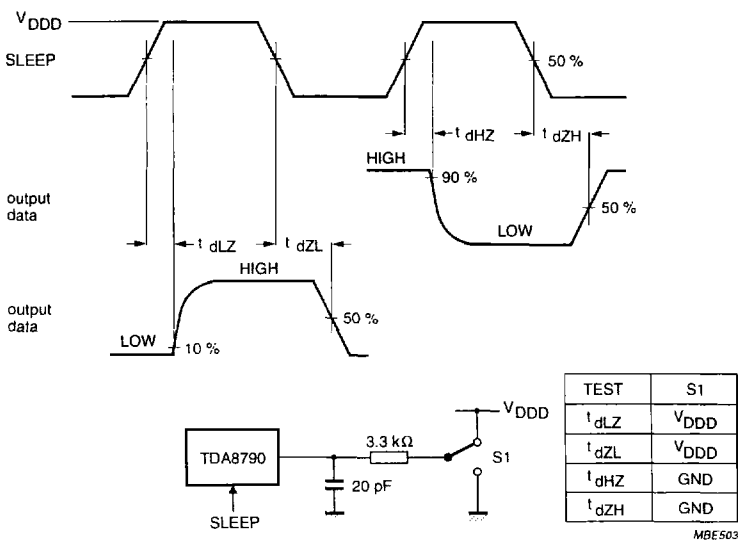



Fig.4 Timing diagram.




| TEST | S1 |
|---|---|
| $t_{dLZ}$ | $V_{DDD}$ |
| $t_{dZL}$ | $V_{DDD}$ |
| $t_{dHZ}$ | GND |
| $t_{dZH}$ | GND |

$f_{SLEEP}$ = 100 kHz.

Fig.5 Timing diagram and test conditions of 3-state output delay time.

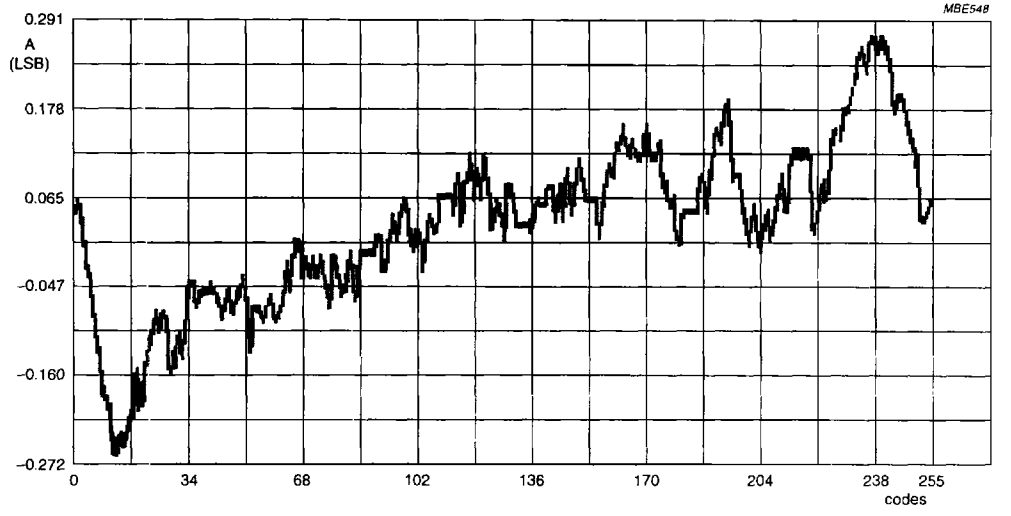



Fig.6 Typical integral non-linearity (INL) performance.

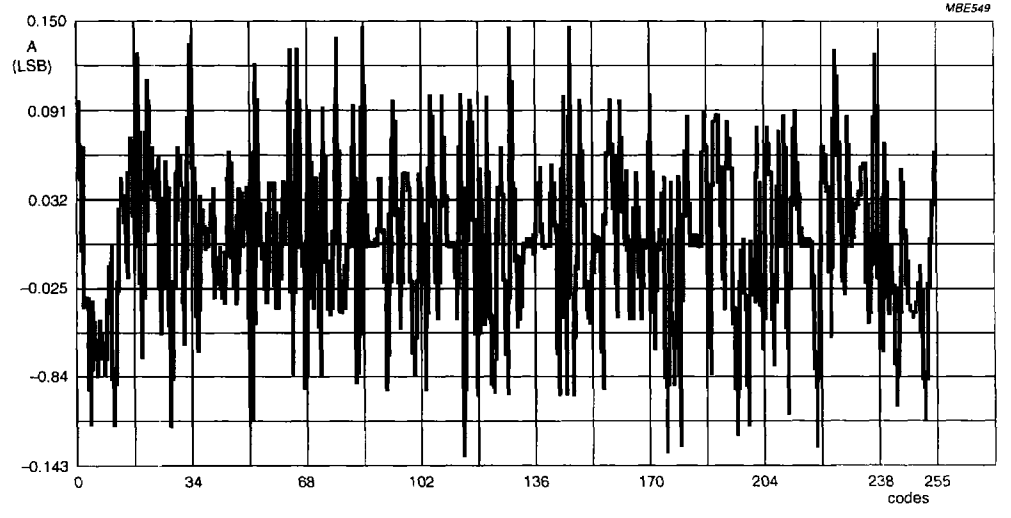



Fig.7 Typical differential non-linearity (DNL) performance.

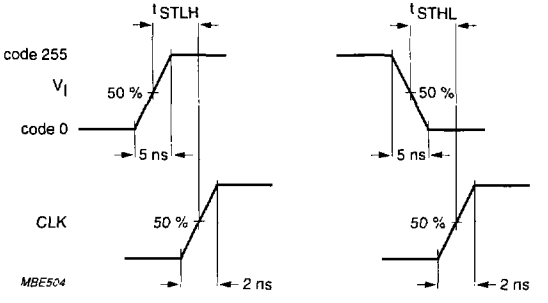
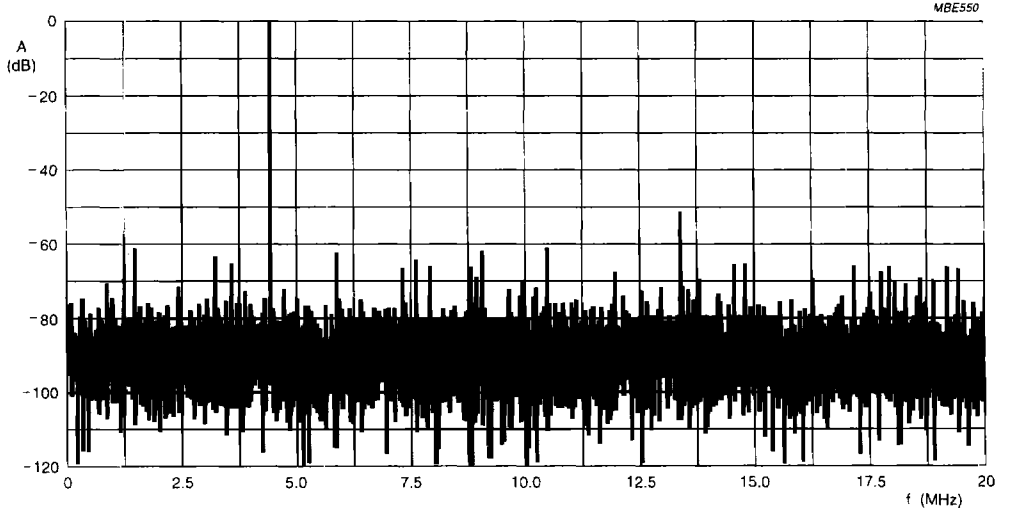



Fig.8 Analog input settling-time diagram.




*Effective bits*: 7.32; THD = 51.08 dB.
Harmonic levels (dB): 2nd = −68.99; 3rd = −51.62; 4th = −66.05; 5th = −63.23; 6th = −72.79.

Fig.9 Typical Fast Fourier Transform ($f_{clk}$ = 40 MHz; $f_i$ = 4.43 MHz).

## INTERNAL PIN CONFIGURATIONS

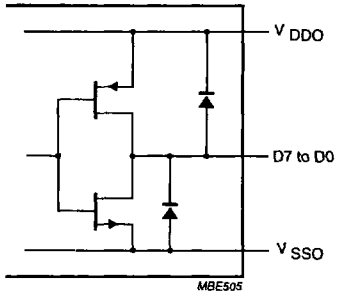



Fig.10 CMOS data outputs.

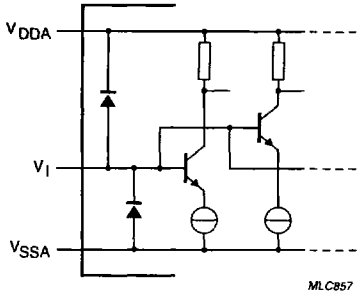



Fig.11 Analog inputs.

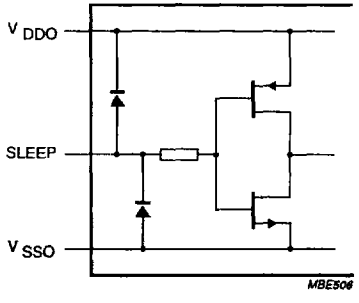



Fig.12 SLEEP 3-state input.

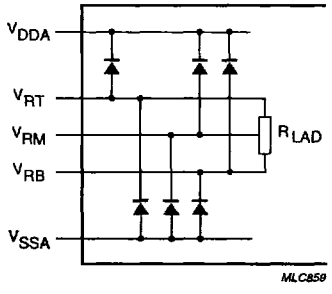



Fig.13 $V_{RB}$, $V_{RM}$ and $V_{RT}$.

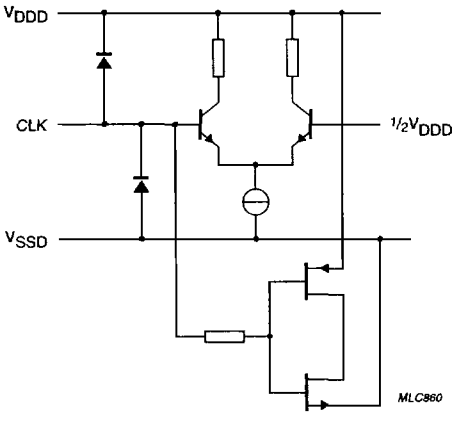
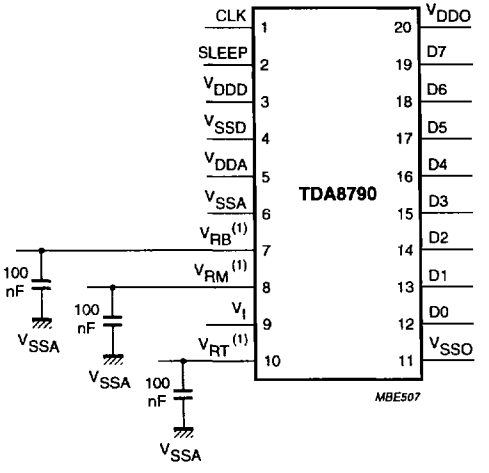



Fig.14 CLK input.

## APPLICATION INFORMATION




The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated $V_{DDA}$ supply through a resistor bridge and a decoupled capacitor.

(1) $V_{RB}$, $V_{RM}$ and $V_{RT}$ are decoupled to $V_{SSA}$.

Fig.15 Application diagram.