NEC

MOS INTEGRATED CIRCUIT
MC-45V8AD641KS

8M-WORD BY 64-BIT
VIRTUAL CHANNEL SYNCHRONOUS DYNAMIC RAM MODULE (SO DIMM)

Description

The MC-45V8AD641KS is a 8,388,608 words by 64 bits virtual channel synchronous dynamic RAM module (small outline DIMM) on which 8 pieces of 64M virtual channel SDRAM : μPD4565161 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 64 bits organization
- Clock frequency and access time from CLK

	Part number	Read latency	Clock frequency (MAX.)	Access time from CLK (MAX.)	Maximum supply current				
					Operating			Refresh	
					Prefetch	Restore	Channel read / write (Burst)	Auto	Self
	MC-45V8AD641KS-A75	2	133 MHz	5.4 ns	440 mA		480 mA	640 mA	8 mA
	MC-45V8AD641KS-A10		100 MHz	6 ns	420 mA		400 mA	560 mA	
	MC-45V8AD641KS-A15	1	67 MHz	12 ns	380 mA		340 mA	540 mA	
★	MC-45V8AD641KS-A75L	2	133 MHz	5.4 ns	440 mA		480 mA	640 mA	4 mA
★	MC-45V8AD641KS-A10L		100 MHz	6 ns	420 mA		400 mA	560 mA	
★	MC-45V8AD641KS-A15L	1	67 MHz	12 ns	380 mA		340 mA	540 mA	

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Dual internal banks controlled by BA0 (Bank Select)
- Programmable burst-length : 1, 2, 4, 8 or 16
- Programmable wrap sequence : Sequential or Interleave
- Prefetch read latency : 4
- Auto precharge and without auto precharge
- Auto refresh and self refresh
- Single 3.3 V ± 0.3 V power supply
- LVTTL compatible
- 4,096 refresh cycles / 64 ms
- 144-pin small outline dual in-line memory module (Pin pitch = 0.8 mm)
- Unbuffered type
- Serial PD

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The mark ★ shows major revised points.

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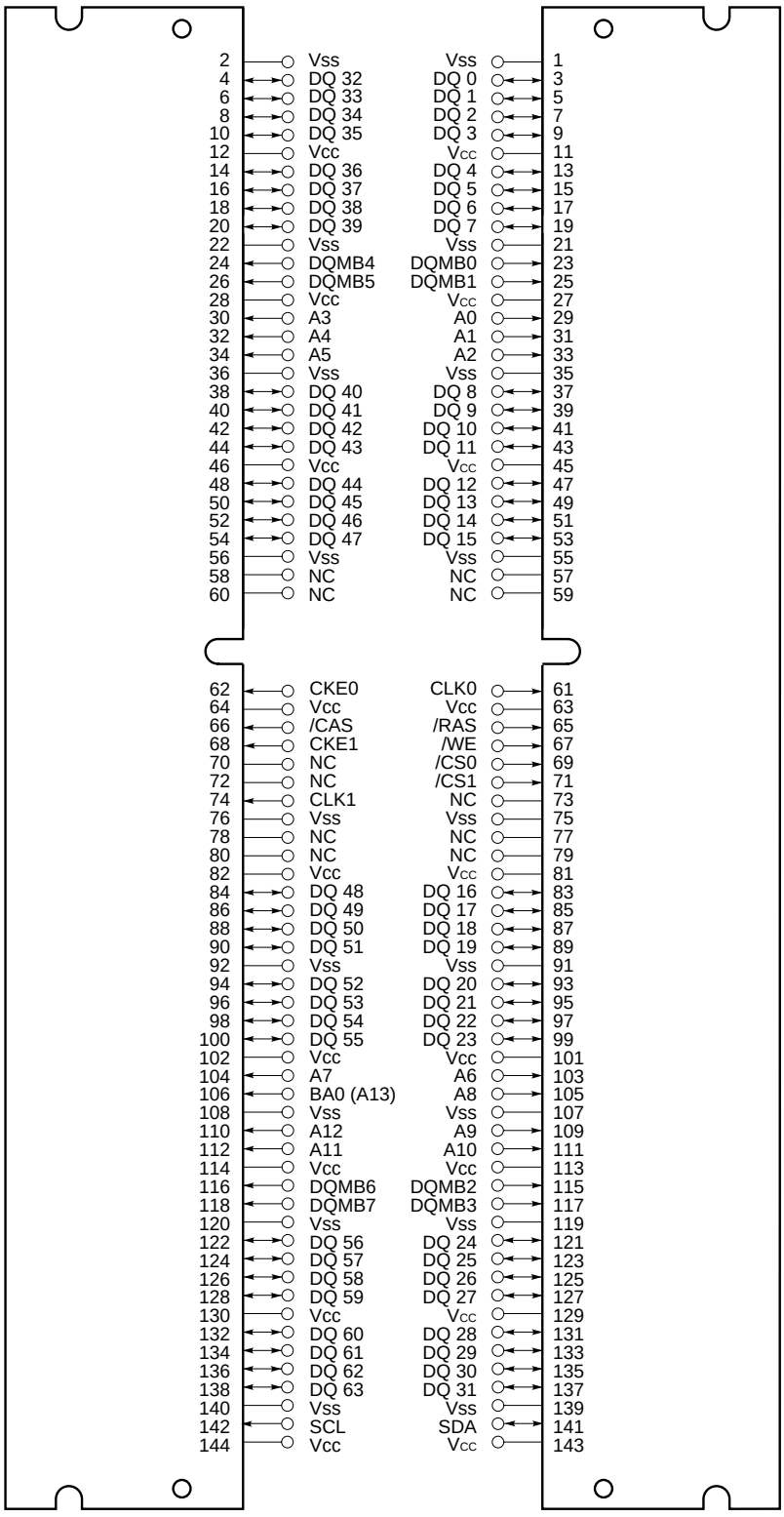
★ Ordering Information

Part number	Clock frequency (MAX.)	Read latency	Prefetch read latency	Package	Mounted devices
MC-45V8AD641KS-A75	133 MHz	2	4	144-pin Small Outline DIMM (Socket type) Edge connector : Gold plated 26.67 mm (1.05 inch) height	8 pieces of μPD4565161G5 (400 mil TSOP (II))
MC-45V8AD641KS-A10	100 MHz				
MC-45V8AD641KS-A15	67 MHz	1			
MC-45V8AD641KS-A75L[Note]	133 MHz	2			
MC-45V8AD641KS-A10L	100 MHz				
MC-45V8AD641KS-A15L[Note]	67 MHz	1			

Note Under development

Pin Configuration

144-pin Small Outline Dual In-line Memory Module Socket Type (Edge connector : Gold plated)

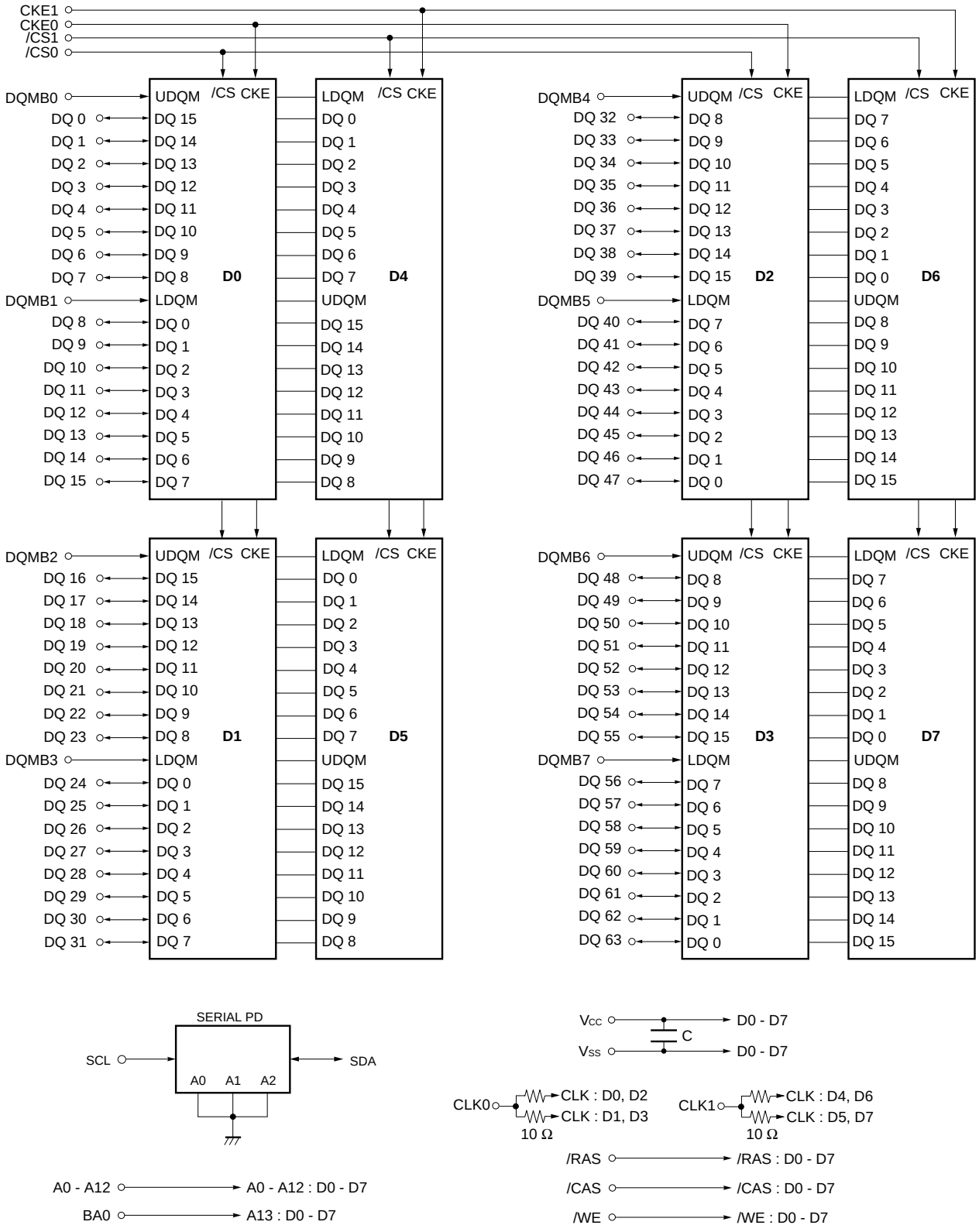


2	Vss	Vss	1		
4	DQ 32	DQ 0	3		
6	DQ 33	DQ 1	5		
8	DQ 34	DQ 2	7		
10	DQ 35	DQ 3	9		
12	Vcc	Vcc	11		
14	DQ 36	DQ 4	13		
16	DQ 37	DQ 5	15		
18	DQ 38	DQ 6	17		
20	DQ 39	DQ 7	19		
22	Vss	Vss	21		
24	DQMB4	DQMB0	23		
26	DQMB5	DQMB1	25		
28	Vcc	Vcc	27		
30	A3	A0	29		
32	A4	A1	31		
34	A5	A2	33		
36	Vss	Vss	35		
38	DQ 40	DQ 8	37		
40	DQ 41	DQ 9	39		
42	DQ 42	DQ 10	41		
44	DQ 43	DQ 11	43		
46	Vcc	Vcc	45		
48	DQ 44	DQ 12	47		
50	DQ 45	DQ 13	49		
52	DQ 46	DQ 14	51		
54	DQ 47	DQ 15	53		
56	Vss	Vss	55		
58	NC	NC	57		
60	NC	NC	59		
62	CKE0	CLK0	61		
64	Vcc	Vcc	63		
66	/CAS	/RAS	65		
68	CKE1	/WE	67		
70	NC	/CS0	69		
72	NC	/CS1	71		
74	CLK1	NC	73		
76	Vss	Vss	75		
78	NC	NC	77		
80	NC	NC	79		
82	Vcc	Vcc	81		
84	DQ 48	DQ 16	83		
86	DQ 49	DQ 17	85		
88	DQ 50	DQ 18	87		
90	DQ 51	DQ 19	89		
92	Vss	Vss	91		
94	DQ 52	DQ 20	93		
96	DQ 53	DQ 21	95		
98	DQ 54	DQ 22	97		
100	DQ 55	DQ 23	99		
102	Vcc	Vcc	101		
104	A7	A6	103		
106	BA0 (A13)	A8	105		
108	Vss	Vss	107		
110	A12	A9	109		
112	A11	A10	111		
114	Vcc	Vcc	113		
116	DQMB6	DQMB2	115		
118	DQMB7	DQMB3	117		
120	Vss	Vss	119		
122	DQ 56	DQ 24	121		
124	DQ 57	DQ 25	123		
126	DQ 58	DQ 26	125		
128	DQ 59	DQ 27	127		
130	Vcc	Vcc	129		
132	DQ 60	DQ 28	131		
134	DQ 61	DQ 29	133		
136	DQ 62	DQ 30	135		
138	DQ 63	DQ 31	137		
140	Vss	Vss	139		
142	SCL	SDA	141		
144	Vcc	Vcc	143		

/xxx indicates active low signal.

A0 - A12	: Address Inputs
[Row : A0 - A12, Column : A0 - A5]	
BA0 (A13)	: Virtual Channel SDRAM Bank Select
DQ0 - DQ63	: Data Inputs/Outputs
CLK0, CLK1	: Clock Input
CKE0, CKE1	: Clock Enable Input
/CS0, /CS1	: Chip Select Input
/RAS	: Row Address Strobe
/CAS	: Column Address Strobe
/WE	: Write Enable
DQMB0 - DQMB7	: DQ Mask Enable
SDA	: Serial Data I/O for PD
SCL	: Clock Input for PD
Vcc	: Power Supply
Vss	: Ground
NC	: No Connection

Block Diagram



Remark D0 - D7 : μPD4565161 (2M words × 16 bits × 2 banks)

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute power on sequence and auto refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		–0.5 to +4.6	V
Voltage on input pin relative to GND	V_T		–0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		8	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	A0 - A12, BA0 (A13), /RAS, /CAS, /WE, CLK0, CLK1, CKE0, CKE1, /CS0, /CS1 DQMB0 - DQMB7	TBD	TBD	TBD	pF
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ63	TBD	TBD	TBD	pF

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current (Prefetch mode at one bank active)	$I_{CC1}P$	$t_{RC} \geq t_{RC\ (MIN.)}$ Prefetch is executed one time during t_{RC}.	-A75		440	mA	1
			-A10		420		
			-A15		380		
Operating current (Restore mode at one bank active)	$I_{CC1}R$	$t_{RC} \geq t_{RC\ (MIN.)}$	-A75		440	mA	1
			-A10		420		
			-A15		380		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns			8	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞			4		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.			200	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞, Input signals are stable.			64		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns			40	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞			32		
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.			200	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞ Input signals are stable.			80		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, I_O = 0 mA Background : precharge standby	-A75		480	mA	2
			-A10		400		
			-A15		340		
Auto refresh current	I_{CC5}	$t_{RC} \geq t_{RC\ (MIN.)}$	-A75		640	mA	3
			-A10		560		
			-A15		540		
★ Self refresh current	I_{CC6}	CKE ≤ 0.2 V	-Axx		8	mA	
			-AxxL		4		
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V, All other pins not under test = 0 V		−8	+8	μA	
Output leakage current	$I_{O\ (L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V		−1.5	+1.5	μA	
High level output voltage	V_{OH}	I_O = −4.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.0 mA			0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

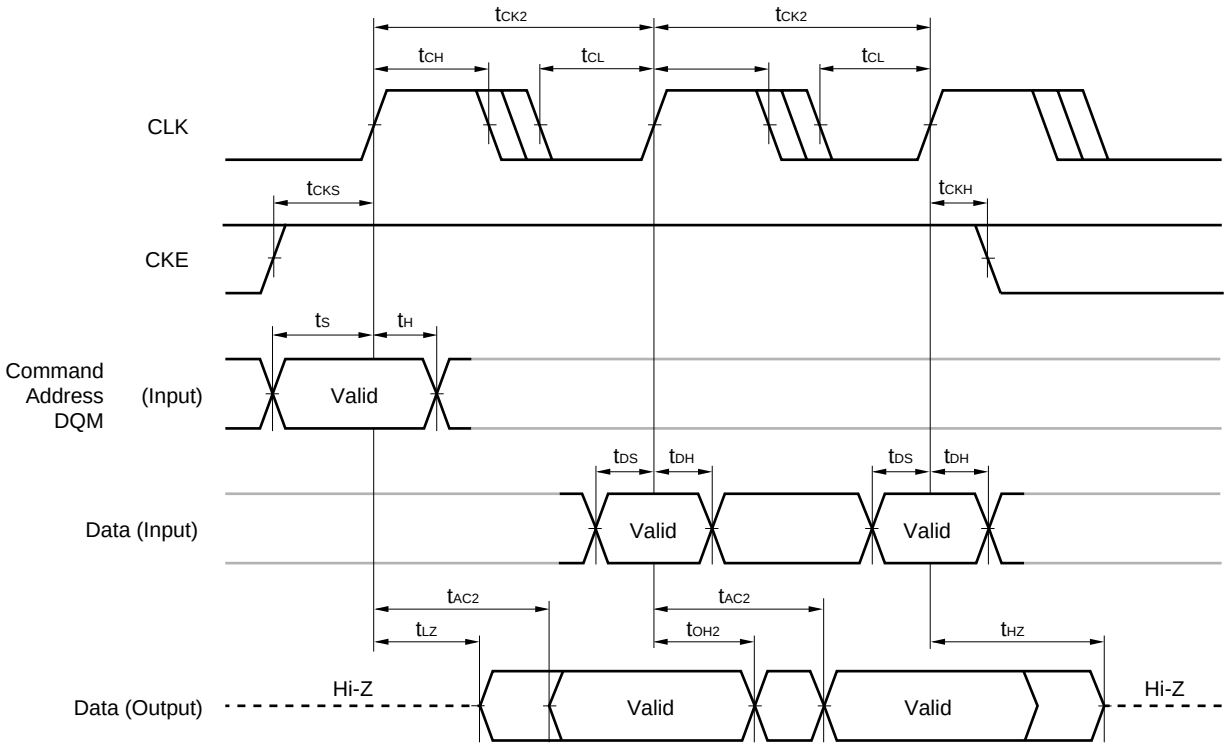
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

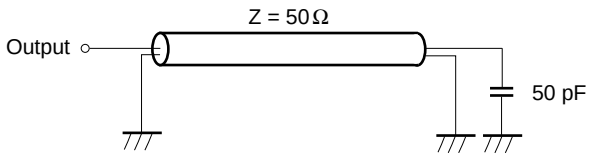
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\ (MIN.)}$ and $V_{IL\ (MAX.)}$.
- An access time is measured at 1.4 V.



★ **AC characteristics**

Parameter	Symbol	-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	t_{CK}	7.5	–	10	–	15	–	ns	
Access time from CLK	t_{AC}	–	5.4	–	6	–	12	ns	1
CLK high level width	t_{CH}	2.5	–	3	–	3	–	ns	
CLK low level width	t_{CL}	2.5	–	3	–	3	–	ns	
Data-out hold time	t_{OH}	2.7	–	3	–	3	–	ns	1
Data-out low-impedance time	t_{LZ}	0	–	0	–	0	–	ns	
Data-out high-impedance time	t_{HZ}	2.5	5.5	3	6	3	6	ns	
Data-in setup time	t_{DS}	1.5	–	2	–	2	–	ns	
Data-in hold time	t_{DH}	0.8	–	1	–	1	–	ns	
Address, Command, DQM setup time	t_{S}	1.5	–	2	–	2	–	ns	
Address, Command, DQM hold time	t_{H}	0.8	–	1	–	1	–	ns	
CKE setup time	t_{CKS}	1.5	–	2	–	2	–	ns	
CKE hold time	t_{CKH}	0.8	–	1	–	1	–	ns	
CKE setup time (Power down exit)	t_{CKSP}	1.5	–	2	–	2	–	ns	
Transition time	t_{T}	0.8	30	1	30	1	30	ns	
Refresh time (4,096 refresh cycles)	t_{REF}	–	64	–	64	–	64	ms	
Mode register set cycle time	t_{RSC}	2	–	2	–	2	–	CLK	

★ **Note 1.** Output load.



★ **AC characteristics (Background to Background operation)**

Parameter	Symbol	-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Same Bank Operation									
ACT to ACT / REF Command period	t_{RC}	67.5	–	80	–	90	–	ns	
REF to REF / ACT Command period	t_{RCF}	67.5	–	80	–	90	–	ns	
ACT to PRE Command period	t_{RAS}	52	120,000	60	120,000	60	120,000	ns	
PRE to ACT / REF Command period	t_{RP}	20	–	20	–	30	–	ns	
ACT to PFC / PFCA / PPF / PPFA Command delay time	t_{APD}	15	–	20	–	30	–	ns	
ACT to PFR Command delay time (Prefetch read operation)	t_{APRD}	20	–	20	–	TBD	–	ns	3
PFC to PRE Command delay time	t_{PPL}	22.5	–	30	–	30	–	ns	
PFCA / PFR to ACT / REF Command delay time	t_{PAL}	45	–	50	–	60	–	ns	
PPF to PRE Command delay time	t_{PPP}	45	–	60	–	75	–	ns	
PPFA to ACT / REF Command delay time	t_{PPA}	67.5	–	80	–	90	–	ns	
RST / RSTA to ACT (R) Note1 Command delay time	t_{RAD}	7.5	30	10	40	10	60	ns	2
Same, Other Bank Operation									
ACT (R) Note1 to PFC / PFCA / PFR / PPF / PPFA Command delay time	t_{RPD}	37.5	–	40	–	45	–	ns	
PFC to PFC / PFCA Command delay time	t_{PPD}	22.5	–	30	–	30	–	ns	
PPF to PPF / PPFA Command delay time	t_{PPPD}	45	–	60	–	75	–	ns	
Other Bank Operation									
ACT to ACT / ACT (R) or ACT (R) to ACT Command delay time	t_{RRD}	15	–	20	–	30	–	ns	
ACT (R) to ACT (R) Command delay time	t_{RRDR}	30	–	40	–	45	–	ns	
PFC / PFCA to RST / RSTA Command delay time	t_{PRD}	22.5	–	30	–	30	–	ns	
PPF / PPFA to RST / RSTA Command delay time	t_{PPRD}	45	–	60	–	75	–	ns	

Notes 1. ACT (R) command is ACT command after RST command.

2. The another background operation and same channel foreground operation are illegal while t_{RAD} period.

3. When Read latency of SCLR (Set Channel Latency Register) is set up 1, this operation can not be used.

★ **AC characteristics (Foreground to Foreground operation)**

Parameter	Symbol	-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
READ / WRITE to READ / WRITE Command delay time	t_{CCD}	7.5	–	10	–	15	–	ns	

★ **AC characteristics (Background to Foreground operation)**
(after same channel Prefetch / Restore)

Parameter	Symbol	-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
PFC / PFCA / PPF / PPFA to READ / WRITE Command delay time	t_{PCD}	15	–	20	–	30	–	ns	
PPF / PPFA to READ / WRITE Command delay time (2nd prefetch channel read write)	t_{PPCD}	37.5	–	50	–	75	–	ns	
ACT (R) to READ / WRITE Command delay time	t_{RCD}	30	–	40	–	45	–	ns	1

Note 1. ACT (R) command is ACT command after RST command.

★ Serial PD

(1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		08H	0	0	0	0	1	0	0	0	VC SDRAM
3	Number of row addresses		0DH	0	0	0	0	1	1	0	1	13 rows
4	Number of column addresses		06H	0	0	0	0	0	1	1	0	6 columns
5	Number of banks		02H	0	0	0	0	0	0	1	0	2 banks
6	Data width		40H	0	1	0	0	0	0	0	0	64 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface standard		01H	0	0	0	0	0	0	0	1	LVTTL
9	Read latency (/CAS latency) = 2 cycle time	-A75	75H	0	1	1	1	0	1	0	1	7.5 ns
		-A10	A0H	1	0	1	0	0	0	0	0	10 ns
		-A15	F0H	1	1	1	1	0	0	0	0	15 ns
10	Read latency (/CAS latency) = 2 access time	-A75	54H	0	1	0	1	0	1	0	0	5.4 ns
		-A10	60H	0	1	1	0	0	0	0	0	6 ns
		-A15	C0H	1	1	0	0	0	0	0	0	12 ns
11	DIMM configuration type		00H	0	0	0	0	0	0	0	0	None
12	Refresh rate / type		80H	1	0	0	0	0	0	0	0	Normal
13	VC SDRAM width		10H	0	0	0	1	0	0	0	0	×16
14	Error checking SDRAM width		00H	0	0	0	0	0	0	0	0	None
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		1FH	0	0	0	1	1	1	1	1	1, 2, 4, 8, 16
17	Number of banks on each VC SDRAM		02H	0	0	0	0	0	0	1	0	2 banks
18	Read latency (/CAS latency) supported		03H	0	0	0	0	0	0	1	1	1, 2
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	VC SDRAM module attributes		00H	0	0	0	0	0	0	0	0	
22	VC SDRAM device attributes : general		0EH	0	0	0	0	1	1	1	0	
23	Read latency (/CAS latency) = 1 cycle time	-A75	00H	0	0	0	0	0	0	0	0	Not supported
		-A10	00H	0	0	0	0	0	0	0	0	Not supported
		-A15	F0H	1	1	1	1	0	0	0	0	15 ns
24	Read latency (/CAS latency) = 1 access time	-A75	00H	0	0	0	0	0	0	0	0	Not supported
		-A10	00H	0	0	0	0	0	0	0	0	Not supported
		-A15	C0H	1	1	0	0	0	0	0	0	12 ns
25-26			00H	0	0	0	0	0	0	0	0	
27	$t_{RP\ (MIN.)}$	-A75	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns

(2/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
28	$t_{RRD\ (MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns
29	$t_{APD\ (MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns
30	$t_{RAS\ (MIN.)}$	-A75	34H	0	0	1	1	0	1	0	0	52 ns
		-A10	3CH	0	0	1	1	1	1	0	0	60 ns
		-A15	3CH	0	0	1	1	1	1	0	0	60 ns
31	Module bank density		08H	0	0	0	0	1	0	0	0	32M bytes
32	Address and command signal input setup time		20H	0	0	1	0	0	0	0	0	2 ns
33	Address and command signal input hold time		10H	0	0	0	1	0	0	0	0	1 ns
34	Data signal input setup time		20H	0	0	1	0	0	0	0	0	2 ns
35	Data signal hold setup time		10H	0	0	0	1	0	0	0	0	1 ns
36	Prefetch read latency	-A75	04H	0	0	0	0	0	1	0	0	4 clocks
		-A10	04H	0	0	0	0	0	1	0	0	4 clocks
		-A15	00H	0	0	0	0	0	0	0	0	Not supported
37	$t_{PCD\ (MIN.)}$	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns
38	Number of segment addresses		02H	0	0	0	0	0	0	1	0	2 bits
39	Number of channels		04H	0	0	0	0	0	1	0	0	16
40	Depth of channels		06H	0	0	0	0	0	1	1	0	64 bits
41-61												
62	SPD revision		02H	0	0	0	0	0	0	1	0	2.0
63	Checksum for bytes 0 - 62	-A75	63H	0	1	1	0	0	0	1	1	
		-A10	B1H	1	0	1	1	0	0	0	1	
		-A15	35H	0	0	1	1	0	1	0	1	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											

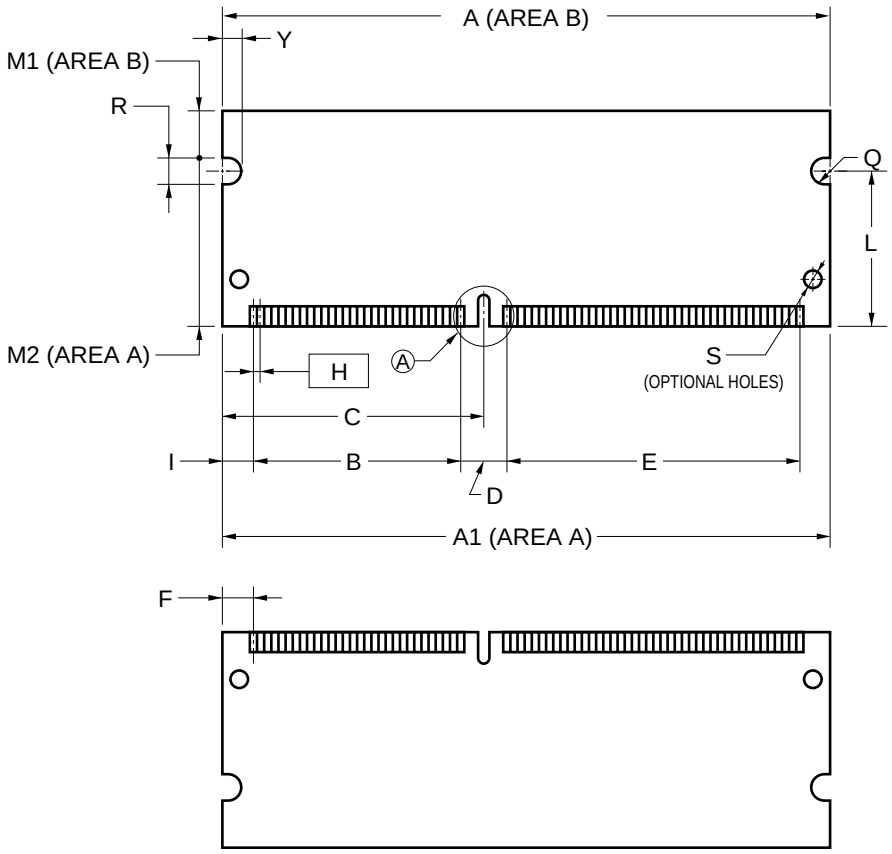
Timing Charts

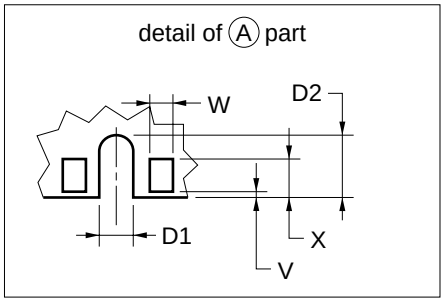
Please refer to the μPD4565421, 4565821, 4565161 Data sheet (M13022E).

Package Drawing

[MC-45V8AD641KS]

144 PIN DUAL IN-LINE MODULE (SOCKET TYPE)





ITEM	MILLIMETERS
A	67.6
A1	67.6±0.15
B	23.2
C	29.0
D	4.6
D1	1.5±0.10
D2	4.0
E	32.8
F	3.7
H	0.8(T.P)
I	3.3
L	20.0
M	31.75±0.15
M1	9.75
M2	22.0
N	3.8 MAX.
Q	R2.0
R	4.0±0.10
S	ϕ1.8
T	1.0±0.1
U1	3.2 MIN.
U2	4.0 MIN.
V	0.25 MAX.
W	0.6±0.05
X	2.55 MIN.
Y	2.0 MIN.

★ **Revision History**

Edition / Date	Page		Description	
	This edition	Previous edition	Type of revision	Location
4th edition / June 1999	Throughout	Throughout	Addition	Low power (-A75L, -A10L, -A15L)
	p.1	p.1	Deletion	-A70
	p.2	p.2		
	p.6	p.6		
			Addition	I_{CC6} (-AxxL)
	p.8	p.8	Deletion	-A70
			Modification	Note1
	p.9	p.9	Deletion	-A70 , t_{RCPD} , t_{DAL}
			Modification	t_{APD} (Parameter) , t_{RPD} (Parameter)
	p.10	p.10	Deletion	-A70
			Modification	t_{PCD} (Parameter)
	p.11	p.11	Deletion	-A70
	p.12	p.12		
	p.14	p.14	Addition	Revision History

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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