



## UR6512

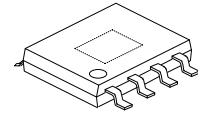
## LINEAR INTEGRATED CIRCUIT

### 2A DDR BUS TERMINATION REGULATOR

#### DESCRIPTION

The **UR6512** is a linear regulator providing up to 2A for DDR 1/DDR 2 and 1.5A for DDR 3 transient peak current and has sourcing and sinking capability for DDR SDRAM bus terminator applications while regulating an output voltage to within 20mV. It contains a high speed operational amplifier which provides fast load transient response and only requires 10uF of ceramic output capacitance.

The **UR6512** output termination voltage tracks the reference voltage applied at  $V_{REF}$  pin. A resistor divider connected to  $V_{IN}$ , GND and  $V_{REF}$  pins is used to force the reference voltage to  $V_{REF}$  pin. Additional features include current limiting protection and thermal shutdown protection.



HSOP-8

#### FEATURES

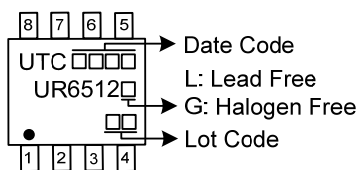
- \* DDR1/ DDR2/DDR3 Termination Voltage Applications
- \* Adjustable Output Voltage by External Resistors
- \* Integrated Power MOS Devices
- \* Suspend to RAM(STR) Functionality
- \* Current Limiting Protection
- \* Thermal Shutdown Protection
- \* Cost-Effective and Easy to Use

#### ORDERING INFORMATION

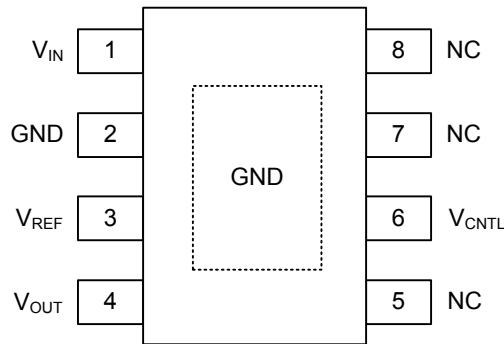
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UR6512G-SH2-R	UR6512G-SH2-R	HSOP-8	Tape Reel

<p>UR6512G-SH2-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) SH2: HSOP-8</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING



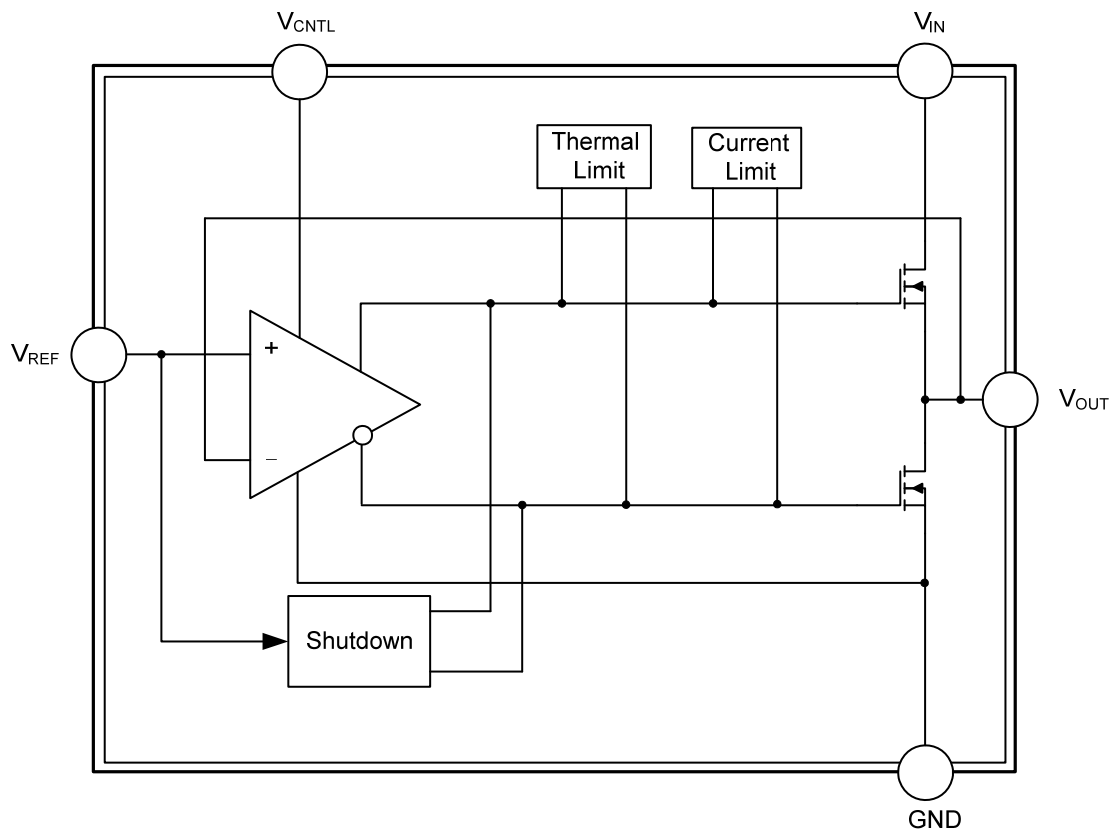
### PIN CONFIGURATIONS



### PIN DESCRIPTION

PIN NO	PIN NAME	PIN DESCRIPTION
1	V <sub>IN</sub>	Power supply pin for the V <sub>OUT</sub> output
2	GND	Ground pin
3	V <sub>REF</sub>	Reference voltage input and active-low shutdown control pin
4	V <sub>OUT</sub>	Output voltage pin
5,7,8	NC	No connect
6	V <sub>CNTL</sub>	Power supply pin for the internal control circuits
Exposed Pad	GND	Ground pin

### BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING ( $T_A=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
$V_{\text{CNTL}}$ Control Voltage	$V_{\text{CNTL}}$	6	V
$V_{\text{IN}}$ Supply Voltage	$V_{\text{IN}}$	6	V
Power Dissipation ( $T_A=25^\circ\text{C}$ )	$P_D$	1.176	W
Junction Temperature	$T_J$	125	$^\circ\text{C}$
Storage Temperature	$T_{\text{STG}}$	-65 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (Note)	$\theta_{\text{JA}}$	86	$^\circ\text{C/W}$
Junction to Case	$\theta_{\text{JC}}$	15	$^\circ\text{C/W}$

■ RECOMMENDED OPERATING CONDITIONS (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
$V_{\text{CNTL}}$ Control Voltage	$V_{\text{CNTL}}$	(3.3 or 5) $\pm 5\%$	V
$V_{\text{IN}}$ Supply Voltage	$V_{\text{IN}}$	(1.5 ~ 2.5) $\pm 3\%$	V
$V_{\text{REF}}$ Input Voltage	$V_{\text{REF}}$	(0.75 ~ 1.25) $\pm 3\%$	V
Junction Temperature	$T_J$	-40 ~ +125	$^\circ\text{C}$

Notes: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.

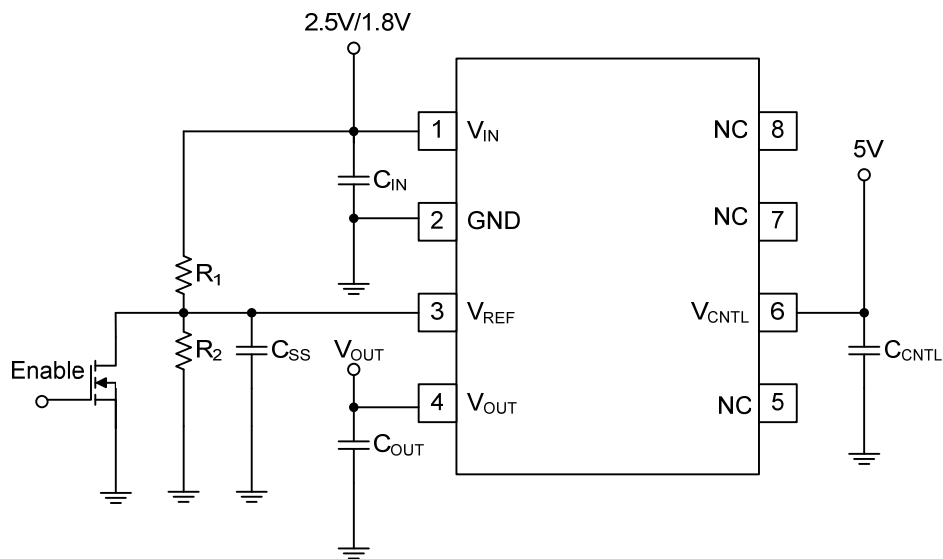
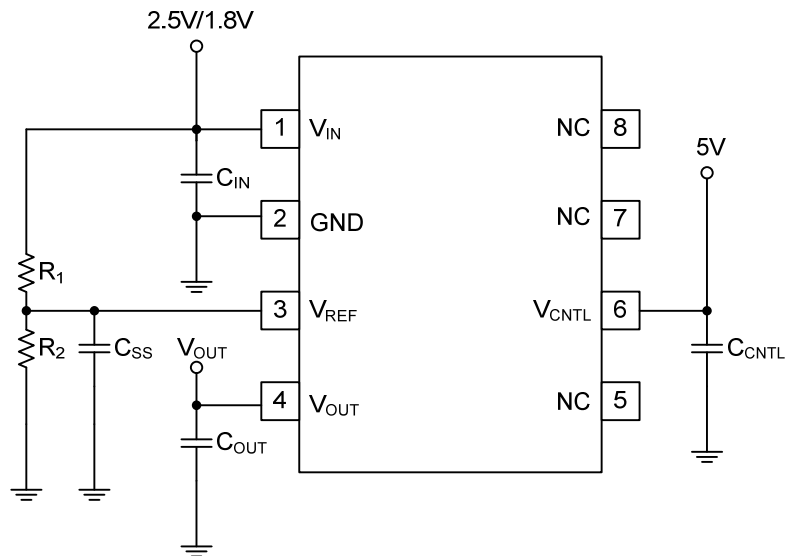
2. The  $V_{\text{OUT}}$  tracks the  $V_{\text{REF}}$  with additional voltage offset and load regulation.

■ ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ , unless otherwise specified)

( $V_{\text{IN}}=1.8\text{V}$ ,  $V_{\text{CNTL}}=5\text{V}$ ,  $V_{\text{REF}}=0.9\text{V}$ ,  $C_{\text{OUT}} = 10\mu\text{F}$  (Ceramic))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CURRENT</b>						
Operation Current of $V_{\text{CNTL}}$	$I_{\text{CNTL}}$	$I_{\text{OUT}}=0\text{A}$		1	2.5	mA
Standby Current	$I_{\text{STB}}$	$V_{\text{REF}}<0.2\text{V}$ , $R_{\text{LOAD}}=180\Omega$		2	90	$\mu\text{A}$
<b>OUTPUT VOLTAGE (DDR/DDR II/DDR III)</b>						
Output Voltage Offset ( $V_{\text{REF}}-V_{\text{OUT}}$ )	$V_{\text{OS}}$	$I_{\text{OUT}}=0\text{A}$	-20		20	mV
Load Regulation	$\Delta V_{\text{LOAD}}$	DDR1/DDR2: $I_{\text{OUT}}=\pm 1.8\text{A}$	-20		20	mV
		DDR3: $I_{\text{OUT}}=\pm 1.5\text{A}$	-20		20	mV
<b>PROTECTION</b>						
Current Limit	$I_{\text{LIMIT}}$	$V_{\text{IN}}=2.5\text{V}/1.8\text{V}$	2			A
		$V_{\text{IN}}=1.5\text{V}$	1.5			A
Thermal Shutdown Temperature	$T_{\text{SD}}$	$V_{\text{CNTL}}=5\text{V}$	125	170		$^\circ\text{C}$
Thermal Shutdown Hysteresis	$\Delta T_{\text{SD}}$	$V_{\text{CNTL}}=5\text{V}$		35		$^\circ\text{C}$
<b><math>V_{\text{REF}}</math> Shutdown</b>						
Shutdown Threshold	$V_{\text{IH}}$	Enable	0.6			V
	$V_{\text{IL}}$	Shutdown			0.15	V

### ■ TYPICAL APPLICATIONS CIRCUIT

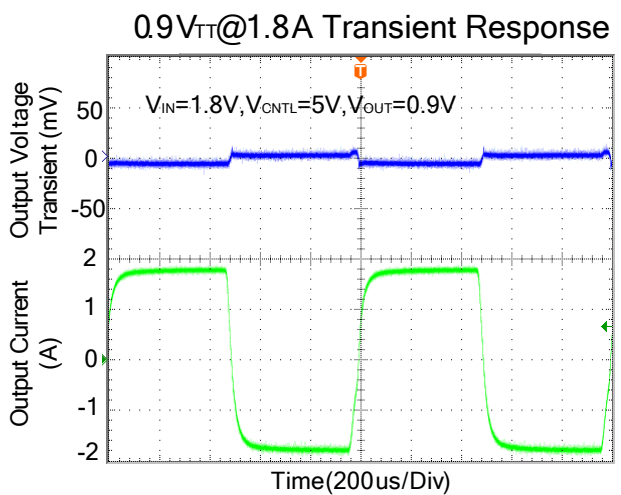
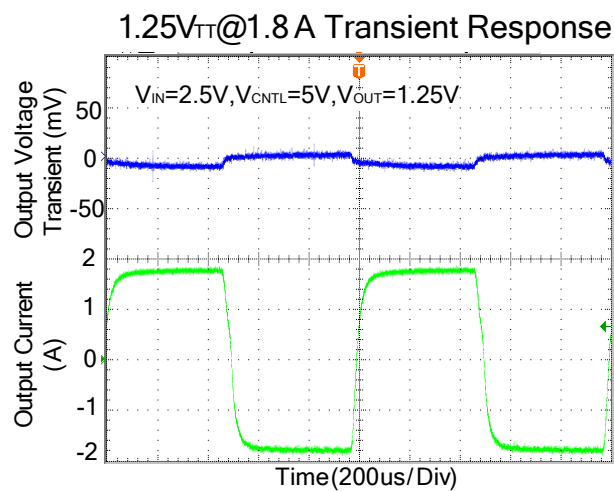
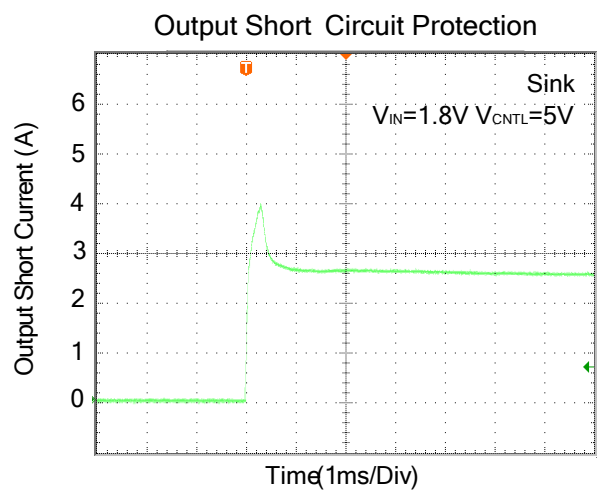
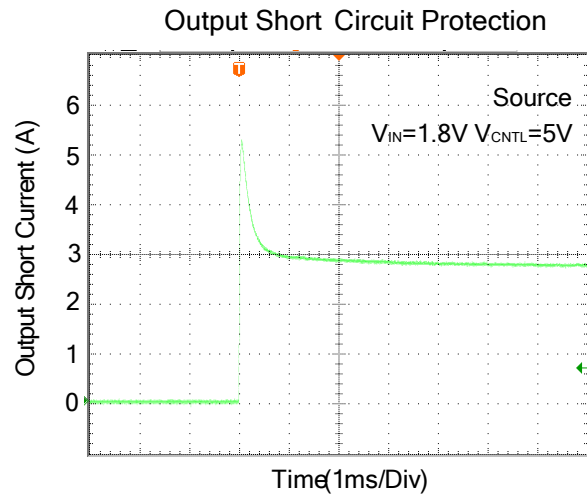
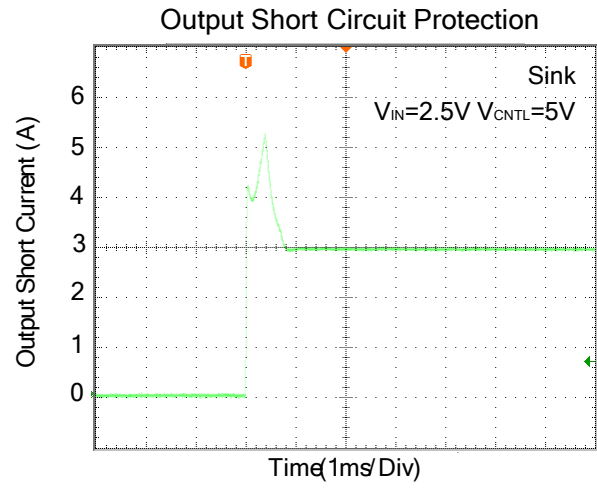
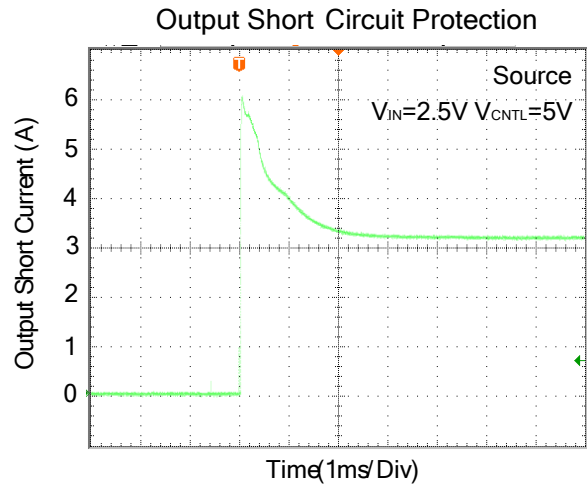


$R_1=R_2=100\text{K}\Omega$ ,  $C_{OUT}=10\mu\text{F}(\text{Ceramic})+1000\mu\text{F}$  under the worst case testing condition

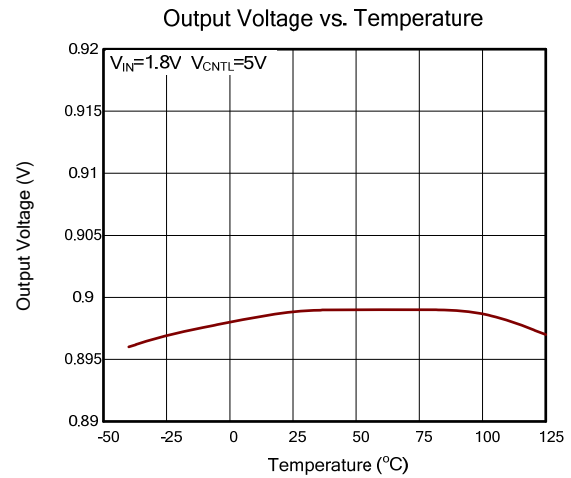
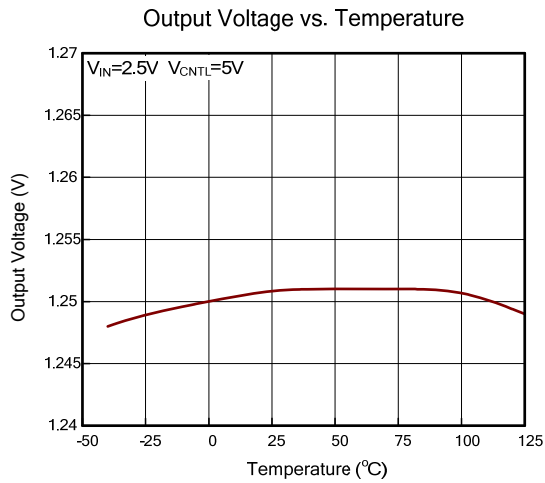
$C_{SS}=1\mu\text{F}$ ,  $C_{IN}=470\mu\text{F}(\text{Low ESR})$ ,  $C_{CNTRL}=47\mu\text{F}$

$$V_{REF} = \frac{R_2}{R_1 + R_2} V_{IN}(V), V_{OUT} \text{ track } V_{REF}$$

■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



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