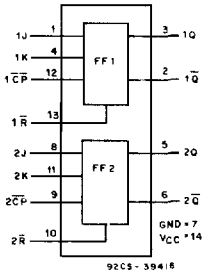
CD54/74HC107
CD54/74HCT107

File Number **1722**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual J-K Flip-Flop with Reset

Negative-Edge Trigger

Type Features:

- *Hysteresis on clock inputs for improved noise immunity and increased input Rise and Fall times.*
- *Asynchronous Reset*
- *Complementary Outputs*
- *Buffered Inputs*
- *Typical f_{max} = 60 MHz @ V_{CC} = 5V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC107 and CD54/74HCT107 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Reset and Clock inputs and Q and $\overline{Q}$ outputs. They change state on the negative-going transition of the clock pulse. Reset is accomplished asynchronously by a low-level input.

This device is functionally identical to the HC/HCT73 but differs in terminal assignment and in some parametric limits.

The 54HCT/74HCT logic family is functionally as well as pin-compatible with the standard 54LS/74LS logic family.

The CD54HC107 and CD54HCT107 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC107 and CD74HCT107 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

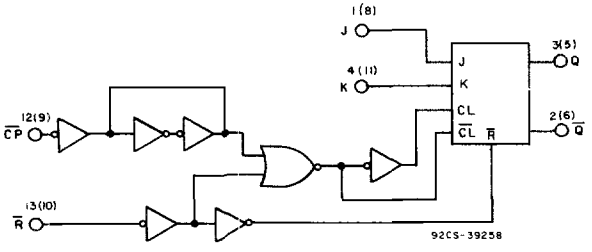


Fig. 1 - Logic diagram.

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↘	L	L	No Change	
H	↘	H	L	H	L
H	↘	L	H	L	H
H	↘	H	H	Toggle	
H	H	X	X	No Change	

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↘ = High-to-Low transition

CD54/74HC107
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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 V < V_O < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

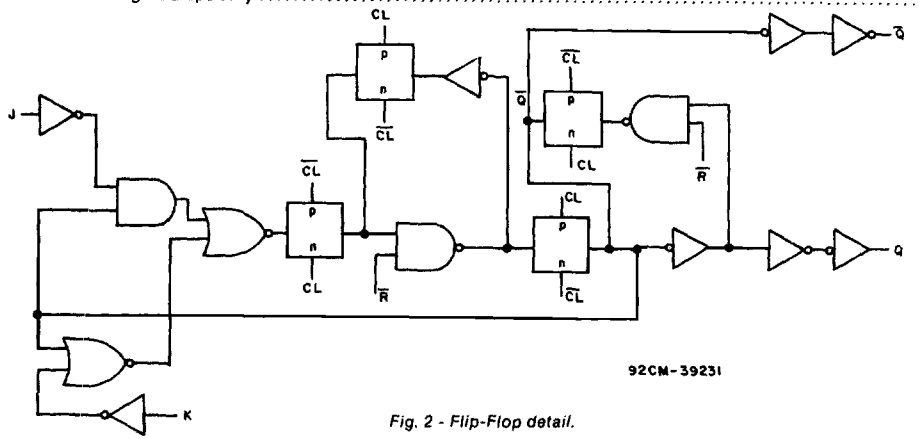


Fig. 2 - Flip-Flop detail.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}: *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f •			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.
• Applicable for all inputs except clock.

CD54/74HC107
CD54/74HCT107

STATIC ELECTRICAL CHARACTERISTICS

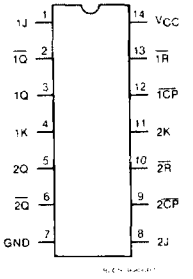
CHARACTERISTIC	CD74HC107, CD54HC107										CD74HCT107, CD54HCT107										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C			
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent *Device Current* I_{CC}	V_{CC} *or* Gnd	0	6	—	—	4	—	40	—	80	V_{CC} *or* Gnd	5.5	—	—	4	—	40	—	80		μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490		μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
All	0.3

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.



TERMINAL ASSIGNMENT

CD54/74HC107
CD54/74HCT107

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r, t_f=6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay $\overline{CP}$ to Q	t_{PLH} t_{PHL}	15	14	18	ns
$\overline{CP}$ to $\overline{Q}$			14	17	ns
$\overline{R}$ to Q, $\overline{Q}$			13	16	ns
$\overline{CP}$ Frequency	f_{max}	15	60	56	MHz
Power Dissipation Capacitance*	C_{PD}	—	31	30	pF

* C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2f_i + \Sigma\ C_LV_{CC}^2f_o$ where f_i = input frequency, f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

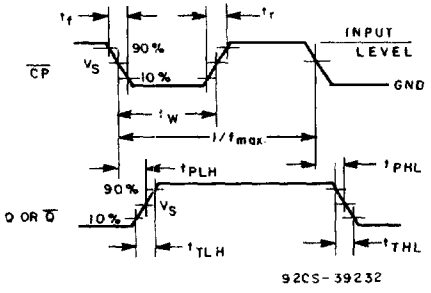
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min	HC Max	HCT Min	HCT Max	-40°C to +85°C 74HC Min	74HC Max	74HCT Min	74HCT Max	-55°C to +125°C 54HC Min	54HC Max	54HCT Min	54HCT Max	UNITS
Pulse Width $\overline{CP}$	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	18	—	20	—	23	—	24	—	27	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{R}$		2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	24	—	20	—	30	—	24	—	36	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time J, K to $\overline{CP}$	t_{SU}	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Hold Time J, K to $\overline{CP}$	t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
		4.5	3	—	5	—	3	—	5	—	3	—	5	—	
		6	3	—	—	—	3	—	—	—	3	—	—	—	
Removal Time	t_{rem}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
$\overline{CP}$ Frequency	f_{max}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	28	—	25	—	22	—	20	—	19	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	

CD54/74HC107
CD54/74HCT107

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min	HC Max	HCT Min	HCT Max	-40°C to +85°C 74HC Min	74HC Max	74HCT Min	74HCT Max	-55°C to +125°C 54HC Min	54HC Max	54HCT Min	54HCT Max	UNITS
Propagation Delay $\overline{CP}$ to Q	t_{PLH}	2	—	170	—	—	—	215	—	—	—	255	—	—	
	t_{PHL}	4.5	—	34	—	43	—	43	—	54	—	51	—	65	ns
		6	—	29	—	—	—	37	—	—	—	43	—	—	
$\overline{CP}$ to $\overline{Q}$		2	—	170	—	—	—	215	—	—	—	255	—	—	
		4.5	—	34	—	40	—	43	—	50	—	51	—	60	ns
		6	—	29	—	—	—	37	—	—	—	43	—	—	
$\overline{R}$ to Q, $\overline{Q}$		2	—	155	—	—	—	195	—	—	—	235	—	—	
		4.5	—	31	—	38	—	39	—	48	—	47	—	57	ns
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



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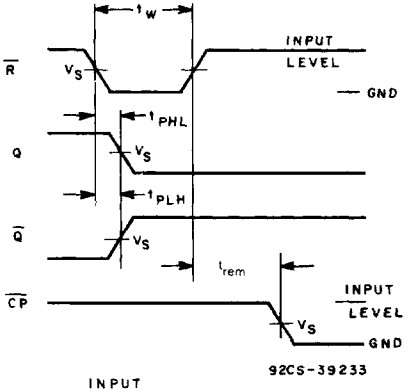

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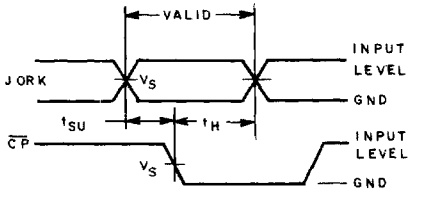

92CS-39234

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

Fig. 3 - Transition times, propagation delay times, and setup and hold times.