

Features

HARDWARE

- 8-Bit HCMOS Microcontroller
- Extended Version of MC68HC05C4A/C8A Family
 - Pin for Pin Compatible
- Power-Saving Stop, Wait and Data Retention Modes
 - STOP Instruction can be Disabled via Mask Option
- Fully Static Operation
- On-Chip Memory
 - CDP68HC05C4B, 68HCL05C4B, 68HSC05C4B
 - 176 Bytes RAM, 4160 Bytes ROM
 - CDP68HC05C8B, 68HCL05C8B, 68HSC05C8B
 - 176 Bytes RAM, 7744 Bytes ROM
- Keyboard Scanning Logic
- Watchdog Timer (COP)
- 24 Bidirectional I/O Lines and 7 Input-Only Lines
 - 1 High Current Output for LED drive (PC7)
- Internal 16-Bit Timer
- Serial Communications Interface (SCI) System
- Serial Peripheral Interface (SPI) System
- Fixed Frequency Tone/Simple PWM Outputs (Mask Programmable)
- Self-Check Mode
- External, Timer, SCI, and SPI Interrupts
- Master Reset and Power-On Reset
- On-Chip Oscillator with RC or Crystal Mask Options
- CDP68HC05C4B, CDP68HC05C8B
 - 4.2MHz Oscillator (2.1MHz Internal Bus Frequency) at 5V; 2.0MHz (1.0MHz Internal Bus) at 3.0V
 - Single 3.0V to 6.0V Supply (1.2V Data Retention Mode)
- CDP68HCL05C4B, CDP68HCL05C8B
 - Lower Supply Current, I_{DD} in RUN, WAIT and STOP Modes at 5.5V, 2.5V and 1.8V
 - Single 1.8V to 6.0V Supply (1.2V Data Retention Mode)
- CDP68HSC05C4B, CDP68HSC05C8B
 - 8.0MHz Oscillator (4.0MHz Internal Bus Frequency)
 - Single 2.4V to 6.0V Supply (1.2V Data Retention Mode)

SOFTWARE

- Complete 68HC05 Instruction Set
- Efficient Use of Program Space
- Memory Mapped I/O
- Versatile Interrupt Handling
- True Bit Manipulation
- Addressing Modes with Indexed Addressing for Accessing Tables

Description

The CDP68HC05C4B HCMOS Microcomputer is a new member of the CDP68HC05 family of low-cost single chip microcomputers. It is an enhanced version of the CDP68HC05C4. The enhancements include keyboard scanning logic, a high current output pin, a watchdog timer, fixed tone outputs, and a maskable STOP instruction. This 8-bit microcomputer unit (MCU) also contains an on-chip oscillator, CPU, 176 bytes of RAM, 4160 bytes of user ROM in the CDP68HC05C4B and 7744 bytes of user ROM in the CDP68HC05C8B, I/O, two serial interface systems, and timer. The fully static design allows operation at frequencies down to DC, further reducing its already low-power consumption. All information pertaining to the CDP68HC05C4B MCU applies to the CDP68HC05C8B with the exception of the memory description.

The CDP68HCL05C4B and CDP68HCL05C8B MCU devices are low-power versions of the CDP68HC05C4B and CDP68HC05C8B, respectively. They contain all the features of the CDP68HC05C4B and CDP68HC05C8B with additional features of lower power consumption in the RUN, WAIT and STOP modes; and low voltage operation down to 2.4V. The CDP68HSC05C4B and CDP68HSC05C8B MCU devices are high-speed versions of the CDP68HC05C4B and CDP68HC05C8B, respectively. They also contain all the features of the CDP68HC05C4B and CDP68HC05C8B with the and have a higher frequency operation (up to 8.0MHz).

Table of Contents

Ordering Information	2
Pinouts	3
MCU Block Diagram	4
Characterization Curves	5
Electrical and Timing Specifications	6
Functional Pin Description	23
Input/Output Programming	25
Memory Maps	27
Memory	27
Self Check Mode	29
Resets, Interrupts and Low Power Modes	30
Hardware/Power-On Resets	30
COP Watchdog System	30
Interrupts	31
Low Power Modes	34
Programmable Timer	35
Counter	38
Output Compare	38
Input Capture	38
Serial Communications Interface (SCI)	40
Serial Peripheral Interface (SPI)	45
Port A Tone and Simple PWM Circuitry	52
Effects of STOP and WAIT modes	53
Package Outline Dimensions	54
Opcode Map	59
I/O, Control, Status and Data Register Definitions	61
Ordering Information Sheet	62

CDP68HC05C4B/C8B, CDP68HCL05C4B/C8B, CDP68HSC05C4B/C8B

Ordering Information

PART NUMBER	PACKAGE	PKG. NO.
CDP68HC05C4BE	40 Ld PDIP	E40.6
CDP68HC05C4BN	44 Ld PLCC	N44.65
CDP68HC05C4BQ	44 Ld MQFP	Q44.10x10
CDP68HC05C4BSE	42 Ld SPDIP	E42.6C
CDP68HC05C4BD	40 Ld SBDIP	D40.6
CDP68HC05C4BH	Chip	
CDP68HCL05C4BE	40 Ld PDIP	E40.6
CDP68HCL05C4BN	44 Ld PLCC	N44.65
CDP68HCL05C4BQ	44 Ld MQFP	Q44.10x10
CDP68HCL05C4BSE	42 Ld SPDIP	E42.6C
CDP68HCL05C4BD	40 Ld SBDIP	D40.6
CDP68HCL05C4BH	Chip	
CDP68HSC05C4BE	40 Ld PDIP	E40.6
CDP68HSC05C4BN	44 Ld PLCC	N44.65
CDP68HSC05C4BQ	44 Ld MQFP	Q44.10x10
CDP68HSC05C4BSE	42 Ld SPDIP	E42.6C
CDP68HSC05C4BD	40 Ld SBDIP	D40.6
CDP68HSC05C4BH	Chip	

NOTE: Pin number references throughout this specification refer to the 40 lead DIP. See pinouts for cross reference.

ROM Ordering Information

The CDP68HC05C4B and CDP68HC05C8B families of microcontrollers contain mask programmed ROMs. The contents of these ROMs are personalized to meet a customer's code requirements during manufacturing of the ICs. The code is programmed via photomasking techniques. Semiconductor manufacturing is a batch process, and all microcontrollers manufactured in a given lot (a batch) will contain identical ROM code.

Harris generates a customer's ROM mask from an ASCII representation of the desired ROM contents together with other specific information. The end of this document contains a sheet which can be used to provide the required information when ordering a masked ROM microcontroller.

Data Format Options

The ROM data can be submitted in various formats. The following list summarizes the principal formats which Harris will accept. The list is in order of preference, with S-Record formatted data files being the preferred format.

- **S-Record Formatted Hex Data File via modem upload**
- **S-Record Formatted Hex Data File via e-mail**
- **S-Record Formatted Hex Data File on floppy disk**
- **6805 Assembly Language Source File on floppy disk**
- **Contents of a 27XX type EPROM/EEPROM**

Regardless of the medium used to transfer the data, contents of all of the User ROM regions of the memory map of the particular microcontroller should be specified. This includes any Page 0 User ROM and User Reset/Interrupt Vectors. Data should not be specified for the Self Check ROM space of a device. All unused locations should either not be specified (S-Record and source files) or specified as \$00 (EPROM/EEPROM). Any unspecified locations will be filled with \$00 by Harris.

Procedure for Submitting Data

When submitting data via a physical medium such as a floppy disk or EPROM, the "Ordering Information Sheet" at the end of this document must be completed and submitted with the data.

When utilizing the Harris Customer Pattern Retrieval System (modem upload) the customer will be prompted for the same information as that specified on the "Ordering Information Sheet".

If the data is submitted via e-mail, the message should include the same information as that specified on the "Ordering Information Sheet".

Harris Customer Pattern Retrieval System

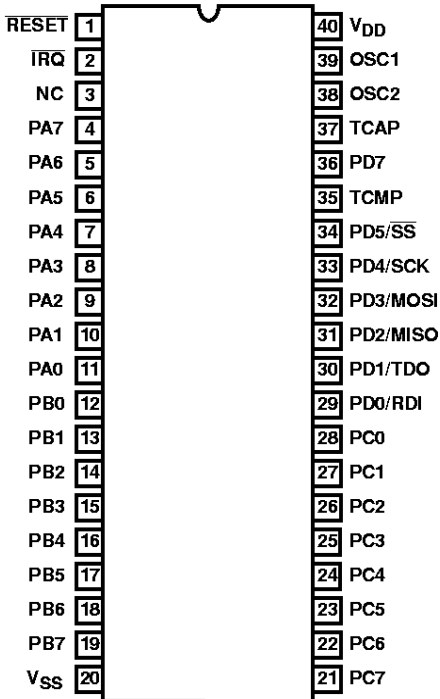
To access the Harris Customer Pattern Retrieval System, you must first obtain an account ID and password from your Harris sales representative. The system is accessed by dialing 1-908-685-6541. It is presently set to run with baud rates up to 2400 baud, with 8 data bits, 1 stop bit, and no parity bit. The data transfer is done using text mode Kermit transfers.

Check the Harris Corporate internet site, www.harris.com, for the latest information on the Harris Customer Pattern Retrieval System.

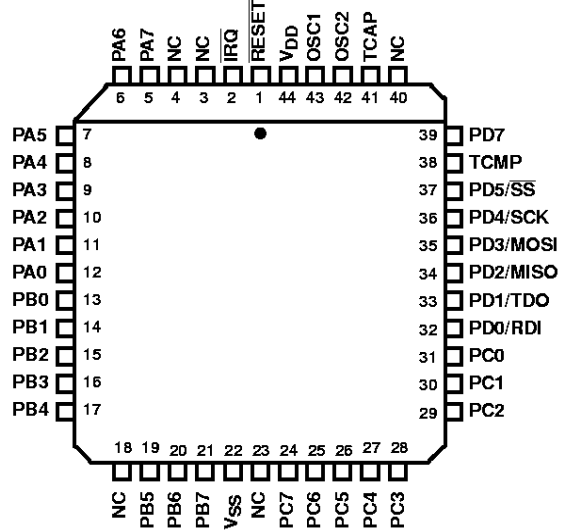
CDP68HC05C4B/C8B, CDP68HCL05C4B/C8B, CDP68HSC05C4B/C8B

Pinouts

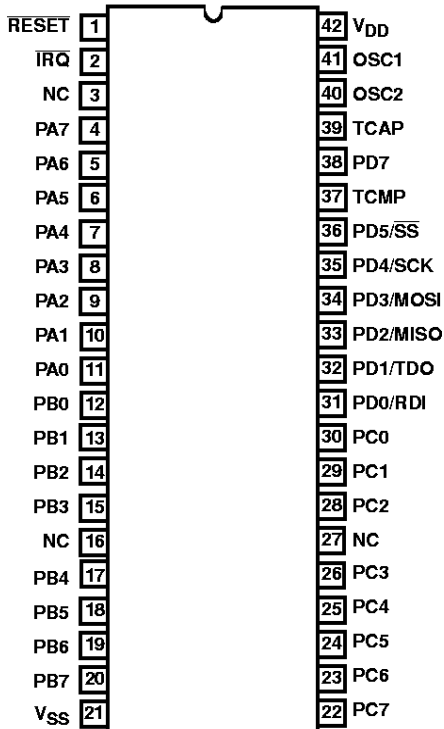
CDP68HC05C4B, CDP68HC05C8B
 CDP68HCL05C4B, CDP68HCL05C8B
 CDP68HSC05C4B, CDP68HSC05C8B
 (SBDIP, PDIP)
 TOP VIEW



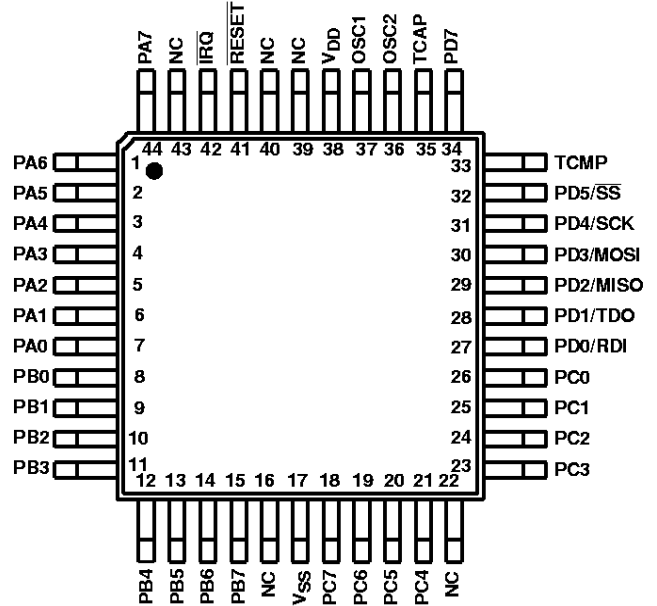
CDP68HC05C4B, CDP68HC05C8B
 CDP68HCL05C4B, CDP68HCL05C8B
 CDP68HSC05C4B, CDP68HSC05C8B
 (PLCC)
 TOP VIEW



CDP68HC05C4B, CDP68HC05C8B
 CDP68HCL05C4B, CDP68HCL05C8B
 CDP68HSC05C4B, CDP68HSC05C8B
 (SPDIP)
 TOP VIEW

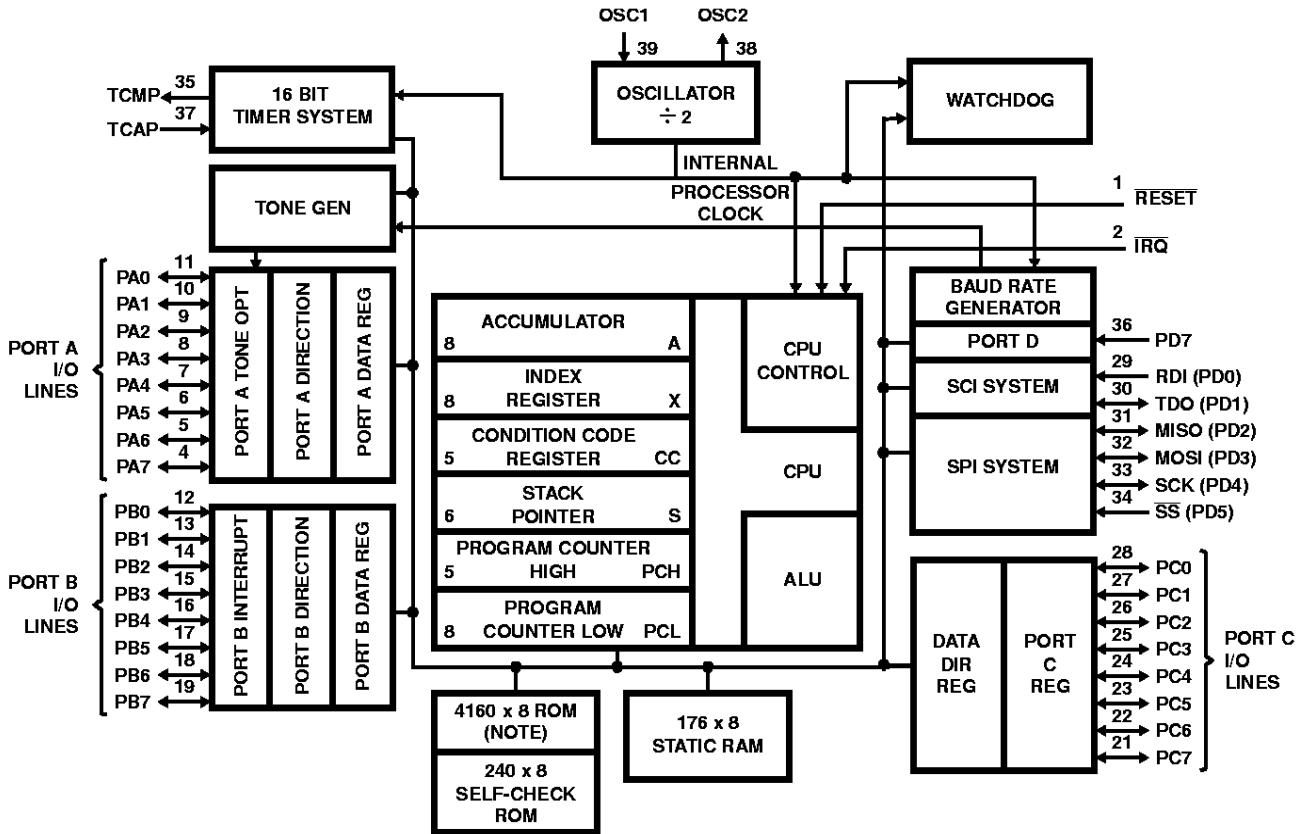


CDP68HC05C4B, CDP68HC05C8B
 CDP68HCL05C4B, CDP68HCL05C8B
 CDP68HSC05C4B, CDP68HSC05C8B
 (MQFP)
 TOP VIEW



NOTE: Low EMI Pinouts Available. Refer to Harris Tech Brief TB354 for more information

Microcomputer Block Diagram



NOTE: 7744 Bytes of ROM for: CDP68HC05C8B, CDP68HCL05C8B, CDP68HSC05C8B

Power Considerations

The average chip-junction temperature, T_J , in $^{\circ}\text{C}$ can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (\text{EQ. 1})$$

Where: T_A = Ambient Temperature, $^{\circ}\text{C}$
 θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, $^{\circ}\text{C}/\text{W}$

$P_D = P_{INT} + P_{I/O}$
 $P_{INT} = I_{CC} \times V_{CC}$, Watts - Chip Internal Power
 $P_{I/O}$ = Power Dissipation on Input and Output Pins - User Determined

For most applications $P_{I/O} \ll P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

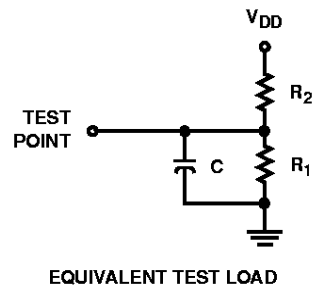
$$P_D = K \div (T_J + 273^{\circ}\text{C}) \quad (\text{EQ. 2})$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \cdot (T_A + 273^{\circ}\text{C}) + \theta_{JA} \cdot P_D^2 \quad (\text{EQ. 3})$$

Where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

PINS	R1	R2	C
$V_{DD} = 4.5\text{V}$			
PA0-7, PB0-7, PC0-7, PD6	3.26k Ω	2.38k Ω	50pF
PD1-4	1.9k Ω	2.26k Ω	200pF
$V_{DD} = 3.0\text{V}$			
PA0-7, PB0-7, PC0-7, PD6	10.19k Ω	6.32k Ω	50pF
PD1-4	6k Ω	6k Ω	200pF



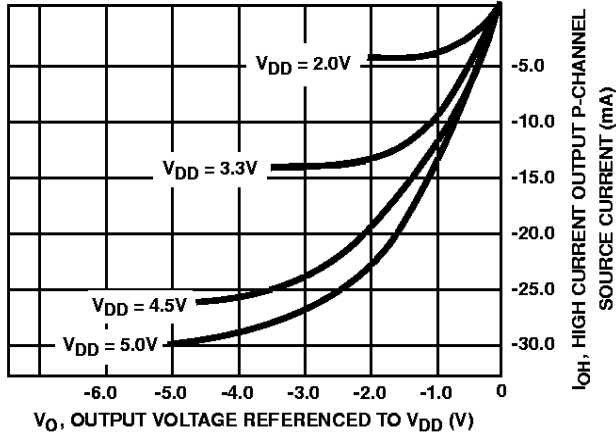


FIGURE 1A. TYPICAL PC7 PORT OUTPUT P-CHANNEL SOURCE CURRENT FOR $V_{DD} = 2V, 3.3V, 4.5V$ AND $5V$ AT $25^\circ C$

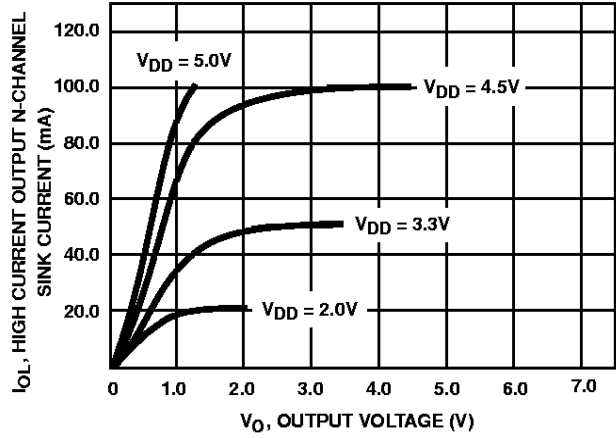


FIGURE 1B. TYPICAL PC7 PORT OUTPUT N-CHANNEL SINK CURRENT FOR $V_{DD} = 2V, 3.3V, 4.5V$ AND $5V$ AT $25^\circ C$

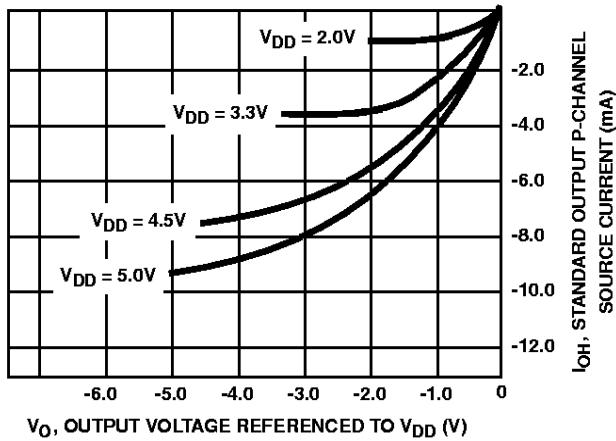


FIGURE 1C. TYPICAL PORT OUTPUT P-CHANNEL SOURCE CURRENT FOR $V_{DD} = 2V, 3.3V, 4.5V$ AND $5V$ AT $25^\circ C$

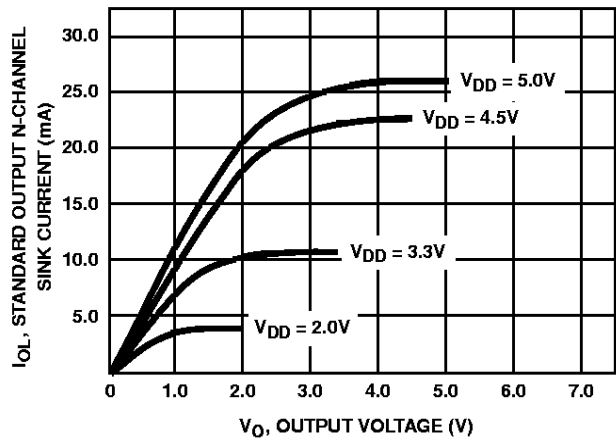


FIGURE 1D. TYPICAL PORT OUTPUT N-CHANNEL SINK CURRENT FOR $V_{DD} = 2V, 3.3V, 4.5V$ AND $5V$ AT $25^\circ C$

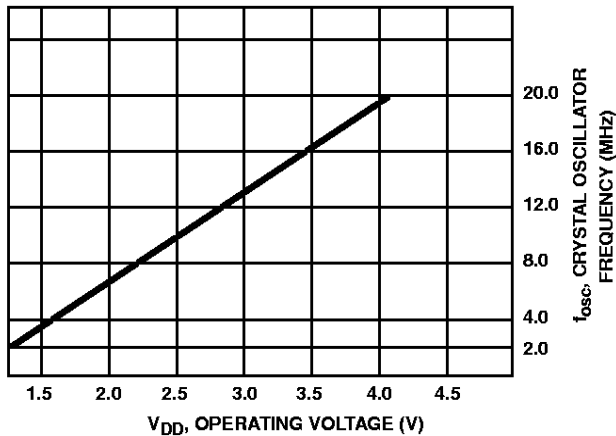


FIGURE 1E. TYPICAL CRYSTAL OSCILLATOR OPERATING FREQUENCIES vs OPERATING VOLTAGE, V_{DD} AT $25^\circ C$

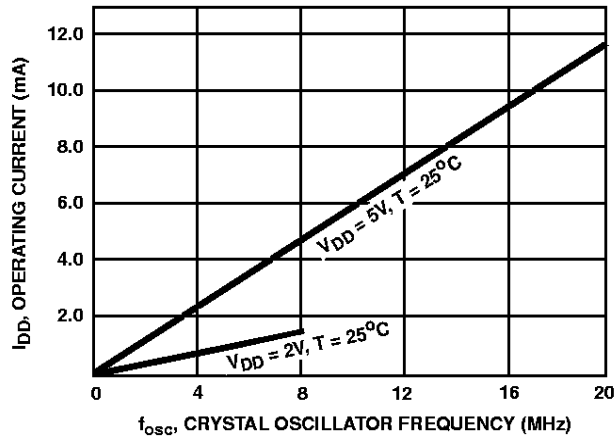


FIGURE 1F. TYPICAL SUPPLY CURRENT vs OPERATING FREQUENCY AT $25^\circ C$

CDP68HC05C4B/C8B Electrical Specifications

Absolute Maximum Ratings

Supply Voltage, V_{DD} -0.5V to +7V
 Input Voltage, V_{IN} $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
 Self-Check Mode (IRQ Pin Only), V_{IN} : $V_{SS} - 0.3V$ to $2 \times V_{DD} + 0.3V$
 Current Drain Per Pin Excluding V_{DD} and V_{SS} , I 25mA

Operating Conditions

Operating Voltage Range +4.5V to +5.5V
 Operating Temperature Range -55°C to 125°C
 CDP68HC05C4B, CDP68HC05C8B -40°C to 85°C
 CDP68HCL05C4B, CDP68HCL05C8B 0°C to 70°C
 CDP68HSC05C4B, CDP68HSC05C8B -40°C to 85°C
 Input Low Voltage 0V to +0.8V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SPDIP Package	55	N/A
PDIP Package	55	N/A
PLCC Package	45	N/A
MQFP Package	70	N/A
SBDIP Package	45	14
Maximum Junction Temperature (Hermetic Package)	175°C	
Maximum Junction Temperature (Plastic Package)	150°C	
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C (PLCC, MQFP - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications HC Product Type, $V_{DD} = 5.0V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HC05C4B/C8B $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$ (Note 2)						
Output Voltage	V_{OL}	$I_{LOAD} < 10\mu A$	-	-	0.1	V
	V_{OH}		$V_{DD} - 0.1$	-	-	V
Output High Voltage	V_{OH}	$I_{LOAD} = -0.8mA$	$V_{DD} - 0.8$	-	-	V
PA0-7, PB0-7, PC0-6, TCMP						
PD1-4						
PC7	V_{OH}	$I_{LOAD} = -1.6mA$	$V_{DD} - 0.8$	-	-	V
PC7	V_{OH}	$I_{LOAD} = -5.0mA$	$V_{DD} - 0.8$	-	-	V
Output Low Voltage	V_{OL}	$I_{LOAD} = 1.6mA$	-	-	0.4	V
PA0-7, PB0-7, PC0-6, PD1-4, TCMP						
PC7						
Input High Voltage	V_{IH}		$0.7 \cdot V_{DD}$	-	V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}	-	$0.2 \cdot V_{DD}$	V
Data Retention Mode	V_{RM}	$T_A = 0^\circ C$ to $70^\circ C$	1.2	-	-	V
Supply Current	I_{DD}	$f_{OSC} = 4.2MHz$ External Square Wave	-	3.5	5.25	mA
RUN (Note 6)				1.0	3.25	mA
WAIT (Notes 7, 9)		$T_A = 25^\circ C$	-	1.0	20.0	μA
STOP (Note 8)				-	-	50
STOP (Note 8)	$T_A = -40^\circ C$ to $85^\circ C$	-	-	-	-	μA
I/O Ports Hi-Z Leakage Current:	I_{OZ}		-	-	± 10	μA
PA0-7, PB0-7 (without pullups), PC0-7, PD1-4						
Input Current	I_{IN}		-	-	± 1	μA
RESET, IRQ, TCAP, OSC1, PD0, PD5, PD7	C_{OUT}		-	-	12	pF
Capacitance Ports (As Input or Output)						
RESET, IRQ, TCAP, OSC1, PD0-5, PD7	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		175	385	750	μA

CDP68HC05C4B/C8B Electrical Specifications

DC Electrical Specifications HC Product Type , $V_{DD} = 5.0V$ (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis Voltage: PB0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: RESET, IRQ, OSC1, TCAP	V_{HYS}		$0.1 \cdot V_{DD}$	1.0	$0.5 \cdot V_{DD}$	V

Control Timing HC Product Type, $V_{DD} = 5.0V$

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HC05C4B/C8B $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	4.2	MHz
External Clock Option	f_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal ($f_{OSC} \div 2$)	f_{OP}	-	2.1	MHz
External Clock ($f_{OSC} \div 2$)	f_{OP}	DC	2.1	MHz
Cycle Time (See Figure 15)	t_{CYC}	476	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{LCH}	-	100	ms
RESET Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	125	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{LIH}	125	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{LIH}	(Note11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	-	ns

DC Electrical Specifications HC Product Type , $V_{DD} = 3.3V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HC05C4B/C8B $V_{DD} = 3.3V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$ (Note 2)						
Output Voltage	V_{OL}	$I_{LOAD} < 10\mu A$	-	-	0.1	V
	V_{OH}		$V_{DD} - 0.1$	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMP	V_{OH}	$I_{LOAD} = -0.2mA$	$V_{DD} - 0.3$	-	-	V
PD1-4	V_{OH}	$I_{LOAD} = -0.4mA$	$V_{DD} - 0.3$	-	-	V
PC7	V_{OH}	$I_{LOAD} = -1.5mA$	$V_{DD} - 0.3$	-	-	V
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD1-4, TCMP	V_{OL}	$I_{LOAD} = 0.4mA$	-	-	0.3	V
PC7	V_{OL}	$I_{LOAD} = 6.0mA$	-	-	0.3	V
Input High Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IH}		$0.7 \cdot V_{DD}$	-	V_{DD}	V

CDP68HC05C4B/C8B Electrical Specifications

DC Electrical Specifications HC Product Type, $V_{DD} = 3.3V$ (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IL}		V_{SS}	-	$0.2 \cdot V_{DD}$	V
Data Retention Mode	V_{RM}	$T_A = 0^{\circ}C$ to $70^{\circ}C$	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	$f_{OSC} = 2.1MHz$ External Square Wave	-	1.0	1.6	mA
WAIT (Notes 7, 9)	I_{DD}		-	0.5	0.9	mA
STOP (Note 8)	I_{DD}	$T_A = 25^{\circ}C$	-	1.0	8.0	μA
STOP (Note 8)	I_{DD}	$T_A = -40^{\circ}C$ to $85^{\circ}C$	-	-	20	μA
I/O Ports Hi-Z Leakage Current: PA0-7, PB0-7 (without pullups), PC0-7, PD1-4	I_{OZ}		-	-	± 10	μA
Input Current RESET, IRQ, TCAP, OSC1, PD0, PD5, PD7	I_{IN}		-	-	± 1	μA
Capacitance Ports (As Input or Output) RESET, IRQ, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		75	175	350	μA
Input Hysteresis Voltage: PB0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: RESET, IRQ, OSC1, TCAP	V_{HYS}		$0.1 \cdot V_{DD}$	1.0	$0.5 \cdot V_{DD}$	V

Control Timing HC Product Type, $V_{DD} = 3.3V$

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HC05C4B/C8B $V_{DD} = 3.3V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 2)				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	2.1	MHz
External Clock Option	f_{OSC}	DC	2.1	MHz
Internal Operating Frequency				
Crystal ($f_{OSC} \div 2$)	f_{OP}	-	1.05	MHz
External Clock ($f_{OSC} \div 2$)	f_{OP}	DC	1.05	MHz
Cycle Time (See Figure 15)	t_{CYC}	952	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
RESET Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	250	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{LIH}	250	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{LIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	-	ns

CDP68HCL05C4B/C8B Electrical Specifications

DC Electrical Specifications HCL Product Type, $V_{DD} = 5.0V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HCL05C4B/C8B $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$ (Note 2)						
Output Voltage	V_{OL}	$I_{LOAD} < 10\mu A$	-	-	0.1	V
	V_{OH}		$V_{DD} - 0.1$	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMP	V_{OH}	$I_{LOAD} = -0.8mA$	$V_{DD} - 0.8$	-	-	V
PD1-4	V_{OH}	$I_{LOAD} = -1.6mA$	$V_{DD} - 0.8$	-	-	V
PC7	V_{OH}	$I_{LOAD} = -5.0mA$	$V_{DD} - 0.8$	-	-	V
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD1-4, TCMP	V_{OL}	$I_{LOAD} = 1.6mA$	-	-	0.4	V
PC7	V_{OL}	$I_{LOAD} = 10.0mA$	-	-	0.4	V
Input High Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IH}		$0.7 \cdot V_{DD}$	-	V_{DD}	V
Input Low Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IL}		V_{SS}	-	$0.2 \cdot V_{DD}$	V
Data Retention Mode	V_{RM}	$T_A = 0^\circ C$ to $70^\circ C$	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	$f_{OSC} = 4.2MHz$ External Square Wave	-	3.5	4.25	mA
WAIT (Notes 7, 9)	I_{DD}		-	1.6	2.25	mA
STOP (Note 8)	I_{DD}	$T_A = 25^\circ C$	-	1.0	15.0	μA
STOP (Note 8)	I_{DD}	$T_A = 0^\circ C$ to $70^\circ C$	-	-	25	μA
I/O Ports Hi-Z Leakage Current:						
PA0-7, PB0-7 (without pullups), PC0-7, PD1-4	I_{OZ}		-	-	± 10	μA
Input Current						
RESET, IRQ, TCAP, OSC1, PD0, PD5, PD7	I_{IN}		-	-	± 1	μA
Capacitance Ports (As Input or Output)						
RESET, IRQ, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		5		250	μA
Input Hysteresis Voltage: PB0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: RESET, IRQ, OSC1, TCAP	V_{HYS}		$0.1 \cdot V_{DD}$	1.0	$0.5 \cdot V_{DD}$	V

Control Timing HCL Product Type, $V_{DD} = 5.0V$

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HCL05C4B/C8B $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	4.2	MHz
External Clock Option	f_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal ($f_{OSC} \div 2$)	f_{OP}	-	2.1	MHz
External Clock ($f_{OSC} \div 2$)	f_{OP}	DC	2.1	MHz

CDP68HCL05C4B/C8B Electrical Specifications

Control Timing HCL Product Type, $V_{DD} = 5.0V$ (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Cycle Time (See Figure 15)	t_{CYC}	476	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{LCH}	-	100	ms
RESET Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	125	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{LTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{LIH}	125	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{LIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	-	ns

DC Electrical Specifications HCL Product Type, $V_{DD} = 2.5V - 3.6V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HCL05C4B/C8B $V_{DD} = 2.5V - 3.6V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$ (Note 2)						
Output Voltage	V_{OL}	$I_{LOAD} < 10\mu A$	-	-	0.1	V
	V_{OH}		$V_{DD} - 0.1$	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMP	V_{OH}	$I_{LOAD} = -0.2mA$	$V_{DD} - 0.3$	-	-	V
PD1-4	V_{OH}	$I_{LOAD} = -0.4mA$	$V_{DD} - 0.3$	-	-	V
PC7	V_{OH}	$I_{LOAD} = -1.5mA$	$V_{DD} - 0.3$	-	-	V
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD1-4, TCMP	V_{OL}	$I_{LOAD} = 0.4mA$	-	-	0.3	V
PC7	V_{OL}	$I_{LOAD} = 6.0mA$	-	-	0.3	V
Input High Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IH}		$0.7 \cdot V_{DD}$	-	V_{DD}	V
Input Low Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IL}		V_{SS}	-	$0.2 \cdot V_{DD}$	V
Data Retention Mode	V_{RM}	$T_A = 0^\circ C$ to $70^\circ C$	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	$f_{OSC} = 2.1MHz$ External Square Wave	-	1.0	1.4	mA
WAIT (Notes 7, 9)	I_{DD}		-	0.7	1.0	mA
STOP (Note 8)	I_{DD}	$T_A = 25^\circ C$	-	1.0	5.0	μA
STOP (Note 8)	I_{DD}	$T_A = 0^\circ C$ to $70^\circ C$	-	-	10	μA
Supply Current						
RUN (Note 6)	I_{DD}	$f_{OSC} = 1.0MHz$ External Square Wave	-	0.5	0.75	mA
WAIT (Notes 7, 9)	I_{DD}		-	0.3	0.5	mA
STOP (Note 8)	I_{DD}	$T_A = 25^\circ C$	-	1.0	5.0	μA
STOP (Note 8)	I_{DD}	$T_A = 0^\circ C$ to $70^\circ C$	-	-	10	μA

CDP68HCL05C4B/C8B Electrical Specifications

DC Electrical Specifications HCL Product Type, $V_{DD} = 2.5V - 3.6V$ (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Ports Hi-Z Leakage Current: PA0-7, PB0-7 (without pullups), PC0-7, PD1-4	I_{OZ}		-	-	± 10	μA
Input Current RESET, IRQ, TCAP, OSC1, PD0, PD5, PD7	I_{IN}		-	-	± 1	μA
Capacitance Ports (As Input or Output) RESET, IRQ, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		40	160	300	μA
Input Hysteresis Voltage: PB0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: RESET, IRQ, OSC1, TCAP	V_{HYS}		$0.1 \cdot V_{DD}$	1.0	$0.5 \cdot V_{DD}$	V

Control Timing HCL Product Type, $V_{DD} = 2.4V - 3.6V$

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HCL05C4B/C8B $V_{DD} = 2.4V$ to $3.6V$, $V_{SS} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$ ($V_{DC} = 3.6$)				
Frequency Of Operation Crystal Option	f_{OSC}	-	2.1	MHz
External Clock Option	f_{OSC}	DC	2.1	MHz
Internal Operating Frequency Crystal ($f_{OSC} \div 2$)	f_{OP}	-	1.05	MHz
External Clock ($f_{OSC} \div 2$)	f_{OP}	DC	1.05	MHz
Cycle Time (See Figure 15)	t_{CYC}	952	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
RESET Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer Resolution (Note 12)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH} , t_{TL}	250	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 11)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{LIH}	250	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{LIH}	(Note 13)	-	t_{CYC}
OSC1 Pulse Width	t_{OH} , t_{OL}	200	-	ns

DC Electrical Specifications HCL Product Type, $V_{DD} = 1.8V - 2.4V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HCL05C4B/C8B $V_{DD} = 1.8V - 2.4V$, $V_{SS} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$, Unless Otherwise Specified						
Output Voltage	V_{OL}	$I_{LOAD} < 10\mu A$	-	-	0.1	V
	V_{OH}		$V_{DD} - 0.1$	-	-	V
Output High Voltage PA0-7, PB0-7, PC0-6, TCMP	V_{OH}	$I_{LOAD} = -0.1mA$	$V_{DD} - 0.3$	-	-	V
PD1-4	V_{OH}	$I_{LOAD} = -0.2mA$	$V_{DD} - 0.3$	-	-	V
PC7	V_{OH}	$I_{LOAD} = -0.75mA$	$V_{DD} - 0.3$	-	-	V

CDP68HCL05C4B/C8B Electrical Specifications

DC Electrical Specifications HCL Product Type, $V_{DD} = 1.8V - 2.4V$ (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD1-4, TCMPL	V_{OL}	$I_{LOAD} = 0.2mA$	-	-	0.3	V
PC7	V_{OL}	$I_{LOAD} = 2.0mA$	-	-	0.3	V
Input High Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, \overline{IRQ} , RESET, OSC1	V_{IH}		$0.7 \cdot V_{DD}$	-	V_{DD}	V
Input Low Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, \overline{IRQ} , RESET, OSC1	V_{IL}		V_{SS}	-	$0.2 \cdot V_{DD}$	V
Data Retention Mode	V_{RM}	$T_A = 0^{\circ}C$ to $70^{\circ}C$	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	$f_{OSC} = 1.0MHz$ External Square Wave	-	300	600	μA
WAIT (Notes 7, 9)	I_{DD}		-	250	400	μA
STOP (Note 8)	I_{DD}	$T_A = 25^{\circ}C$	-	1.0	2.0	μA
STOP (Note 8)	I_{DD}	$T_A = 0^{\circ}C$ to $70^{\circ}C$	-	-	5.0	μA
I/O Ports Hi-Z Leakage Current:						
PA0-7, PB0-7 (without pullups), PC0-7, PD1-4	I_{OZ}		-	-	± 10	μA
Input Current						
\overline{RESET} , \overline{IRQ} , TCAP, OSC1, PD0, PD5, PD7	I_{IN}		-	-	± 1	μA
Capacitance Ports (As Input or Output)						
\overline{RESET} , \overline{IRQ} , TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		15	110	200	μA
Input Hysteresis Voltage: PB0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: \overline{RESET} , \overline{IRQ} , OSC1, TCAP	V_{HYS}		$0.1 \cdot V_{DD}$	1.0	$0.5 \cdot V_{DD}$	V

Control Timing HCL Product Type, $V_{DD} = 1.8V - 2.4V$

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HCL05C4B/C8B $V_{DD} = 1.8V$ to $2.4V$, $V_{SS} = 0V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$ ($V_{DC} = 2.4$)				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	1.0	MHz
External Clock Option	f_{OSC}	DC	1.0	MHz
Internal Operating Frequency				
Crystal ($f_{OSC} \div 2$)	f_{OP}	-	0.5	MHz
External Clock ($f_{OSC} \div 2$)	f_{OP}	DC	0.5	MHz
Cycle Time (See Figure 15)	t_{CYC}	2000	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{LCH}	-	100	ms
\overline{RESET} Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}

CDP68HCL05C4B/C8B Electrical Specifications

Control Timing HCL Product Type, $V_{DD} = 1.8V - 2.4V$ (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Timer				
Resolution (Note 12)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	500	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{LIH}	500	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{LIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	400	-	ns

CDP68HSC05C4B/C8B Electrical Specifications

DC Electrical Specifications HSC Product Type, $V_{DD} = 5.0V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HSC05C4B/C8B $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$ (Note 2)						
Output Voltage	V_{OL}	$I_{LOAD} < 10\mu A$	-	-	0.1	V
	V_{OH}		$V_{DD} - 0.1$	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMP	V_{OH}	$I_{LOAD} = -0.8mA$	$V_{DD} - 0.8$	-	-	V
PD1-4	V_{OH}	$I_{LOAD} = -1.6mA$	$V_{DD} - 0.8$	-	-	V
PC7	V_{OH}	$I_{LOAD} = -5.0mA$	$V_{DD} - 0.8$	-	-	V
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD1-4, TCMP	V_{OL}	$I_{LOAD} = 1.6mA$	-	-	0.4	V
PC7	V_{OL}	$I_{LOAD} = 10.0mA$	-	-	0.4	V
Input High Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IH}		$0.7 \cdot V_{DD}$	-	V_{DD}	V
Input Low Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IL}		V_{SS}	-	$0.2 \cdot V_{DD}$	V
Data Retention Mode	V_{RM}	$T_A = 0^\circ C$ to $70^\circ C$	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	$f_{OSC} = 8.0MHz$ External Square Wave	-	7.0	11.0	mA
WAIT (Notes 7, 9)	I_{DD}		-	2.0	6.5	mA
STOP (Note 8)	I_{DD}	$T_A = 25^\circ C$	-	1.0	20.0	μA
STOP (Note 8)	I_{DD}	$T_A = -40^\circ C$ to $85^\circ C$	-	-	50	μA
I/O Ports Hi-Z Leakage Current:						
PA0-7, PB0-7 (without pullups), PC0-7, PD1-4	I_{OZ}		-	-	± 10	μA
Input Current						
RESET, IRQ, TCAP, OSC1, PD0, PD5, PD7	I_{IN}		-	-	± 1	μA
Capacitance Ports (As Input or Output)						
RESET, IRQ, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF
Input Pullup Current (Note 10)	I_{IN}		175	385	750	μA
Input Hysteresis Voltage: PB0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: RESET, IRQ, OSC1, TCAP	V_{HYS}		$0.1 \cdot V_{DD}$	1.0	$0.5 \cdot V_{DD}$	V

Control Timing HSC Product Type, $V_{DD} = 5.0V$

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HSC05C4B/C8B $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$ (Note 2)				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	8.2	MHz
External Clock Option	f_{OSC}	DC	8.2	MHz
Internal Operating Frequency				
Crystal ($f_{OSC} \div 2$)	f_{OP}	-	4.1	MHz
External Clock ($f_{OSC} \div 2$)	f_{OP}	DC	4.1	MHz

CDP68HSC05C4B/C8B Electrical Specifications

Control Timing HSC Product Type, $V_{DD} = 5.0V$ (Continued)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Cycle Time (See Figure 15)	t_{CYC}	244	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
RESET Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH}, t_{TL}	64	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{LIH}	64	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{LIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	50	-	ns

DC Electrical Specifications HSC Product Type, $V_{DD} = 2.6V - 3.6V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CDP68HSC05C4B/C8B $V_{DD} = 2.4V - 3.6V, V_{SS} = 0V, T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 2)						
Output Voltage	V_{OL}	$I_{LOAD} \leq 10\mu A$	-	-	0.1	V
	V_{OH}		$V_{DD} - 0.1$	-	-	V
Output High Voltage						
PA0-7, PB0-7, PC0-6, TCMF	V_{OH}	$I_{LOAD} = -0.2mA$	$V_{DD} - 0.3$	-	-	V
PD1-4	V_{OH}	$I_{LOAD} = -0.4mA$	$V_{DD} - 0.3$	-	-	V
PC7	V_{OH}	$I_{LOAD} = -1.5mA$	$V_{DD} - 0.3$	-	-	V
Output Low Voltage						
PA0-7, PB0-7, PC0-6, PD1-4, TCMF	V_{OL}	$I_{LOAD} = 0.4mA$	-	-	0.3	V
PC7	V_{OL}	$I_{LOAD} = 6.0mA$	-	-	0.3	V
Input High Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IH}		$0.7 \cdot V_{DD}$	-	V_{DD}	V
Input Low Voltage						
PA0-7, PB0-7, PC0-7, PD0-5, PD7, TCAP, IRQ, RESET, OSC1	V_{IL}		V_{SS}	-	$0.2 \cdot V_{DD}$	V
Data Retention Mode	V_{RM}	$T_A = 0^{\circ}C$ to $70^{\circ}C$	1.2	-	-	V
Supply Current						
RUN (Note 6)	I_{DD}	$f_{OSC} = 4.2MHz$ External Square Wave	-	2.5	4.0	mA
WAIT (Notes 7, 9)	I_{DD}		-	1.0	2.0	mA
STOP (Note 8)	I_{DD}	$T_A = 25^{\circ}C$	-	1.0	8.0	μA
STOP (Note 8)	I_{DD}	$T_A = -40^{\circ}C$ to $85^{\circ}C$	-	-	20	μA
I/O Ports Hi-Z Leakage Current:						
PA0-7, PB0-7 (without pullups), PC0-7, PD1-4	I_{OZ}		-	-	± 10	μA
Input Current						
RESET, IRQ, TCAP, OSC1, PD0, PD5, PD7	I_{IN}		-	-	± 1	μA
Capacitance Ports (As Input or Output)						
RESET, IRQ, TCAP, OSC1, PD0-5, PD7	C_{OUT}		-	-	12	pF
	C_{IN}		-	-	8	pF

CDP68HSC05C4B/C8B Electrical Specifications

DC Electrical Specifications HSC Product Type, $V_{DD} = 2.6V - 3.6V$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Current (Note 10)	I_{IN}		50	160	350	μA
Input Hysteresis Voltage: PB0-7	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: \overline{RESET} , \overline{IRQ} , OSC1, TCAP	V_{HYS}		$0.1 \cdot V_{DD}$	1.0	$0.5 \cdot V_{DD}$	V

Control Timing HSC Product Type, $V_{DD} = 2.4V - 3.6V$

PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HSC05C4B/C8B $V_{DD} = 2.4V - 3.6V$, $V_{SS} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 2)				
Frequency Of Operation				
Crystal Option	f_{OSC}	-	4.2	MHz
External Clock Option	f_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal ($f_{OSC} \div 2$)	f_{OP}	-	2.1	MHz
External Clock ($f_{OSC} \div 2$)	f_{OP}	DC	2.1	MHz
Cycle Time (See Figure 15)	t_{CYC}	476	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal (See Figure 15)	t_{OXOV}	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator) (See Figure 1)	t_{ILCH}	-	100	ms
\overline{RESET} Pulse Width (See Figure 15)	t_{RL}	1.5	-	t_{CYC}
Timer				
Resolution (Note 12)	t_{RES}	4.0	-	t_{CYC}
Input Capture Pulse Width (See Figures 2, 23)	t_{TH} , t_{TL}	125	-	ns
Input Capture Pulse Period (See Figures 2, 23)	t_{TLTL}	(Note 13)	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 16B)	t_{LIH}	125	-	ns
Interrupt Pulse Period (See Figure 16B)	t_{LIH}	(Note 11)	-	t_{CYC}
OSC1 Pulse Width	t_{OH} , t_{OL}	90	-	ns

NOTES:

- This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
- Includes ports used as input/output pins; Ports used as input only pins, Ports used as output only pins.
- All values shown reflect average measurement.
- Typical values at midpoint of voltage range, $25^{\circ}C$ only.
- Run (Operating) I_{DD} , Wait I_{DD} : Measured using external square-wave clock source, all inputs 0.2V from rail, no DC loads, less than 50pF on all outputs, $C_L = 20pF$ on OSC2.
- Wait, Stop I_{DD} : All ports configured as inputs, $V_{IL} = 0.2V$, $V_{IH} = V_{DD} - 0.2V$.
- Stop I_{DD} measured with OSC1 = V_{SS} .
- Wait I_{DD} is affected linearly by the OSC2 capacitance.
- Input pullup current measured with $V_{IL} = 0.2V$.
- The minimum period t_{LIH} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC} .
- Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
- The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC} .

CDP68HC05C4B/C8B, CDP68HCL05C4B/C8B, CDP68HSC05C4B/C8B

Serial Peripheral Interface (SPI) Timing - HC, HCL Product Type, $V_{DD} = 5.0V$

NUMBER	PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HC05C4B/C8B, CDP68HCL05C4B/C8B, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$, Unless Otherwise Specified					
	Operating Frequency				
	Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 16)
	Slave	$f_{OP(S)}$	DC	2.1	MHz
1	Cycle Time				
	Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	480	-	ns
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 14)	-	-
	Slave	$t_{LEAD(S)}$	240	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 14)	-	-
	Slave	$t_{LAG(S)}$	720	-	ns
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	340	-	ns
	Slave	$t_{W(SCKH)S}$	190	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	340	-	ns
	Slave	$t_{W(SCKL)S}$	190	-	ns
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	100	-	ns
	Slave	$t_{SU(S)}$	100	-	ns
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	100	-	ns
	Slave	$t_{H(S)}$	100	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	120	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	240	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_V(M)$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 15)	$t_V(S)$	-	240	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time ($V_{DD} = 20\%$ to 70% , $C_L = 200pF$)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{R(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, \overline{SS})	$t_{R(S)}$	-	2.0	μs
13	Fall Time ($V_{DD} = 20\%$ to 70% , $C_L = 200pF$)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{F(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, \overline{SS})	$t_{F(S)}$	-	2.0	μs

CDP68HC05C4B/C8B, CDP68HCL05C4B/C8B, CDP68HSC05C4B/C8B

Serial Peripheral Interface (SPI) Timing - HC, HCL Product Type, $V_{DD} = 3.3V$

NUMBER	PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HC05C4B/C8B, CDP68HCL05C4B/C8B $V_{DD} = 3.3V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$, Unless Otherwise Specified					
	Operating Frequency				
	Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 16)
	Slave	$f_{OP(S)}$	DC	1.0	MHz
1	Cycle Time				
	Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	1.0	-	μs
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 14)	-	-
	Slave	$t_{LEAD(S)}$	500	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 14)	-	-
	Slave	$t_{LAG(S)}$	1.5	-	μs
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	720	-	ns
	Slave	$t_{W(SCKH)S}$	400	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	720	-	ns
	Slave	$t_{W(SCKL)S}$	400	-	ns
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	200	-	ns
	Slave	$t_{SU(S)}$	200	-	ns
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	200	-	ns
	Slave	$t_{H(S)}$	200	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	250	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	500	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_V(M)$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 15)	$t_V(S)$	-	500	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time ($V_{DD} = 20\%$ to 70% , $C_L = 200pF$)				
	SPI Outputs (SCK, MOSI, MISO)	$t_R(M)$	-	200	ns
	SPI Inputs (SCK, MOSI, MISO, \overline{SS})	$t_R(S)$	-	2.0	μs
13	Fall Time ($V_{DD} = 20\%$ to 70% , $C_L = 200pF$)				
	SPI Outputs (SCK, MOSI, MISO)	$t_F(M)$	-	200	ns
	SPI Inputs (SCK, MOSI, MISO, \overline{SS})	$t_F(S)$	-	2.0	μs

CDP68HC05C4B/C8B, CDP68HCL05C4B/C8B, CDP68HSC05C4B/C8B

Serial Peripheral Interface (SPI) Timing - HSC, $V_{DD} = 5.0V$

NUMBER	PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HSC05C4B/C8B $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0^\circ C$ to $85^\circ C$, Unless Otherwise Specified					
	Operating Frequency				
	Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 16)
	Slave	$f_{OP(S)}$	DC	4.1	MHz
1	Cycle Time				
	Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	244	-	ns
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 14)	-	-
	Slave	$t_{LEAD(S)}$	122	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 14)	-	-
	Slave	$t_{LAG(S)}$	366	-	ns
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	166	-	ns
	Slave	$t_{W(SCKH)S}$	93	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	166	-	ns
	Slave	$t_{W(SCKL)S}$	93	-	ns
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	49	-	ns
	Slave	$t_{SU(S)}$	49	-	ns
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	49	-	ns
	Slave	$t_{H(S)}$	49	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	61	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	122	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_{V(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 15)	$t_{V(S)}$	-	122	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time ($V_{DD} = 20\%$ to 70% , $C_L = 200pF$)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{R(M)}$	-	50	ns
	SPI Inputs (SCK, MOSI, MISO, \overline{SS})	$t_{R(S)}$	-	1.0	μs
13	Fall Time ($V_{DD} = 20\%$ to 70% , $C_L = 200pF$)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{F(M)}$	-	50	ns
	SPI Inputs (SCK, MOSI, MISO, \overline{SS})	$t_{F(S)}$	-	1.0	μs

CDP68HC05C4B/C8B, CDP68HCL05C4B/C8B, CDP68HSC05C4B/C8B

Serial Peripheral Interface (SPI) Timing - HSC, $V_{DD} = 2.4V - 3.6V$

NUMBER	PARAMETER	SYMBOL	MIN	MAX	UNITS
CDP68HSC05C4B/C8B, $V_{DD} = 2.4V$ to $3.6V$, $V_{SS} = 0V$, $T_A = 0^{\circ}C$ to $85^{\circ}C$ Unless Otherwise Specified					
	Operating Frequency				
	Master	$f_{OP(M)}$	DC	0.5	f_{OP} (Note 16)
	Slave	$f_{OP(S)}$	DC	2.1	MHz
1	Cycle Time				
	Master	$t_{CYC(M)}$	2.0	-	t_{CYC}
	Slave	$t_{CYC(S)}$	480	-	ns
2	Enable Lead Time				
	Master	$t_{LEAD(M)}$	(Note 14)	-	-
	Slave	$t_{LEAD(S)}$	240	-	ns
3	Enable Lag Time				
	Master	$t_{LAG(M)}$	(Note 14)	-	-
	Slave	$t_{LAG(S)}$	720	-	ns
4	Clock (SCK) High Time				
	Master	$t_{W(SCKH)M}$	340	-	ns
	Slave	$t_{W(SCKH)S}$	190	-	ns
5	Clock (SCK) Low Time				
	Master	$t_{W(SCKL)M}$	340	-	ns
	Slave	$t_{W(SCKL)S}$	190	-	ns
6	Data Setup Time (Inputs)				
	Master	$t_{SU(M)}$	100	-	ns
	Slave	$t_{SU(S)}$	100	-	ns
7	Data Hold Time (Inputs)				
	Master	$t_{H(M)}$	100	-	ns
	Slave	$t_{H(S)}$	100	-	ns
8	Access Time (Time to Data Active from High Impedance State)				
	Slave	t_A	0	120	ns
9	Disable Time (Hold Time to High Impedance State)				
	Slave	t_{DIS}	-	240	ns
10	Data Valid Time				
	Master (Before Capture Edge)	$t_{V(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge) (Note 15)	$t_{V(S)}$	-	240	ns
11	Data Hold Time (Outputs)				
	Master (After Capture Edge)	$t_{HO(M)}$	0.25	-	$t_{CYC(M)}$
	Slave (After Enable Edge)	$t_{HO(S)}$	0	-	ns
12	Rise Time ($V_{DD} = 20\%$ to 70% , $C_L = 200pF$)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{R(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, \overline{SS})	$t_{R(S)}$	-	2.0	μs
13	Fall Time ($V_{DD} = 20\%$ to 70% , $C_L = 200pF$)				
	SPI Outputs (SCK, MOSI, MISO)	$t_{F(M)}$	-	100	ns
	SPI Inputs (SCK, MOSI, MISO, \overline{SS})	$t_{F(S)}$	-	2.0	μs

NOTES:

14. Signal Production depends on software.

15. Assumes 200pF load on all SPI pins.

16. Note that the units this specification uses is f_{OP} (internal operating frequency), not MHz! In the master mode the SPI bus is capable of running at one-half of the device's internal operating frequency, therefore 5V: 2.0MHz and 2.4V to 3.6V: 500kHz maximum.